

# 8-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-8L MB89930C Series

### MB89P935C/PV930A

#### ■ DESCRIPTION

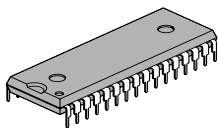
The MB89930C series is a line of single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as timers, serial interfaces, A/D converter and external interrupts.

#### ■ FEATURES

- MB89600 Series CPU core
- Minimum execution time: 0.4  $\mu$ s/10MHz
- Interrupt processing time: 3.6  $\mu$ s/10MHz
- I/O ports: max. 21 channels
- 21-bit timebase timer
- 8-bit PWM timer
- 8/16-bit capture timer/counter
- 10-bit A/D converter: 8 channels
- UART
- 8-bit serial I/O
- External interrupt 1 (Edge): 3 channels
- External interrupt 2 (Level): 8 channels
- Wild Register: 2 bytes
- OTPROM Read protection (Refer to "■ Programming the OTPROM in MB89P935C")
- Low-power consumption modes (sleep mode and stop mode)
- DIP and SH-DIP package
- CMOS Technology

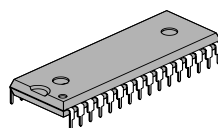
#### ■ PACKAGE

32-pin plastic DIP



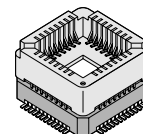
(DIP-32P-M04)

32-pin plastic SH-DIP



(DIP-32P-M05)

48-pin ceramic MQFP



(MQP-48C-P01)

# MB89930C Series

## ■ PRODUCT LINEUP

Part number Parameter	MB89P935C	MB89PV930A
<b>Classification</b>	One-time PROM product (read protection)	Piggyback/evaluation product (for evaluation and development)
<b>ROM size</b>	16K x 8-bit (internal PROM)	32K x 8-bit (external EPROM)
<b>RAM size</b>	512 x 8 bits	
<b>CPU functions</b>	Number of instructions: : 136 Instruction bit length: : 8 bits Instruction length: : 1 to 3 bytes Data bit length: : 1, 8, 16 bits Minimum execution time: : 0.4 μs to 6.4 μs(10 MHz) Minimum interrupt processing time: : 3.6 μs to 57.6 μs(10 MHz)	
<b>Ports</b>	General-purpose I/O ports (CMOS): 21 (also serve as peripherals) (4 ports can be set as N-ch open-drain type)	
<b>21-bit timebase timer</b>	21-bit Interrupt cycle: 0.82, 3.3, 26.2, or 419.4 ms at 10-MHz main clock	
<b>Watchdog timer</b>	Reset generation cycle: 209.7ms minimum at 10-MHz main clock	
<b>8-bit PWM timer</b>	8-bit interval timer operation (square output capable, operating clock cycle: 1 tinst, 16 tinst, 64 tinst, and 8/16-bit capture timer/counter output) 8-bit resolution PWM operation (conversion cycle: 256 tinst, 4096 tinst, 16384 tinst and 256 times 8/16-bit capture timer/counter output)	
<b>8/16-bit capture timer/counter</b>	8-bit capture timer/counter x 1 channel + 8-bit timer or 16-bit capture timer/counter x 1 channel Capable of event count operation and square wave output using external clock input with 8-bit timer 0 or 16-bit counter	
<b>UART</b>	Transfer data length: 6/7/8 bits Transfer rate: 300 to 9600 bps at 10 MHz	
<b>8-bit Serial I/O</b>	8 bits LSB first/MSB first selectable One clock selectable from four operation clocks (one external shift clock, three internal shift clocks: 2 tinst, 8 tinst and 32 tinst)	
<b>12-bit PPG timer</b>	Output frequency: Pulse width and cycle selectable	
<b>External interrupt 1 (wake-up function)</b>	3 channels (interrupt vector, request flag, request output enable) Edge selectable (Rising edge, falling edge, or both edges) Also available for resetting stop/sleep mode (Edge detectable even in stop mode)	
<b>External interrupt 2 (wake-up function)</b>	1 channel with 8 inputs (Independent L-level interrupt and input enable) Also available for resetting stop/sleep mode (Level detectable even in stop mode)	
<b>10-bit A/D converter</b>	10-bit precision x 8 channels A/D conversion function (Conversion time: 38 tinst) Continuous activation by 8/16-bit timer/counter output or timebase timer counter	
<b>Wild Register</b>	8-bit x 2	
<b>Standby mode</b>	Sleep mode and Stop mode	
<b>Power supply voltage</b>	3.0V to 5.5V	2.7V to 5.5V

Note: 1 Tinst = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89P935C	MB89PV930A
DIP-32P-M04	O	X
DIP-32P-M05	O	X
MQP-48C-P01	X	O

O : Availabe    X : Not available

## ■ DIFFERENCES AMONG PRODUCTS

### 1. A/D Converter Power Supply Pin (AV<sub>CC</sub>) and Reference Voltage Input Pin (AVR)

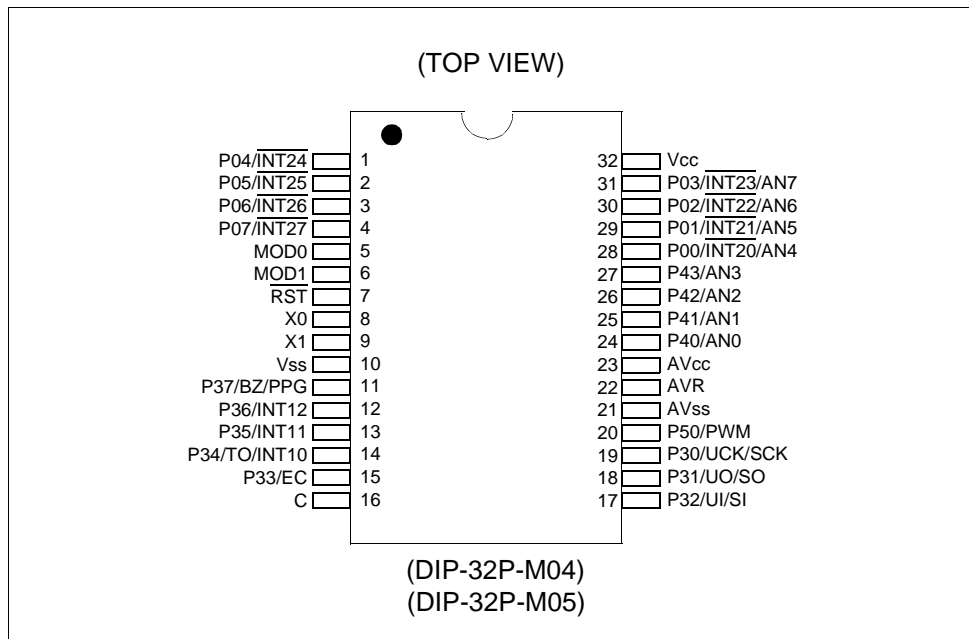
There are AV<sub>CC</sub> and AVR pins in MB89P935C. They are absent in MB89PV930A. Hence, the electrical characteristics of MB89P935C is different from that of MB89PV930A. (Refer to "■ ELECTRICAL CHARACTERISTICS 5. A/D Converter Electrical Characteristics")

### 2. Curent Consumption

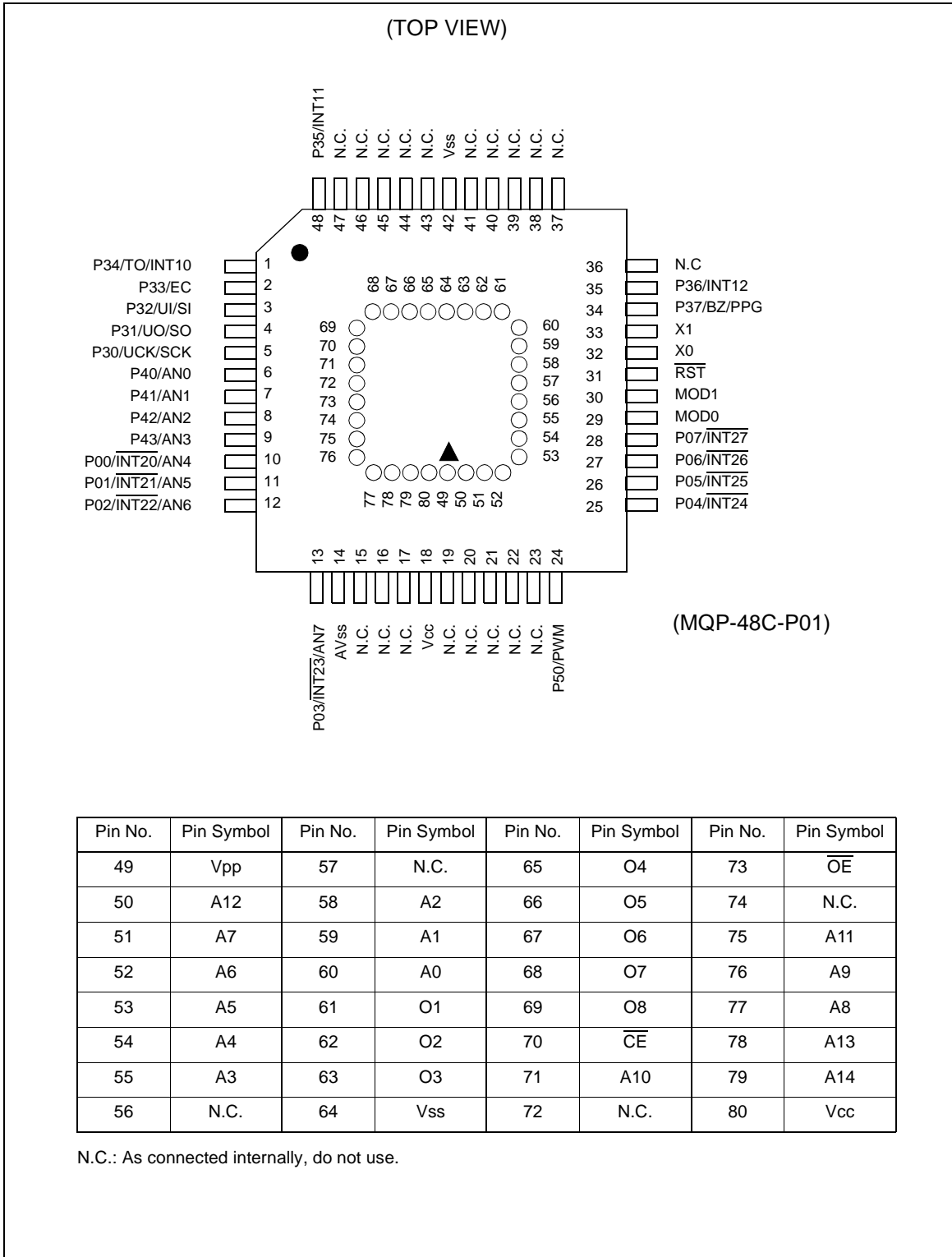
In the case of the MB89PV930A, add the current consumed by the EPROM which is connected to the top socket.

# MB89930C Series

## ■ PIN ASSIGNMENT



# MB89930C Series



# MB89930C Series

## ■ PIN DESCRIPTION

Pin Number		Pin Name	I/O Circuit Type	Function
DIP <sup>*1</sup>	MQFP <sup>*2</sup>			
8	32	X0	A	Pins for connecting the crystal resonator for the main clock. To use an external clock, input the signal to X0 and leave X1 open.
9	33	X1		
5	29	MOD0	B	Memory access mode setting input pins. Connect the pin directly to Vss.
6	30	MOD1		
7	31	$\overline{RST}$	C	Reset I/O pin. The pin is N-ch open-drain type with pull-up resistor and a hysteresis input as well. The pin outputs the "L" level when an internal reset request is present. Inputting an "L" level initializes internal circuits.
28 to 31	10 to 13	$\overline{P00/INT20/AN4}$ to $\overline{P03/INT23/AN7}$	G	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2 or as an A/D converter analog input. The input of external interrupt 2 is a hysteresis input.
1 to 4	25 to 28	$\overline{P04/INT24}$ to $\overline{P07/INT27}$	D	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2. The input of external interrupt 2 is a hysteresis input.
19	5	P30/UCK/SCK	D	General-purpose CMOS I/O port. This pin also serves as the clock I/O pin for the UART or 8-bit serial I/O. The resource is a hysteresis input.
18	4	P31/UO/SO	E	General-purpose CMOS I/O port. This pin also serves as the data output pin for the UART or 8-bit serial I/O.
17	3	P32/UI/SI	D	General-purpose CMOS I/O port. This pin also serves as the data input pin for the UART or 8-bit serial I/O. The resource is a hysteresis input.
15	2	P33/EC	D	General-purpose CMOS I/O port. This pin also serves as the external clock input pin for the 8/16-bit capture timer/counter. The resource is a hysteresis input.
14	1	P34/TO/INT10	D	General-purpose CMOS I/O port. This pin also serves as the output pin for the 8/16-bit capture timer/counter or as the input pin for external interrupt 1. The resource is a hysteresis input.
13,12	48, 35	P35/INT11, P36/INT12	D	General-purpose CMOS I/O ports. These pins also serve as the input pins for external interrupt 1. The resource is a hysteresis input.
11	34	P37/BZ/PPG	E	General-purpose CMOS I/O port. This pin also serves as the buzzer output pin or the 12-bit programmable pulse generator output.
20	24	P50/PWM	E	General-purpose CMOS I/O port. The pin also serves as the 8-bit PWM output pin.
24 to 27	6 to 9	P40/AN0 to P43/AN3	F	General-purpose CMOS I/O ports. These pins can also be used as N-channel open-drain ports. The pins also serve as A/D converter analog input pins.

\*1: DIP-32P-M04 and DIP-32P-M05

\*2: MQP-48C-P01

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# MB89930C Series

(Continued)

Pin No.		Pin Name	I/O Circuit Type	Function
DIP <sup>*1</sup>	MQFP <sup>*2</sup>			
32	18	Vcc	—	Power supply pin
10	42	Vss	—	Power (GND) pin
23	—	AVcc	—	Power supply pin for A/D converter.
21	14	AVss	—	Power supply pin for A/D converter. Apply equal potential to this pin and the Vss pin.
22	—	AVR	—	Reference voltage input pin for the A/D converter.
16	—	C	—	Capacitance pin for regulating the power supply. Connect an external ceramic capacitor of about 0.1 $\mu$ F

\*1: DIP-32P-M04 and DIP-32P-M05

\*2: MQP-48C-P01

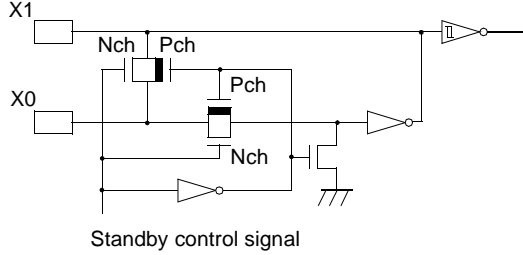
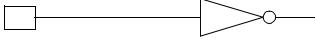
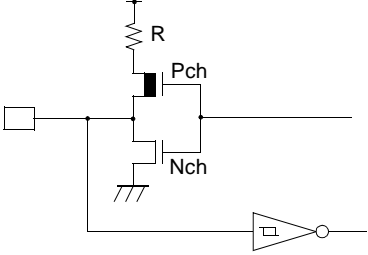
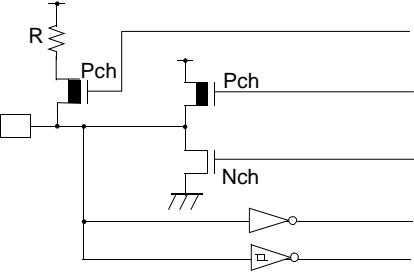
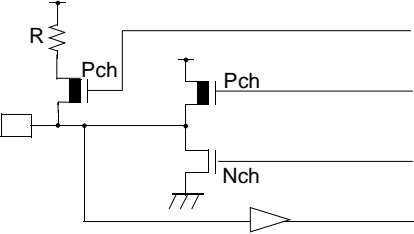
# MB89930C Series

## •External EPROM Socket (MB89PV930A only)

Pin Number MQFP <sup>1</sup>	Pin Name	I/O	Function
49	V <sub>pp</sub>	O	"H" level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins.
61 62 63	O1 O2 O3	I	Data input pins.
64	V <sub>ss</sub>	O	Power supply pin (GND).
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins.
70	$\overline{\text{CE}}$	O	Chip enable pin for the ROM. Outputs "H" in standby mode.
71	A10	O	Address output pin.
72	$\overline{\text{OE}}$	O	Output enable pin for the ROM. Always outputs "L".
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins.
80	V <sub>cc</sub>	O	Power supply pin for the EPROM.
56 57 72 74	N.C.	—	Internally connected pins. Always leave open.



## ■ I/O CIRCUIT TYPE

I/O Circuit Type	Circuit	Remarks
A	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> <li>• Crystal oscillation type</li> </ul>
B		<ul style="list-style-type: none"> <li>• CMOS input</li> </ul>
C		<ul style="list-style-type: none"> <li>• The pull-up resistance (P-channel) Approx. 50 kΩ.</li> <li>• Hysteresis input</li> </ul>
D		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input (Resource input)</li> <li>• Selectable pull-up resistor Approx. 50 kΩ.</li> </ul>
E		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Selectable pull-up resistor Approx. 50 kΩ</li> </ul>

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# MB89930C Series

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<p>F</p>		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Analog input</li> <li>• N-ch open-drain output available</li> </ul>
<p>G</p>		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input (Resource input)</li> <li>• Analog input</li> <li>• Selectable pull-up resistor Approx. 50kΩ.</li> </ul>

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between  $V_{CC}$  and  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply ( $AV_{CC}$  and  $AVR$ ) and analog input from exceeding the digital power supply ( $V_{CC}$ ) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor of at least 2 kilohms between the pin and the power supply.

### 3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 4. Power Supply Voltage Fluctuations

Although  $V_{CC}$  power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{CC}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{CC}$  value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 5. Treatment of Power Supply Pins on Microcontrollers with A/D Converter

Connect to be  $AV_{CC} = V_{CC}$  and  $AV_{SS} = AVR = V_{SS}$  even if the A/D converter is not in use.

### 6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

### 7. About the Wild Register Function

No wild register can be debugged on the MB89PV930A. For the operation check, test the MB89P935C installed on a target system.

### 8. Program Execution in RAM

When the MB89PV930A is used, no program can be executed in RAM.

# MB89930C Series

## ■ PROGRAMMING THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C256A-20TVM

### 2. Programming Socket Adaptor

To program to the PROM using an EPROM programmer, use the socket adaptor (manufacturer: Sun Hayato Co., Ltd.) listed below.

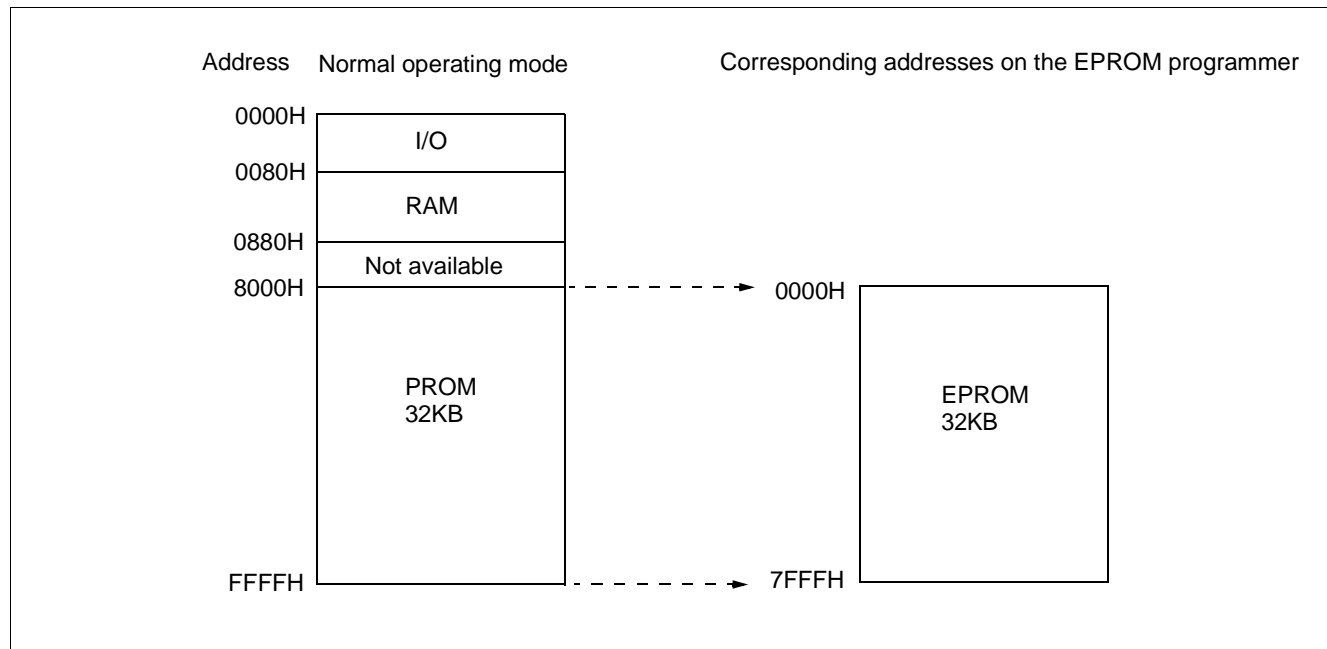
Package	Adaptor socket part number
LCC-32	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3986-0403

FAX 81-3-5396-9106

### 3. Memory Space

Memory space in each mode is diagrammed below.

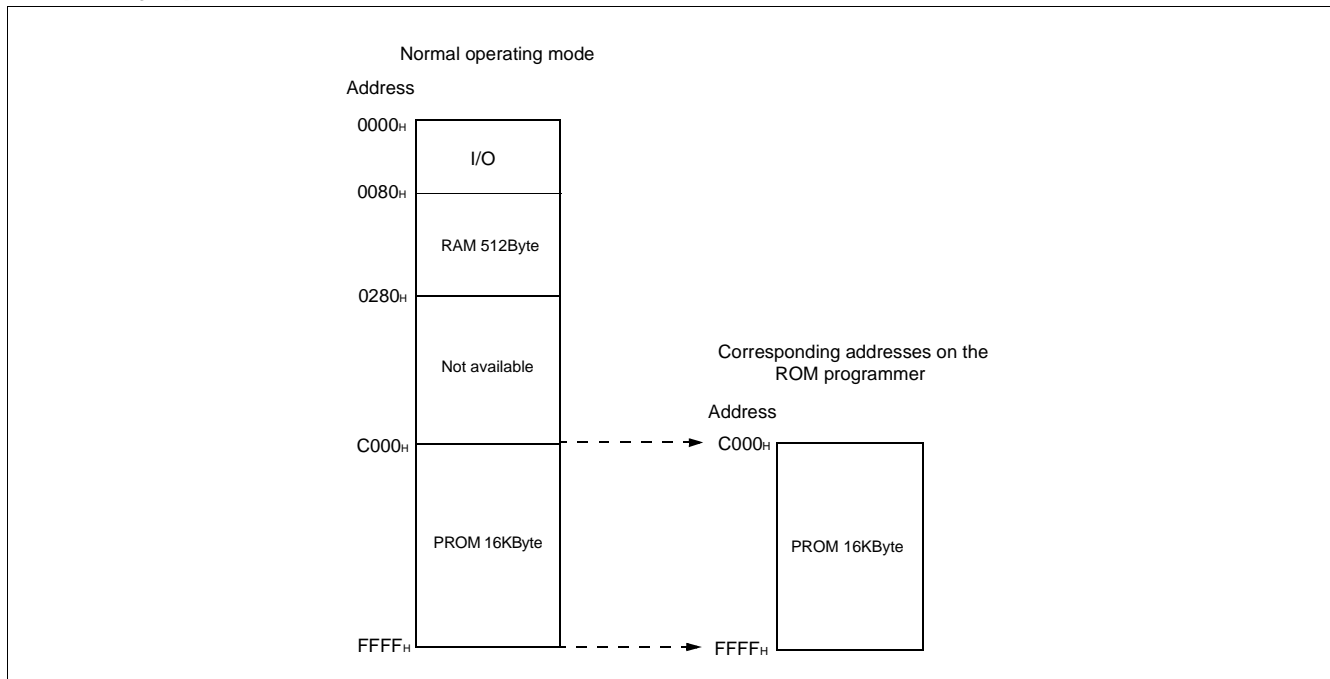


### 4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0000<sub>H</sub> to 7FFF<sub>H</sub>.
- (3) Program to 0000<sub>H</sub> to 7FFF<sub>H</sub> with the EPROM programmer.

## ■ PROGRAMMING THE OTPROM IN MB89P935C

### 1. Memory Space



### 2. Programming the OTPROM

- To program the OTPROM using EPROM programmer AF200 (manufacturer: Yokogawa Digital Computer Corp.).  
Inquiry : Yokogawa Digital Computer Corp. : TEL (81)-42-333-6224
- To program the OTPROM using FUJITSU MCU programmer MB91919-001.  
Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770  
FAX (65)-2810220

Note : Programming the OTPROM in MB89P935C is serial programming mode only.

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# MB89930C Series

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### 3. Programming Adaptor for OTPROM

- To program the OTPROM using EPROM programmer AF200, use the programming adaptor (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adaptor socket part number
DIP-32P-M04	ROM3-FPT30M02-8LA-FJ
DIP-32P-M05	Not available

Inquiry : Sun Hayato Co., Ltd : TEL (81)-3-3986-0403

FAX (81)-3-5396-9106

- To program the OTPROM using FUJITSU MCU programmer MB91919-001, use the programming adaptor listed below.

Package	Adaptor socket part number
DIP-32P-M04	MB91919-809 + MB91919-800
DIP-32P-M05	MB91919-814 + MB91919-800

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

FAX (65)-2810220

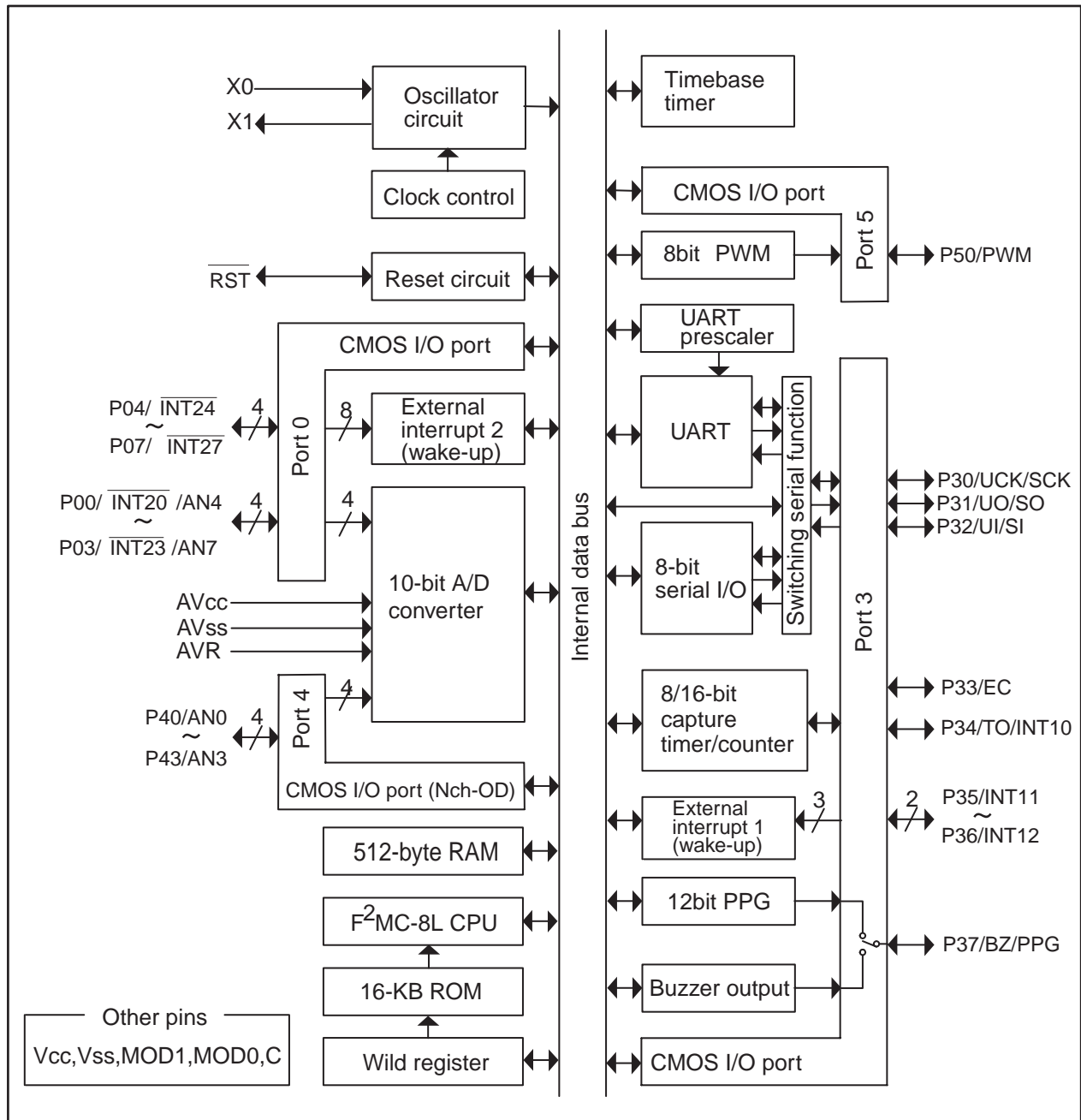
### 4. OTPROM Content Protection

OTPROM content can be read using serial programmer if the OTPROM content protection mechanism is not activated.

One predefined area of the OTPROM (FFFC<sub>H</sub>) is assigned to be used for preventing the read access of OTPROM content. If the protection code "00<sub>H</sub>" is written in this address (FFFC<sub>H</sub>), the OTPROM content cannot be read by any serial programmer.

Note : The program written into the OTPROM cannot be verified once the OTPROM protection code is written ("00<sub>H</sub>" in FFFC<sub>H</sub>). It is advised to write the OTPROM protection code at last.

## ■ Block Diagram

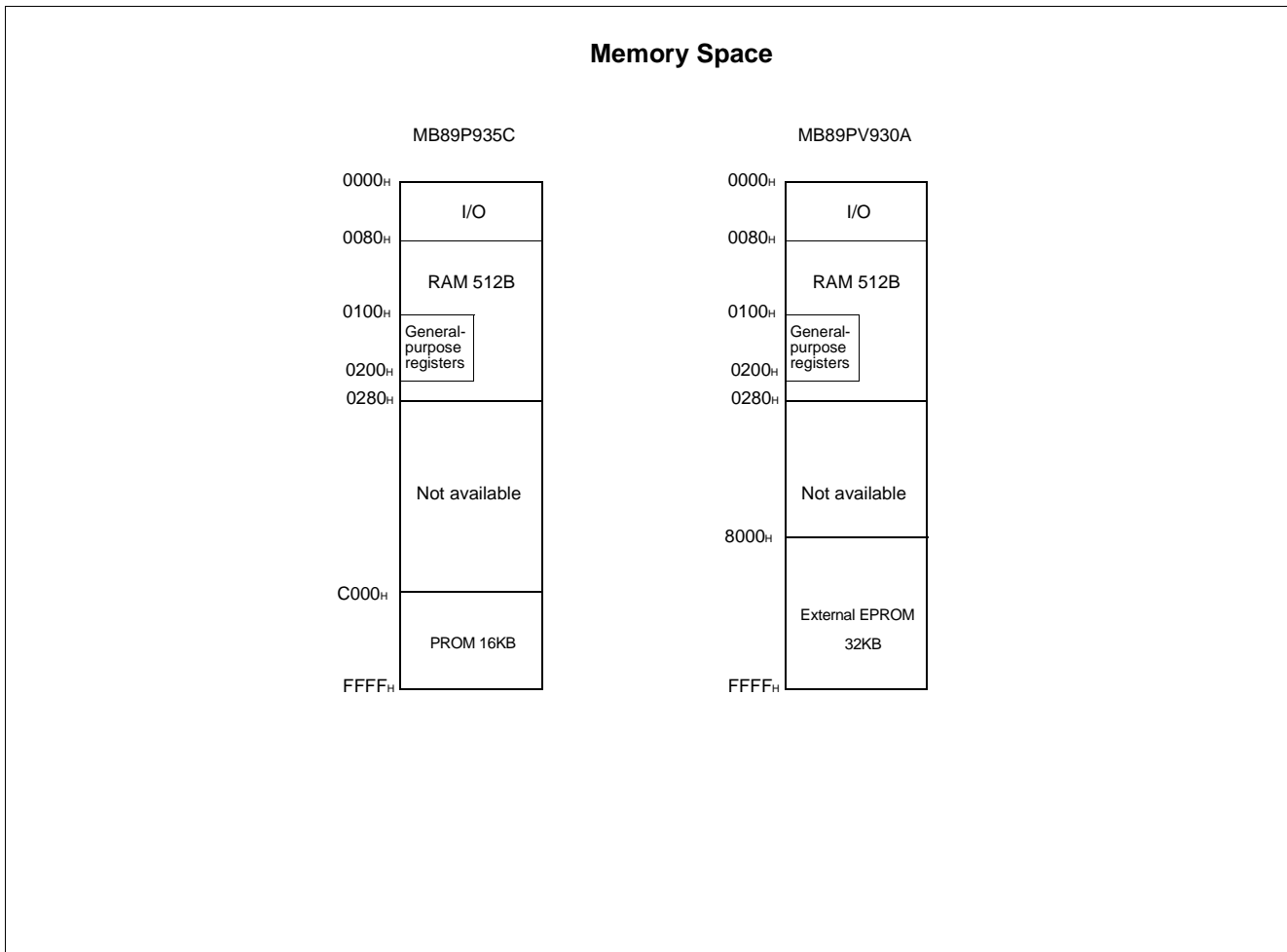


# MB89930C Series

## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89930C series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89930C series is structured as illustrated below.

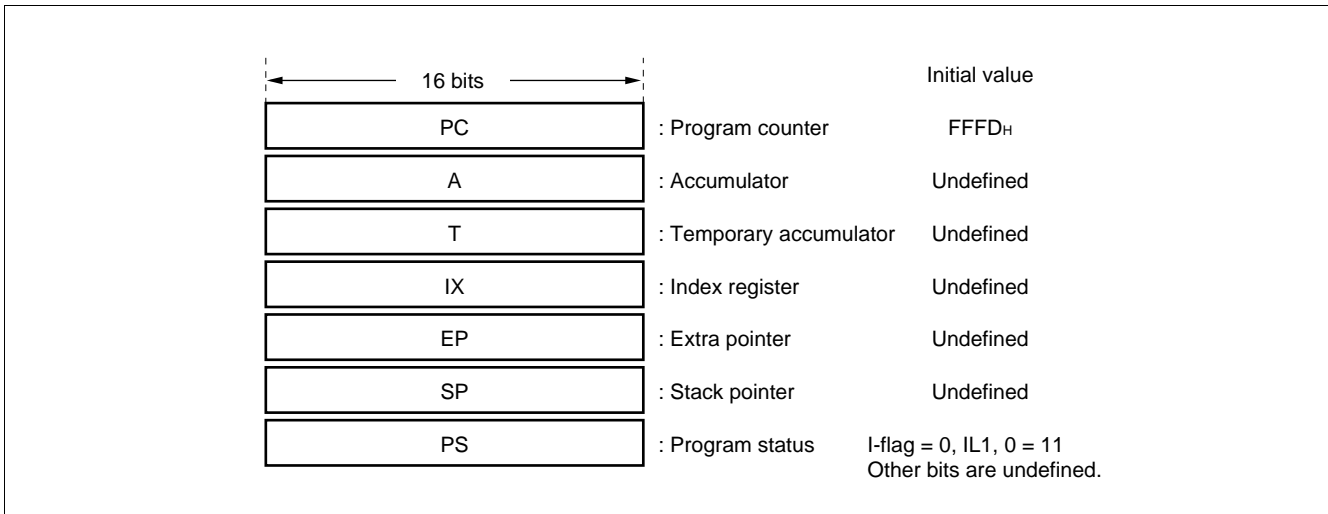




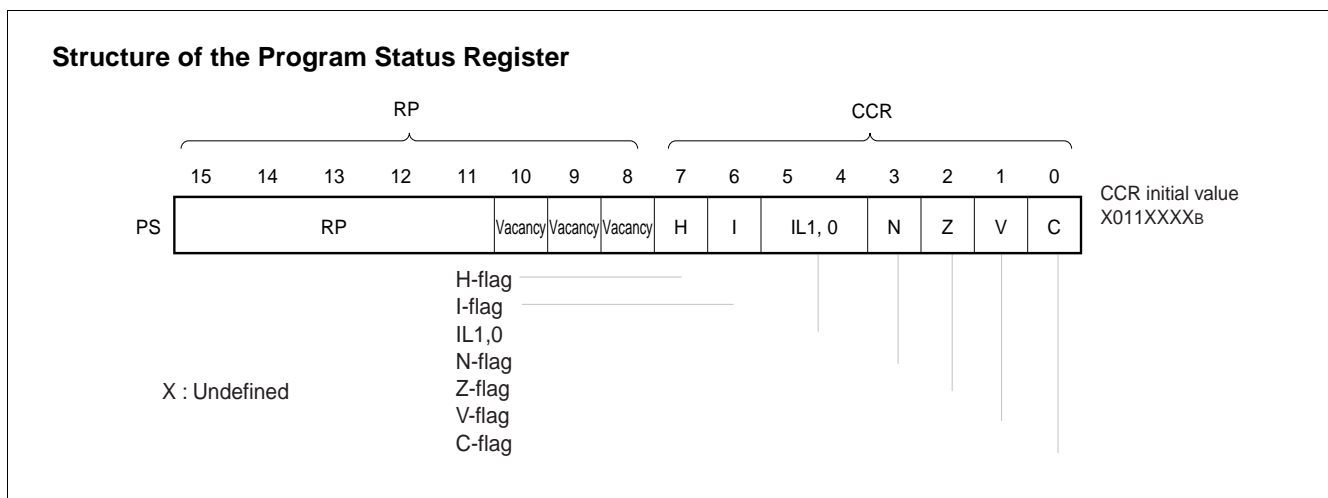
## 2. Registers

The F<sup>2</sup>MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

- Program counter (PC): A 16-bit register for indicating instruction storage positions
- Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX): A 16-bit register for index modification
- Extra pointer (EP): A 16-bit pointer for indicating a memory address
- Stack pointer (SP): A 16-bit register for indicating a stack area
- Program status (PS): A 16-bit register for storing a register pointer, a condition code



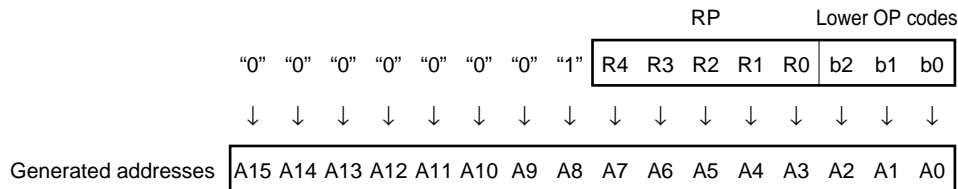
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



# MB89930C Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

## Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

**H-flag:** Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

**I-flag:** Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

**IL1, 0:** Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	ILO	Interrupt level	High-low
0	0	1	High ↑ ↓ Low = no interrupt
0	1		
1	0	2	
1	1	3	

**N-flag:** Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

**Z-flag:** Set when an arithmetic operation results in 0. Cleared otherwise.

**V-flag:** Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

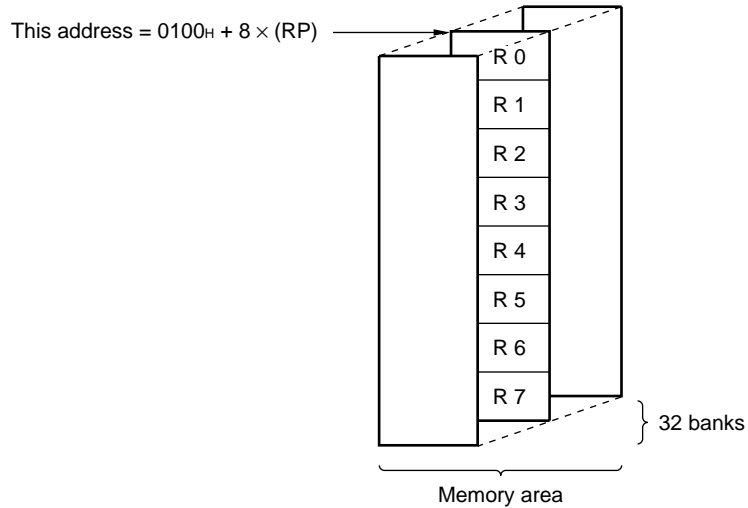
**C-flag:** Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89930C series. The bank currently in use is indicated by the register bank pointer (RP).

## Register Bank Configuration



# MB89930C Series

## ■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00 <sub>H</sub>	PDR0	Port 0 data register	R/W	XXXXXXXX <sub>B</sub>
01 <sub>H</sub>	DDR0	Port 0 data direction register	W	0000000 <sub>B</sub>
02 <sub>H</sub> to 06 <sub>H</sub>	(Reserved)			
07 <sub>H</sub>	SYCC	System clock control register	R/W	1--11100 <sub>B</sub>
08 <sub>H</sub>	STBC	Standby control register	R/W	00010--- <sub>B</sub>
09 <sub>H</sub>	WDC	Watchdog timer control register	W	0---XXXX <sub>B</sub>
0A <sub>H</sub>	TBTC	Timebase timer control register	R/W	00---000 <sub>B</sub>
0B <sub>H</sub>	(Reserved)			
0C <sub>H</sub>	PDR3	Port 3 data register	R/W	XXXXXXXX <sub>B</sub>
0D <sub>H</sub>	DDR3	Port 3 data direction register	W	0000000 <sub>B</sub>
0E <sub>H</sub>	RSFR	Reset flag register	R	XXXX---- <sub>B</sub>
0F <sub>H</sub>	PDR4	Port 4 data register	R/W	----XXXX <sub>B</sub>
10 <sub>H</sub>	DDR4	Port 4 direction register	R/W	----0000 <sub>B</sub>
11 <sub>H</sub>	OUT4	Port 4 output format register	R/W	----0000 <sub>B</sub>
12 <sub>H</sub>	PDR5	Port 5 data register	R/W	-----X <sub>B</sub>
13 <sub>H</sub>	DDR5	Port 5 data direction register	R/W	-----0 <sub>B</sub>
14 <sub>H</sub>	RCR21	12-bit PPG control register 1	R/W	0000000 <sub>B</sub>
15 <sub>H</sub>	RCR22	12-bit PPG control register 2	R/W	--000000 <sub>B</sub>
16 <sub>H</sub>	RCR23	12-bit PPG control register 3	R/W	0-000000 <sub>B</sub>
17 <sub>H</sub>	RCR24	12-bit PPG control register 4	R/W	--000000 <sub>B</sub>
18 <sub>H</sub>	BZCR	Buzzer register	R/W	-----000 <sub>B</sub>
19 <sub>H</sub>	TCCR	Capture control register	R/W	0000000 <sub>B</sub>
1A <sub>H</sub>	TCR1	Timer 1 control register	R/W	0000000 <sub>B</sub>
1B <sub>H</sub>	TCR0	Timer 0 control register	R/W	0000000 <sub>B</sub>
1C <sub>H</sub>	TDR1	Timer 1 data register	R/W	XXXXXXXX <sub>B</sub>
1D <sub>H</sub>	TDR0	Timer 0 data register	R/W	XXXXXXXX <sub>B</sub>
1E <sub>H</sub>	TCPH	Capture data register H	R	XXXXXXXX <sub>B</sub>
1F <sub>H</sub>	TCPL	Capture data register L	R	XXXXXXXX <sub>B</sub>
20 <sub>H</sub>	TCR2	Timer output control register	R/W	-----00 <sub>B</sub>
21 <sub>H</sub>	(Reserved)			
22 <sub>H</sub>	CNTR	PWM control register	R/W	0-000000 <sub>B</sub>
23 <sub>H</sub>	COMR	PWM compare register	W	XXXXXXXX <sub>B</sub>
24 <sub>H</sub>	EIC1	External interrupt 1 control register 1	R/W	0000000 <sub>B</sub>
25 <sub>H</sub>	EIC2	External interrupt 1 control register 2	R/W	----0000 <sub>B</sub>
26 <sub>H</sub>	(Reserved)			
27 <sub>H</sub>	(Reserved)			
28 <sub>H</sub>	SMC	Serial mode control register	R/W	00000-00 <sub>B</sub>
29 <sub>H</sub>	SRC	Serial rate control register	R/W	--011000 <sub>B</sub>
2A <sub>H</sub>	SSD	Serial status and data register	R/W	00100-1X <sub>B</sub>

(Continued)

# MB89930C Series

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
2B <sub>H</sub>	SIDR	Serial input data register	R	XXXXXXXX <sub>B</sub>
	SODR	Serial output data register	W	11111111 <sub>B</sub>
2C <sub>H</sub>	UPC	Clock division selection register	R/W	----0010 <sub>B</sub>
2D <sub>H</sub> to 2F <sub>H</sub>	(Reserved)			
30 <sub>H</sub>	ADC1	A/D converter control register 1	R/W	-0000000 <sub>B</sub>
31 <sub>H</sub>	ADC2	A/D converter control register 2	R/W	-0000001 <sub>B</sub>
32 <sub>H</sub>	ADDH	A/D converter data register H	R/W	-----XX <sub>B</sub>
33 <sub>H</sub>	ADDL	A/D converter data register L	R/W	XXXXXXXX <sub>B</sub>
34 <sub>H</sub>	ADEN	A/D enable register	R/W	00000000 <sub>B</sub>
35 <sub>H</sub>	(Reserved)			
36 <sub>H</sub>	EIE2	External interrupt 2 control register1	R/W	00000000 <sub>B</sub>
37 <sub>H</sub>	EIF2	External interrupt 2 control register 2	R/W	-----0 <sub>B</sub>
38 <sub>H</sub>	(Reserved)			
39 <sub>H</sub>	SMR	Serial mode register	R/W	00000000 <sub>B</sub>
3A <sub>H</sub>	SDR	Serial data register	R/W	XXXXXXXX <sub>B</sub>
3B <sub>H</sub>	SSEL	Serial function switching register	R/W	-----0 <sub>B</sub>
3C <sub>H</sub> to 3F <sub>H</sub>	(Reserved)			
40 <sub>H</sub>	WRARH1	Upper-address setting register 1	R/W	XXXXXXXX <sub>B</sub>
41 <sub>H</sub>	WRARL1	Lower-address setting register 1	R/W	XXXXXXXX <sub>B</sub>
42 <sub>H</sub>	WRDR1	Data setting register 1	R/W	XXXXXXXX <sub>B</sub>
43 <sub>H</sub>	WRARH2	Upper-address setting register 2	R/W	XXXXXXXX <sub>B</sub>
44 <sub>H</sub>	WRARL2	Lower-address setting register 2	R/W	XXXXXXXX <sub>B</sub>
45 <sub>H</sub>	WRDR2	Data setting register 2	R/W	XXXXXXXX <sub>B</sub>
46 <sub>H</sub>	WREN	Wild-register enable register	R/W	XXXXXX00 <sub>B</sub>
47 <sub>H</sub>	WROR	Wild-register data test register	R/W	-----00 <sub>B</sub>
48 to 6F <sub>H</sub>	(Reserved)			
70 <sub>H</sub>	PUL0	Port 0 pull-up setting register	R/W	00000000 <sub>B</sub>
71 <sub>H</sub>	PUL3	Port 3 pull-up setting register	R/W	00000000 <sub>B</sub>
72 <sub>H</sub>	PUL5	Port 5 pull up setting register	R/W	-----0 <sub>B</sub>
73 <sub>H</sub> to 7A <sub>H</sub>	(Reserved)			
7B <sub>H</sub>	ILR1	Interrupt level setting register 1	W	11111111 <sub>B</sub>
7C <sub>H</sub>	ILR2	Interrupt level setting register 2	W	11111111 <sub>B</sub>
7D <sub>H</sub>	ILR3	Interrupt level setting register 3	W	11111111 <sub>B</sub>
7E <sub>H</sub>	ILR4	Interrupt level setting register 4	W	11111111 <sub>B</sub>
7F <sub>H</sub>	ITR	Interrupt test register	Not available	-----00 <sub>B</sub>

- : Unused, X : Undefined

Note : Do not use reserved area.

# MB89930C Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	$V_{CC}$ $AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC}$ must not exceed $V_{CC}$
A/D converter reference input voltage	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	AVR must not exceed $AV_{CC}$
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{CC} + 6.0$	V	
“L” level maximum output current	$I_{OL1}$	—	20	mA	Pins P40 to P43
	$I_{OL2}$	—	10	mA	Pin excluding P40 to P43
“L” level average output current	$I_{OLAV}$	—	4	mA	Average value (operating current x operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“H” level maximum output current	$I_{OH}$	—	-10	mA	
“H” level average output current	$I_{OHAV}$	—	-2	mA	Average value (operating current x operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	-50	mA	
Power consumption	$P_D$	—	200	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

WARNING: Semiconductor device can be permanently damaged by application of stress (voltage, current, temperature etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

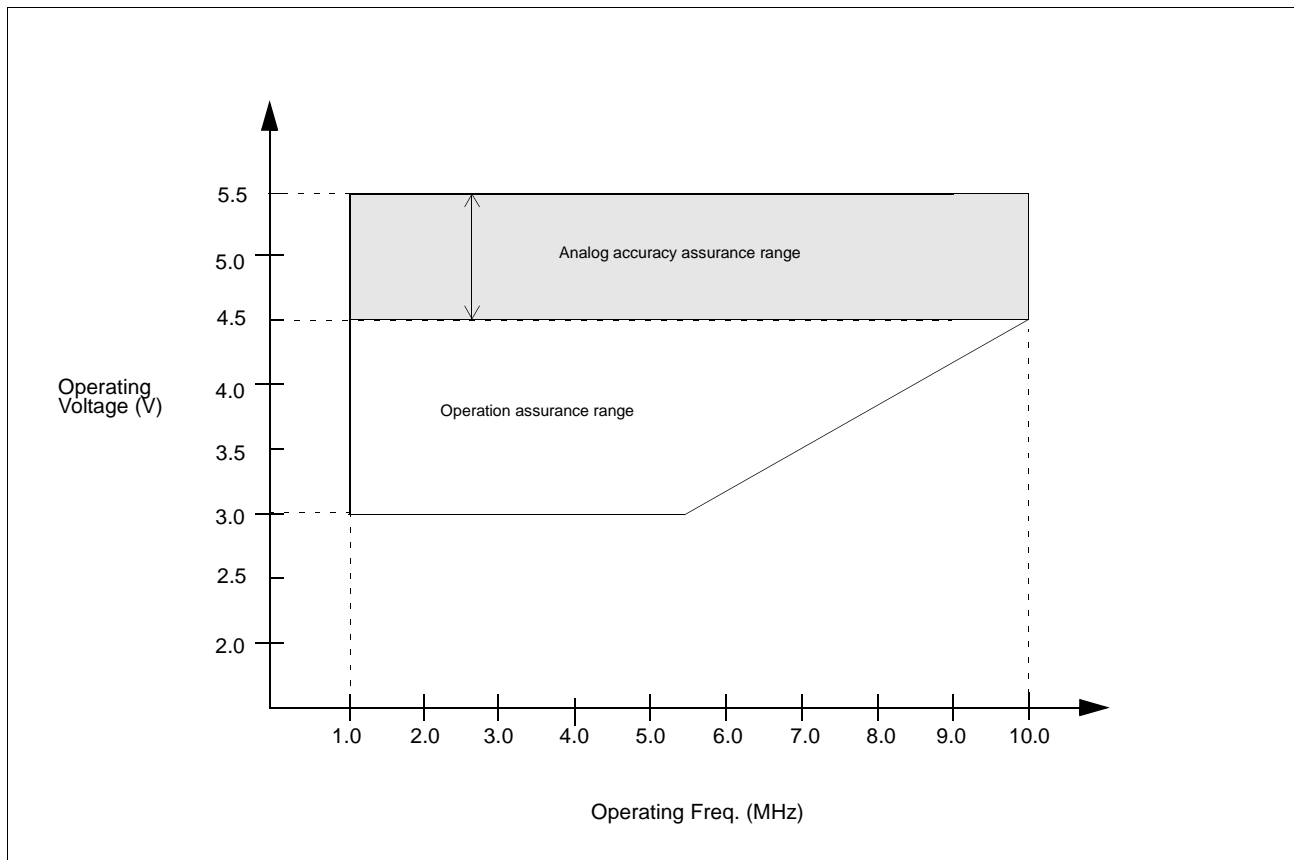
## 2. Recommended Operating Conditions

(AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V <sub>CC</sub>	3.0*	5.5	V	Operation assurance range
	AV <sub>CC</sub>	1.5	5.5	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	4.5	AV <sub>CC</sub>	V	
"H" level input voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V	P00 to P07, P30 to P37, P40 to P43, P50, UI/SI
	V <sub>IHS</sub>	0.8 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V	<u>MOD0/1</u> , <u>RST</u> , <u>EC</u> , <u>INT20</u> to <u>INT27</u> , <u>UCK/SCK</u> , <u>INT10</u> to <u>INT12</u>
"L" level input voltage	V <sub>IL</sub>	V <sub>SS</sub> - 0.3	0.3 V <sub>CC</sub>	V	P00 to P07, P30 to P37, P40 to P43, P50, UI/SI
	V <sub>ILS</sub>	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	V	<u>MOD0/1</u> , <u>RST</u> , <u>EC</u> , <u>INT20</u> to <u>INT27</u> , <u>UCK/SCK</u> , <u>INT10</u> to <u>INT12</u>
Open-drain output pin application voltage	V <sub>D</sub>	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3	V	P40 to P43
Operating temperature	T <sub>A</sub>	-40	+85	°C	

\*: This value depend on the operating conditions and the analog assurance range. See Figure 1 and "5. A/D converter Electrical Characteristics."

# MB89930C Series



**Figure 1 Operating Voltage vs. Operating Frequency**

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.



## 3. DC Characteristics

( $AV_{CC} = V_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $F_{CH} = 10\text{ MHz}$ (External clock),  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	$V_{IH}$	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50, UI/SI	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IHS}$	$\overline{RST}$ , MOD0/1, $\overline{UCK/SCK}$ , $\overline{EC}$ , INT20 ~ INT27, INT10 ~ INT12	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	$V_{IL}$	P00 ~ P07 P30 ~ P37, P40 ~ P43, P50, UI/SI	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	$V_{ILS}$	$\overline{RST}$ , MOD0/1, $\overline{UCK/SCK}$ , $\overline{EC}$ , INT20 ~ INT27, INT10 ~ INT12	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
Open-drain output pin application voltage	$V_D$	P40 ~ P43	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
“H” level output voltage	$V_{OH}$	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50	$I_{OH} = -4.0\text{ mA}$	2.4	—	—	V	
“L” level output voltage	$V_{OL1}$	P00 ~ P07, P30 ~ P37, P50, $\overline{RST}$	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P40 ~ P43	$I_{OL} = 12.0\text{ mA}$	—	—	0.4	V	
Input leakage current	$I_{LI}$	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50, MOD0/1	$0.45\text{ V} < V_I < V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$	Without pull-up resistor
Pull-up resistance	$R_{PULL}$	P00 ~ P07, P30 ~ P37, P40 ~ P43, P50	$V_I = 0.0\text{ V}$	25	50	100	$\text{k}\Omega$	
Power supply current	$I_{CC}$	$V_{CC}$ (External clock operation)	$F_{CH} = 10.0\text{ MHz}$ $T_{inst} = 0.4\mu\text{s}$ Main clock run mode	—	6	9	$\text{mA}$	
	$I_{CCS}$		$F_{CH} = 10.0\text{ MHz}$ $T_{inst} = 0.4\mu\text{s}$ Main clock sleep mode	—	3	5	$\text{mA}$	
	$I_{CCH}$		Stop mode $T_A = +25^\circ\text{C}$	—	—	10	$\mu\text{A}$	
	$I_A$		When A/D converting	—	2.3	6	$\text{mA}$	
	$I_{AH}$	$AV_{CC}$	When A/D stops $T_A = +25^\circ\text{C}$	—	—	5	$\mu\text{A}$	
Input capacitance	$C_{IN}$	Other than $AV_{CC}$ , $AV_{SS}$ , AVR, $V_{CC}$ , $V_{SS}$	—	—	10	—	$\text{pF}$	

# MB89930C Series

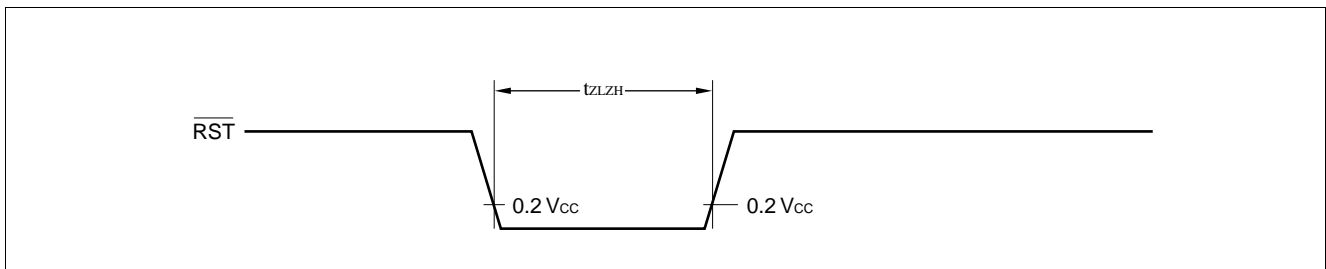
## 4. AC Characteristics

### (1) Reset Timing

( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{\text{RST}}$ "L" pulse width	$t_{\text{ZLZH}}$	—	48 $t_{\text{HCYL}}^*$	—	ns	

\* :  $t_{\text{HCYL}}$  is the oscillation cycle ( $1/F_c$ ) to input to the X0 pin.

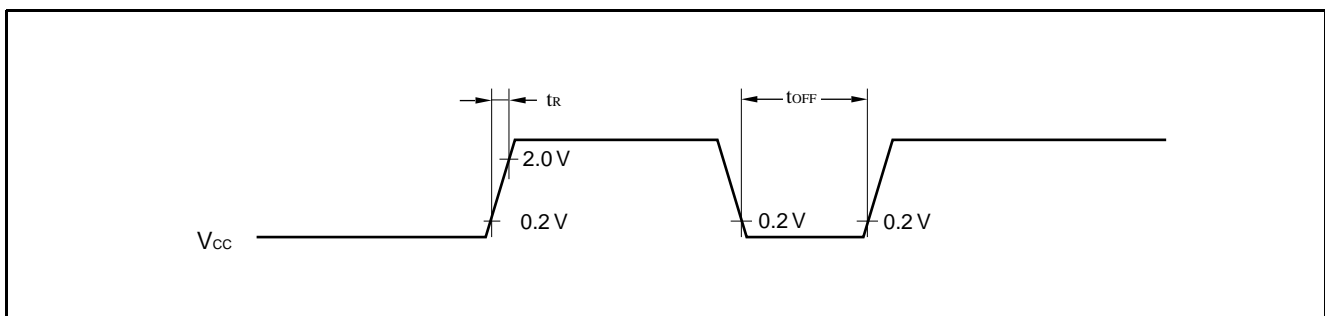


Note: The MCU operation is not guaranteed when the "L" pulse width is shorter than  $t_{\text{ZLZH}}$ .

### (2) Power-on Reset

( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	$t_{\text{r}}$	—	—	50	ms	
Power supply cut-off time	$t_{\text{OFF}}$	—	1	—	ms	Due to repeated operations



Note: The supply voltage must be set to the minimum value required for operation within the prescribed default oscillation setting time.

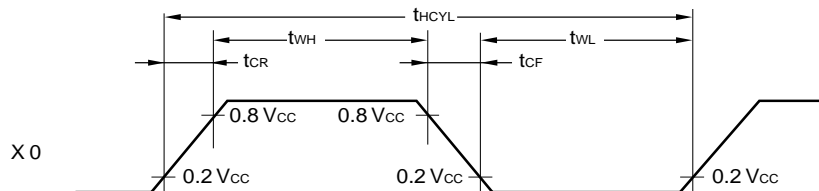
# MB89930C Series

## (3) Clock Timing

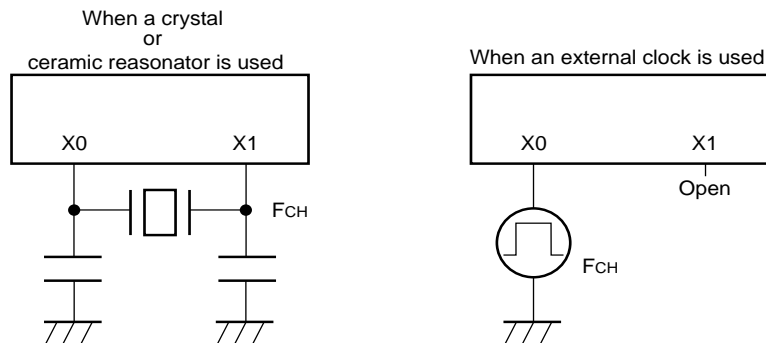
( $V_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Clock frequency	$F_{CH}$	—	1	10	MHz	
Clock cycle time	$t_{HCL}$		100	1000	ns	
Input clock pulse width	$t_{WH}$ $t_{WL}$		20	—	ns	
Input clock rising/falling time	$t_{CR}$ $t_{CF}$		—	10	ns	

### X0 and X1 Timing and Conditions



### Main Clock Conditions



## (4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	$t_{inst}$	$4/F_{CH}$ , $8/F_{CH}$ , $16/F_{CH}$ , $64/F_{CH}$	$\mu\text{s}$	$t_{inst} = 0.4\ \mu\text{s}$ when operating at $F_{CH} = 10\ \text{MHz}$ ( $4/F_{CH}$ )

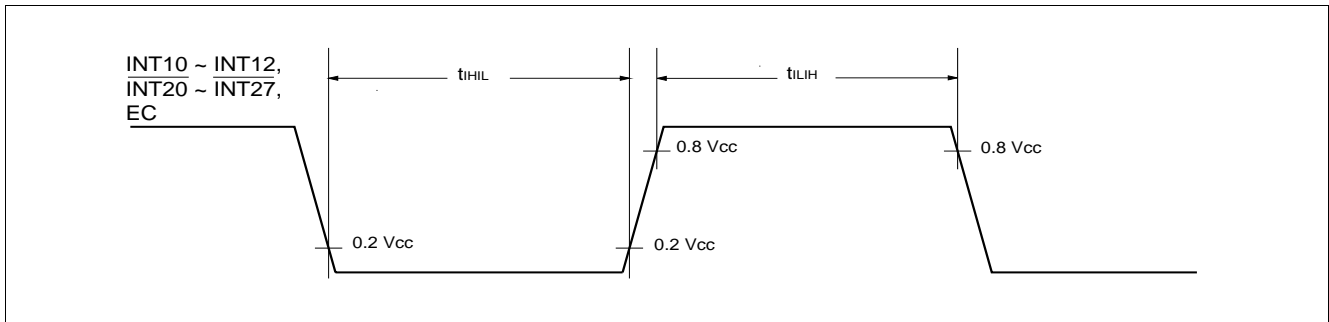
# MB89930C Series

## (5) Peripheral Input Timing

( $A_{V_{CC}} = V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input "H" pulse width	$t_{LIH}$	INT10 ~ INT12, INT20 ~ INT27, EC	$2 t_{inst}^*$	—	$\mu\text{s}$	
Peripheral input "L" pulse width	$t_{LIL}$	INT10 ~ INT12, INT20 ~ INT27, EC	$2 t_{inst}^*$	—	$\mu\text{s}$	

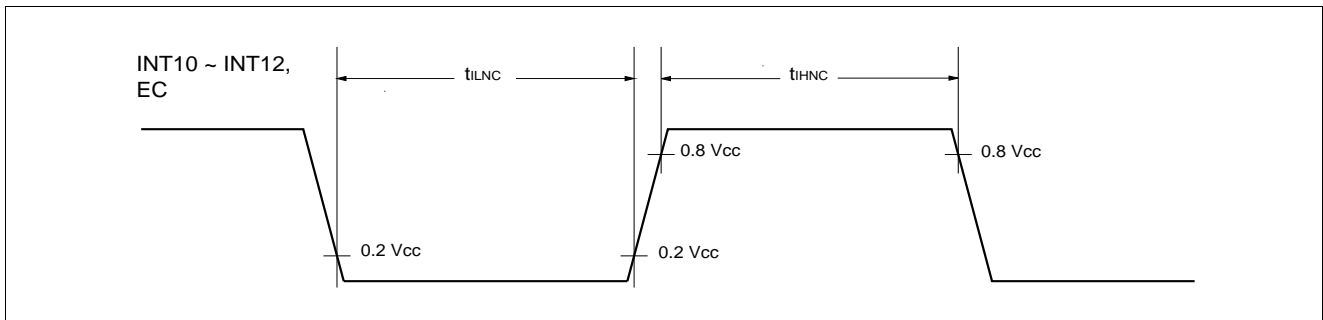
\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."



( $A_{V_{CC}} = V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input "H" noise limit	$t_{IHNC}$	INT10 to INT12, EC	7	15	23	ns	
Peripheral input "L" noise limit	$t_{ILNC}$	INT10 to INT12, EC	7	15	23	ns	

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."

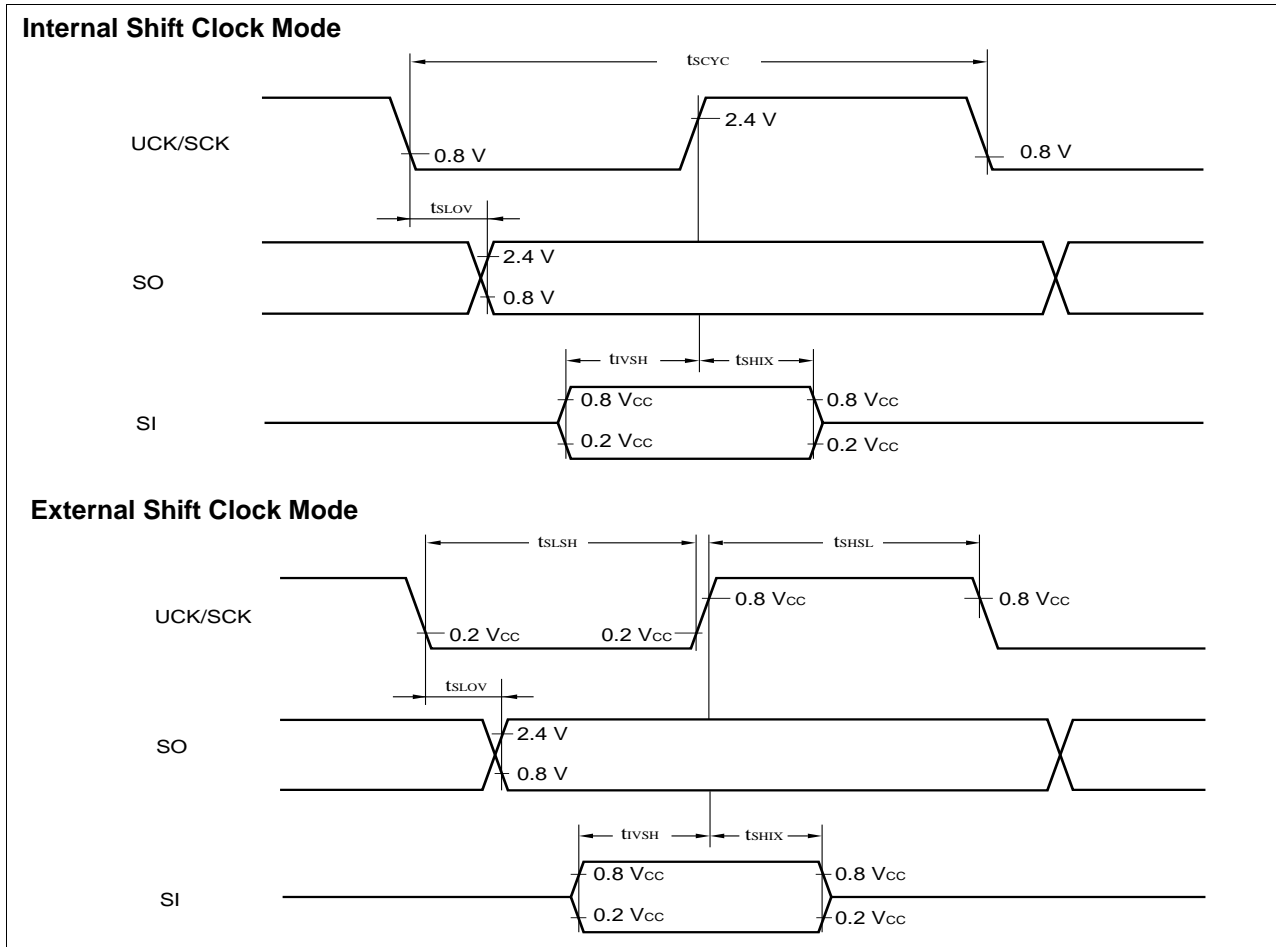


## (6) UART, Serial I/O Timing

( $V_{CC} = V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
Serial clock cycle time	$t_{SCYC}$	UCK/SCK	Internal shift clock mode	$2 t_{inst}^*$	—	$\mu\text{s}$
UCK/SCK $\downarrow \rightarrow$ SO time	$t_{SLOV}$	UCK/SCK, SO		-200	200	ns
Valid SI $\rightarrow$ UCK/SCK $\uparrow$	$t_{IVSH}$	UCK/SCK, SI		$1/2 t_{inst}^*$	—	$\mu\text{s}$
UCK/SCK $\uparrow \rightarrow$ valid SI hold time	$t_{SHIX}$	UCK/SCK, SI		$1/2 t_{inst}^*$	—	$\mu\text{s}$
Serial clock "H" pulse width	$t_{SHSL}$	UCK/SCK	External shift clock mode	$1 t_{inst}^*$	—	$\mu\text{s}$
Serial clock "L" pulse width	$t_{LSLH}$	UCK/SCK		$1 t_{inst}^*$	—	$\mu\text{s}$
UCK/SCK $\downarrow \rightarrow$ SO time	$t_{SLOV}$	UCK/SCK, SO		0	200	ns
Valid SI $\rightarrow$ UCK/SCK $\uparrow$	$t_{IVSH}$	UCK/SCK, SI		$1/2 t_{inst}^*$	—	$\mu\text{s}$
UCK/SCK $\uparrow \rightarrow$ valid SI hold time	$t_{SHIX}$	UCK/SCK, SI	$1/2 t_{inst}^*$	—	$\mu\text{s}$	

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."



# MB89930C Series

## 5. A/D Converter Electrical Characteristics

### (1) A/D Converter Electrical Characteristics

$AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution			—	10	—	bit	
Total error	—	—	—	—	$\pm 3.0$	LSB	MB89P935C
					$\pm 5.0$		MB89PV930A
Linearity error	—	—	—	—	$\pm 2.5$	LSB	MB89P935C
					$\pm 3.0$		MB89PV930A
Differential linearity error	—	—	—	—	$\pm 1.9$	LSB	MB89P935C
					$\pm 2.5$		MB89PV930A
Zero transition voltage	$V_{OT}$	—	$AV_{SS} - 1.5\text{ LSB}$	$AV_{SS} + 0.5\text{ LSB}$	$AV_{SS} + 2.5\text{ LSB}$	LSB	MB89P935C
			$AV_{SS} - 3.5\text{ LSB}$	$AV_{SS} + 0.5\text{ LSB}$	$AV_{SS} + 4.5\text{ LSB}$		MB89PV930A
Full-scale transition voltage	$V_{FST}$	—	$AVR - 3.5\text{ LSB}$	$AVR - 1.5\text{ LSB}$	$AVR + 0.5\text{ LSB}$	LSB	MB89P935C
			$AVR - 6.5\text{ LSB}$	$AVR - 1.5\text{ LSB}$	$AVR + 2.0\text{ LSB}$		MB89PV930A
A/D mode conversion time			—	—	$38\ t_{inst}^*$	$\mu\text{s}$	
Analog port input current	$I_{AIN}$	AN0 to AN7	—	—	10	$\mu\text{A}$	
Analog input voltage	$V_{AIN}$	AN0 to AN7	$AV_{SS}$	—	AVR	V	
Reference voltage	—	—	$AV_{SS} + 3.0$	—	$AV_{CC}$	V	
Reference voltage supply current	$I_R$	AVR	—	140	260	$\mu\text{A}$	At A/D start
	$I_{RH}$	AVR	—	—	5	$\mu\text{A}$	At A/D stop

\* For information on  $t_{inst}$ , see "(4) Instruction Cycle" in "4. AC Characteristics."

### (2) A/D Converter Glossary

- Resolution

Analog changes that are identifiable with the A/D converter

When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .

- Linearity error (unit: LSB)

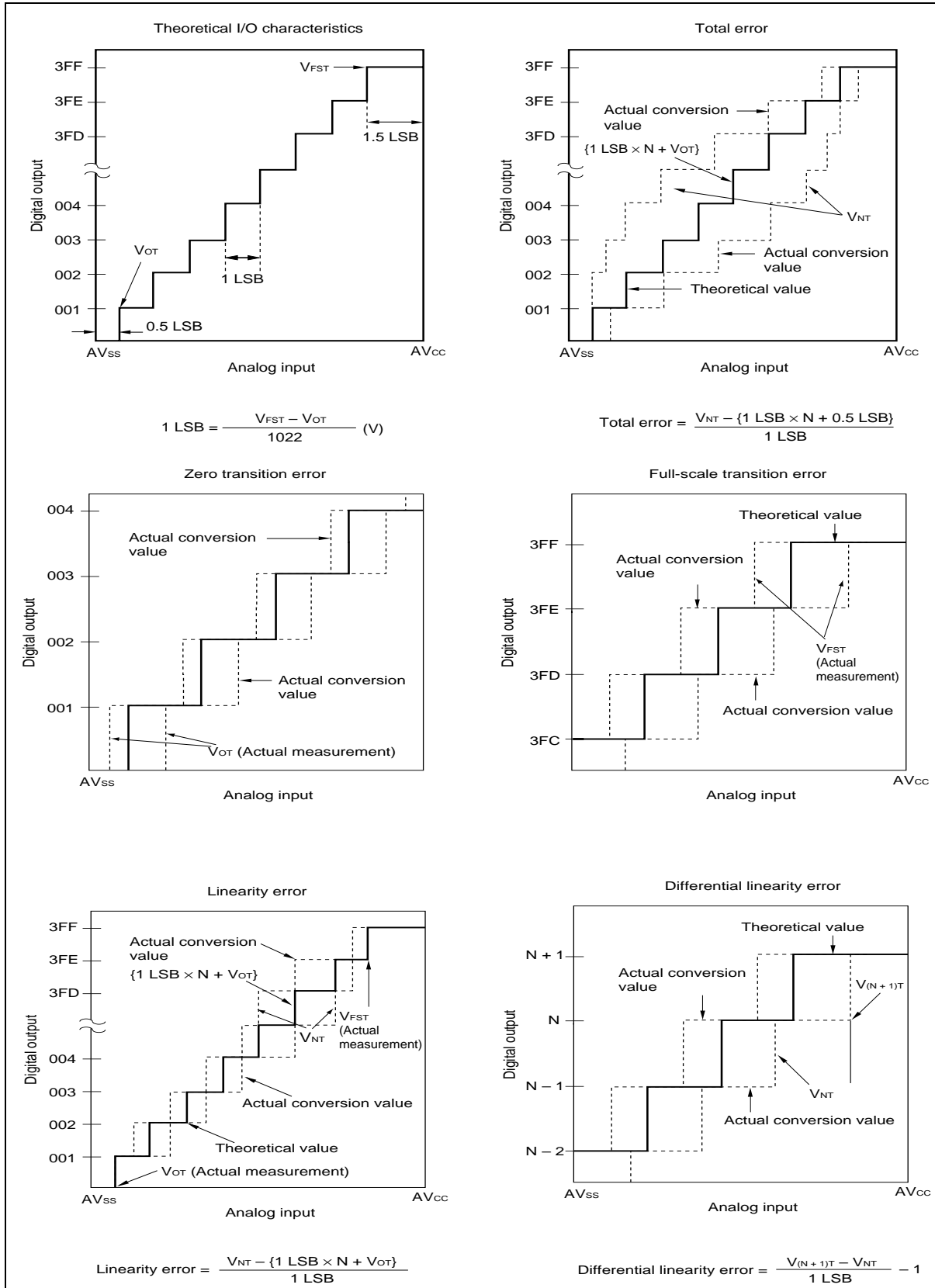
The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1111" ↔ "11 1111 1110") from actual conversion characteristics.

- Differential linearity error (unit: LSB)

The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.

- Total error (unit: LSB)

The difference between theoretical and actual conversion values.



# MB89930C Series

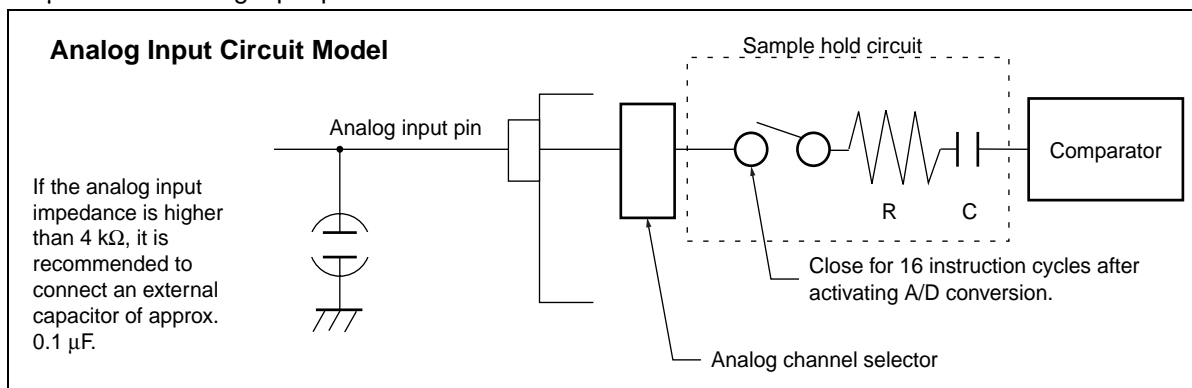
## (3) Notes on Using A/D Converter

- Input impedance of the analog input pins

The A/D converter used for the MB89930C series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for 16 instruction cycles after activation A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below  $4k\Omega$ ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about  $0.1\ \mu\text{F}$  for the analog input pin.



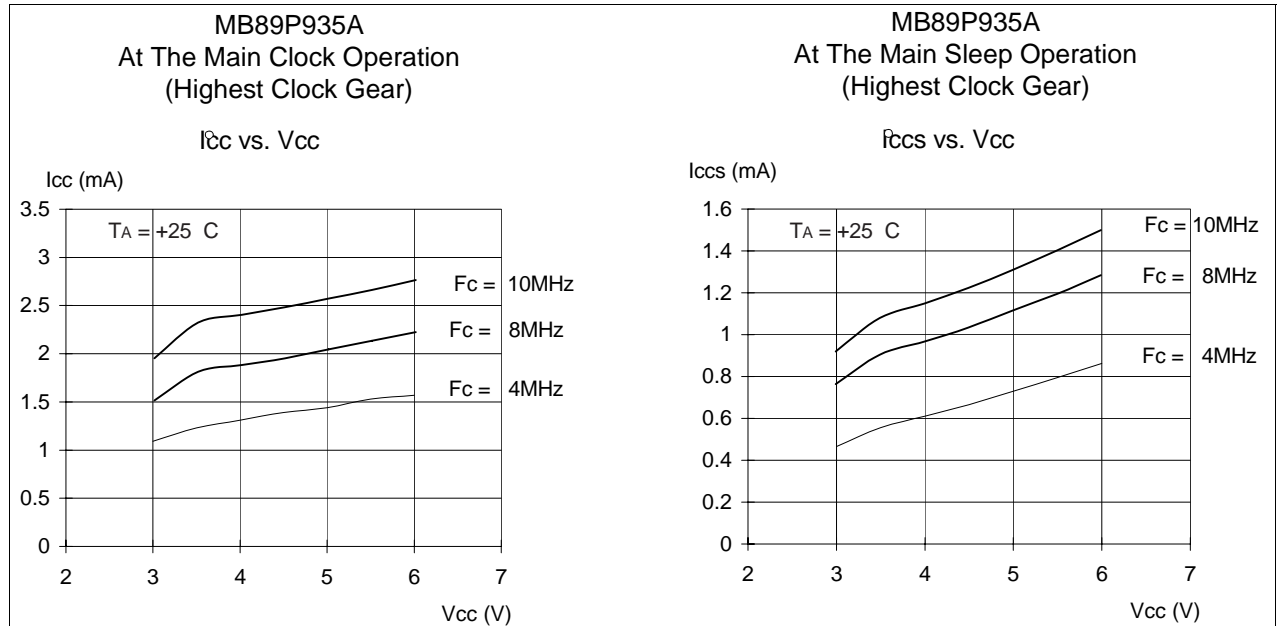
- Error

The smaller the  $|AVR - AV_{SS}|$ , the greater the error would become relatively.



## ■ EXAMPLE CHARACTERISTICS

- Power Supply Current (External Clock)



# MB89930C Series

## ■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

**Table 1 Instruction Symbols**

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
( × )	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(( × ))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- “–” indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

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Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
MOV dir,A	3	2	(dir) ← (A)	-	-	-	----	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	-	-	-	----	46
MOV ext,A	4	3	(ext) ← (A)	-	-	-	----	61
MOV @EP,A	3	1	((EP)) ← (A)	-	-	-	----	47
MOV Ri,A	3	1	(Ri) ← (A)	-	-	-	----	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	-	-	++--	04
MOV A,dir	3	2	(A) ← (dir)	AL	-	-	++--	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	-	-	++--	06
MOV A,ext	4	3	(A) ← (ext)	AL	-	-	++--	60
MOV A,@A	3	1	(A) ← ((A))	AL	-	-	++--	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	-	-	++--	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	-	-	++--	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	-	-	-	----	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	-	-	-	----	86
MOV @EP,#d8	4	2	((EP)) ← d8	-	-	-	----	87
MOV Ri,#d8	4	2	(Ri) ← d8	-	-	-	----	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	-	-	-	----	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	-	-	-	----	D6
MOVW ext,A	5	3	(ext) ← (AH),(ext + 1) ← (AL)	-	-	-	----	D4
MOVW @EP,A	4	1	((EP)) ← (AH),(EP + 1) ← (AL)	-	-	-	----	D7
MOVW EP,A	2	1	(EP) ← (A)	-	-	-	----	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	++--	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	++--	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	++--	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	++--	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A) + 1)	AL	AH	dH	++--	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	++--	C7
MOVW A,EP	2	1	(A) ← (EP)	-	-	dH	----	F3
MOVW EP,#d16	3	3	(EP) ← d16	-	-	-	----	E7
MOVW IX,A	2	1	(IX) ← (A)	-	-	-	----	E2
MOVW A,IX	2	1	(A) ← (IX)	-	-	dH	----	F2
MOVW SP,A	2	1	(SP) ← (A)	-	-	-	----	E1
MOVW A,SP	2	1	(A) ← (SP)	-	-	dH	----	F1
MOV @A,T	3	1	((A)) ← (T)	-	-	-	----	82
MOVW @A,T	4	1	((A)) ← (TH),(A) + 1 ← (TL)	-	-	-	----	83
MOVW IX,#d16	3	3	(IX) ← d16	-	-	-	----	E6
MOVW A,PS	2	1	(A) ← (PS)	-	-	dH	----	70
MOVW PS,A	2	1	(PS) ← (A)	-	-	-	++++	71
MOVW SP,#d16	3	3	(SP) ← d16	-	-	-	----	E5
SWAP	2	1	(AH) ↔ (AL)	-	-	AL	----	10
SETB dir: b	4	2	(dir): b ← 1	-	-	-	----	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	-	-	-	----	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	-	-	----	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	----	43
XCHW A,EP	3	1	(A) ↔ (EP)	-	-	dH	----	F7
XCHW A,IX	3	1	(A) ↔ (IX)	-	-	dH	----	F6
XCHW A,SP	3	1	(A) ↔ (SP)	-	-	dH	----	F5
MOVW A,PC	2	1	(A) ← (PC)	-	-	dH	----	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.

- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F<sup>2</sup>MC-8 family)

**Table 3 Arithmetic Operation Instructions (62 instructions)**

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
ADDC A,Ri	3	1	$(A) \leftarrow (A) + (Ri) + C$	-	-	-	++++	28 to 2F
ADDC A,#d8	2	2	$(A) \leftarrow (A) + d8 + C$	-	-	-	++++	24
ADDC A,dir	3	2	$(A) \leftarrow (A) + (dir) + C$	-	-	-	++++	25
ADDC A,@IX +off	4	2	$(A) \leftarrow (A) + ((IX) + off) + C$	-	-	-	++++	26
ADDC A,@EP	3	1	$(A) \leftarrow (A) + ((EP)) + C$	-	-	-	++++	27
ADDCW A	3	1	$(A) \leftarrow (A) + (T) + C$	-	-	dH	++++	23
ADDC A	2	1	$(AL) \leftarrow (AL) + (TL) + C$	-	-	-	++++	22
SUBC A,Ri	3	1	$(A) \leftarrow (A) - (Ri) - C$	-	-	-	++++	38 to 3F
SUBC A,#d8	2	2	$(A) \leftarrow (A) - d8 - C$	-	-	-	++++	34
SUBC A,dir	3	2	$(A) \leftarrow (A) - (dir) - C$	-	-	-	++++	35
SUBC A,@IX +off	4	2	$(A) \leftarrow (A) - ((IX) + off) - C$	-	-	-	++++	36
SUBC A,@EP	3	1	$(A) \leftarrow (A) - ((EP)) - C$	-	-	-	++++	37
SUBCW A	3	1	$(A) \leftarrow (T) - (A) - C$	-	-	dH	++++	33
SUBC A	2	1	$(AL) \leftarrow (TL) - (AL) - C$	-	-	-	++++	32
INC Ri	4	1	$(Ri) \leftarrow (Ri) + 1$	-	-	-	+++-	C8 to CF
INCW EP	3	1	$(EP) \leftarrow (EP) + 1$	-	-	-	----	C3
INCW IX	3	1	$(IX) \leftarrow (IX) + 1$	-	-	-	----	C2
INCW A	3	1	$(A) \leftarrow (A) + 1$	-	-	dH	+- - -	C0
DEC Ri	4	1	$(Ri) \leftarrow (Ri) - 1$	-	-	-	+++-	D8 to DF
DECW EP	3	1	$(EP) \leftarrow (EP) - 1$	-	-	-	----	D3
DECW IX	3	1	$(IX) \leftarrow (IX) - 1$	-	-	-	----	D2
DECW A	3	1	$(A) \leftarrow (A) - 1$	-	-	dH	+- - -	D0
MULU A	19	1	$(A) \leftarrow (AL) \times (TL)$	-	-	dH	----	01
DIVU A	21	1	$(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$	dL	00	00	----	11
ANDW A	3	1	$(A) \leftarrow (A) \wedge (T)$	-	-	dH	++ R -	63
ORW A	3	1	$(A) \leftarrow (A) \vee (T)$	-	-	dH	++ R -	73
XORW A	3	1	$(A) \leftarrow (A) \nabla (T)$	-	-	dH	++ R -	53
CMP A	2	1	$(TL) - (AL)$	-	-	-	++++	12
CMPW A	3	1	$(T) - (A)$	-	-	-	++++	13
RORC A	2	1	$\boxed{\rightarrow C \rightarrow A}$	-	-	-	++ - +	03
ROLC A	2	1	$\boxed{C \leftarrow A}$	-	-	-	++ - +	02
CMP A,#d8	2	2	$(A) - d8$	-	-	-	++++	14
CMP A,dir	3	2	$(A) - (dir)$	-	-	-	++++	15
CMP A,@EP	3	1	$(A) - ((EP))$	-	-	-	++++	17
CMP A,@IX +off	4	2	$(A) - ((IX) + off)$	-	-	-	++++	16
CMP A,Ri	3	1	$(A) - (Ri)$	-	-	-	++++	18 to 1F
DAA	2	1	Decimal adjust for addition	-	-	-	++++	84
DAS	2	1	Decimal adjust for subtraction	-	-	-	++++	94
XOR A	2	1	$(A) \leftarrow (AL) \nabla (TL)$	-	-	-	++ R -	52
XOR A,#d8	2	2	$(A) \leftarrow (AL) \nabla d8$	-	-	-	++ R -	54
XOR A,dir	3	2	$(A) \leftarrow (AL) \nabla (dir)$	-	-	-	++ R -	55
XOR A,@EP	3	1	$(A) \leftarrow (AL) \nabla ((EP))$	-	-	-	++ R -	57
XOR A,@IX +off	4	2	$(A) \leftarrow (AL) \nabla ((IX) + off)$	-	-	-	++ R -	56
XOR A,Ri	3	1	$(A) \leftarrow (AL) \nabla (Ri)$	-	-	-	++ R -	58 to 5F
AND A	2	1	$(A) \leftarrow (AL) \wedge (TL)$	-	-	-	++ R -	62
AND A,#d8	2	2	$(A) \leftarrow (AL) \wedge d8$	-	-	-	++ R -	64
AND A,dir	3	2	$(A) \leftarrow (AL) \wedge (dir)$	-	-	-	++ R -	65

(Continued)

# MB89930C Series

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
AND A,@EP	3	1	$(A) \leftarrow (AL) \wedge ((EP))$	-	-	-	++R-	67
AND A,@IX +off	4	2	$(A) \leftarrow (AL) \wedge ((IX) +off)$	-	-	-	++R-	66
AND A,Ri	3	1	$(A) \leftarrow (AL) \wedge (Ri)$	-	-	-	++R-	68 to 6F
OR A	2	1	$(A) \leftarrow (AL) \vee (TL)$	-	-	-	++R-	72
OR A,#d8	2	2	$(A) \leftarrow (AL) \vee d8$	-	-	-	++R-	74
OR A,dir	3	2	$(A) \leftarrow (AL) \vee (dir)$	-	-	-	++R-	75
OR A,@EP	3	1	$(A) \leftarrow (AL) \vee ((EP))$	-	-	-	++R-	77
OR A,@IX +off	4	2	$(A) \leftarrow (AL) \vee ((IX) +off)$	-	-	-	++R-	76
OR A,Ri	3	1	$(A) \leftarrow (AL) \vee (Ri)$	-	-	-	++R-	78 to 7F
CMP dir,#d8	5	3	$(dir) - d8$	-	-	-	++++	95
CMP @EP,#d8	4	2	$((EP)) - d8$	-	-	-	++++	97
CMP @IX +off,#d8	5	3	$((IX) +off) - d8$	-	-	-	++++	96
CMP Ri,#d8	4	2	$(Ri) - d8$	-	-	-	++++	98 to 9F
INCW SP	3	1	$(SP) \leftarrow (SP) + 1$	-	-	-	----	C1
DECW SP	3	1	$(SP) \leftarrow (SP) - 1$	-	-	-	----	D1

Table 1

Table 1 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
BZ/BEQ rel	3	2	If $Z = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FD
BNZ/BNE rel	3	2	If $Z = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FC
BC/BLO rel	3	2	If $C = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	F9
BNC/BHS rel	3	2	If $C = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	F8
BN rel	3	2	If $N = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FB
BP rel	3	2	If $N = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FA
BLT rel	3	2	If $V \vee N = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FF
BGE rel	3	2	If $V \vee N = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FE
BBC dir: b,rel	5	3	If $(dir: b) = 0$ then $PC \leftarrow PC + rel$	-	-	-	-+---	B0 to B7
BBS dir: b,rel	5	3	If $(dir: b) = 1$ then $PC \leftarrow PC + rel$	-	-	-	-+---	B8 to BF
JMP @A	2	1	$(PC) \leftarrow (A)$	-	-	-	----	E0
JMP ext	3	3	$(PC) \leftarrow ext$	-	-	-	----	21
CALLV #vct	6	1	Vector call	-	-	-	----	E8 to EF
CALL ext	6	3	Subroutine call	-	-	-	----	31
XCHW A,PC	3	1	$(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$	-	-	dH	----	F4
RET	4	1	Return from subroutine	-	-	-	----	20
RETI	6	1	Return from interrupt	-	-	-	Restore	30

Table 1

Table 1 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
PUSHW A	4	1		-	-	-	----	40
POPW A	4	1		-	-	dH	----	50
PUSHW IX	4	1		-	-	-	----	41
POPW IX	4	1		-	-	-	----	51
NOP	1	1		-	-	-	----	00
CLRC	1	1		-	-	-	----R	81
SETC	1	1		-	-	-	----S	91
CLRI	1	1		-	-	-	----	80
SETI	1	1		-	-	-	----	90

## INSTRUCTION MAP

L/H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SPA	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EPA	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8	/	XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EPA	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EPA	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

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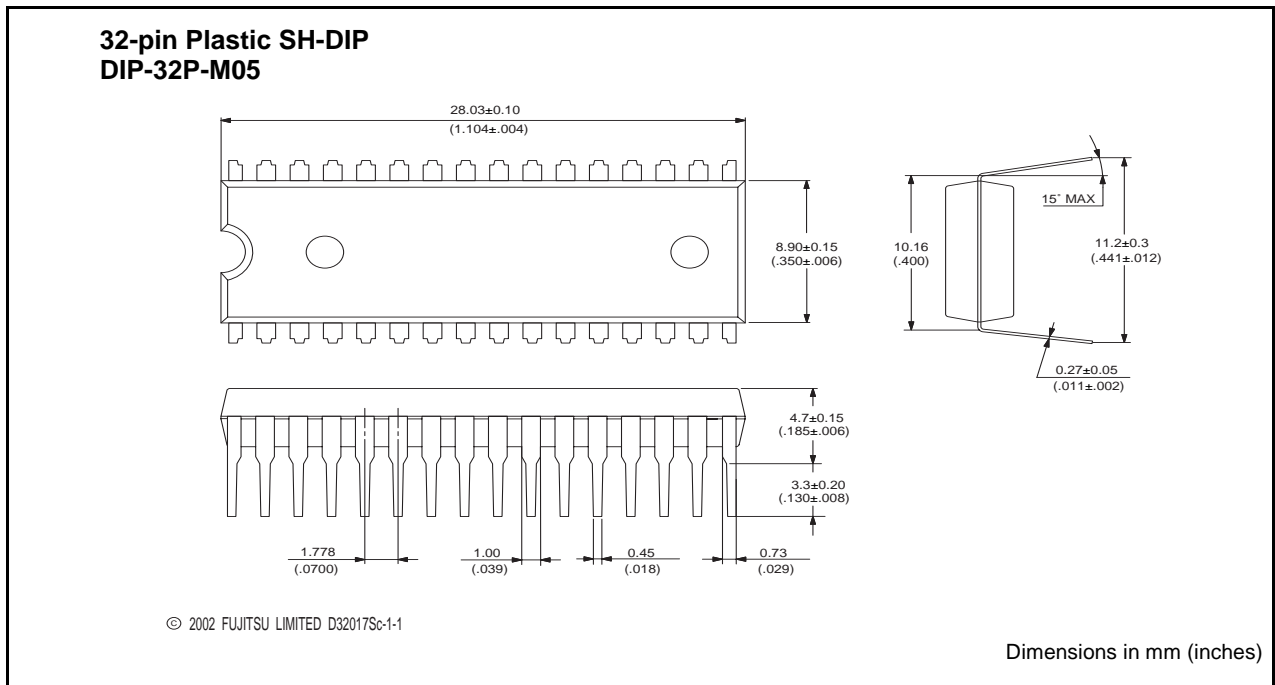
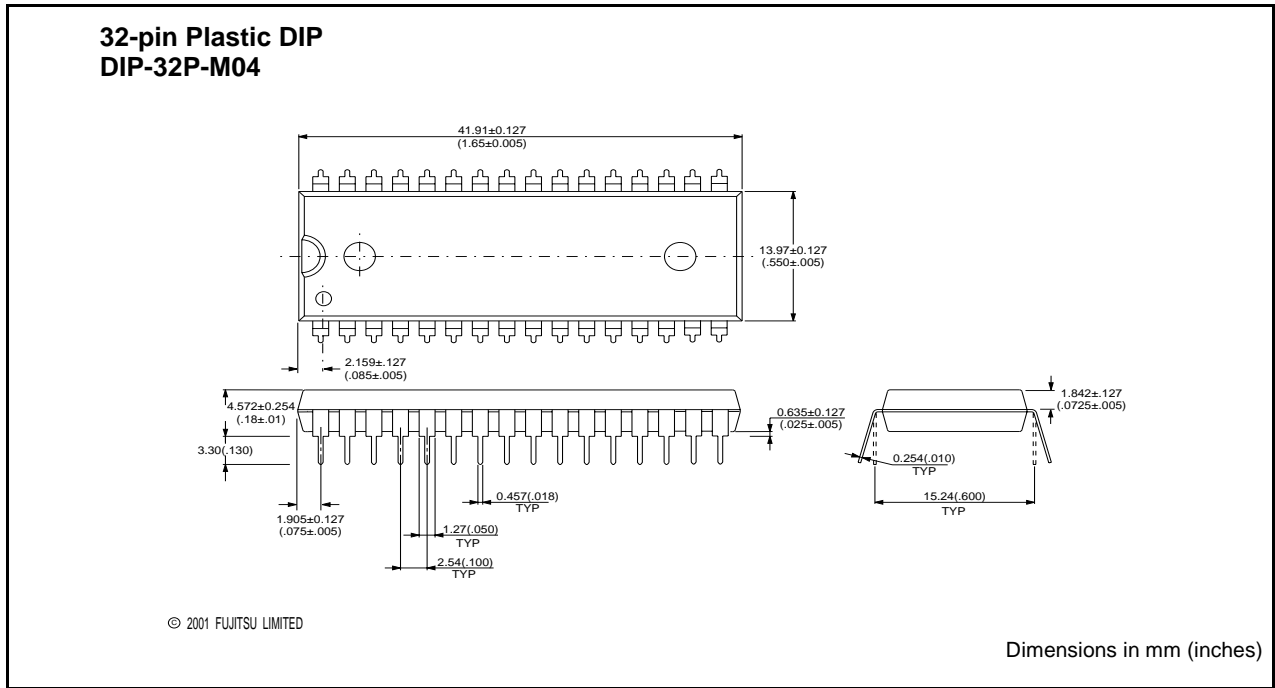
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## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB89P935CP	32-pin Plastic DIP (DIP-32P-M04)	
MB89P935CP-G-SH	32-pin Plastic SH-DIP (DIP-32P-M05)	
MB89PV930ACF	48-pin Ceramic MQFP (MQP-48C-P01)	

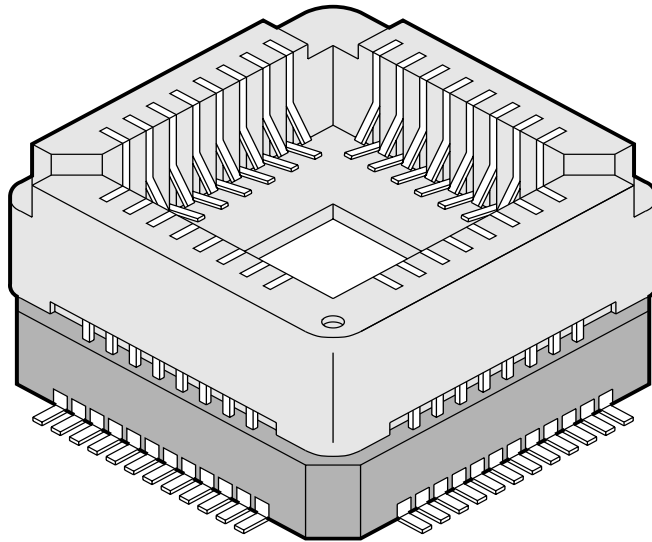


## ■ PACKAGE DIMENSIONS



# MB89930C Series

48-pin Ceramic MQFP  
MQP-48C-P01



(MQP-48C-P01)

Dimensions in mm (inches)

**MEMO**



# MB89930C Series

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