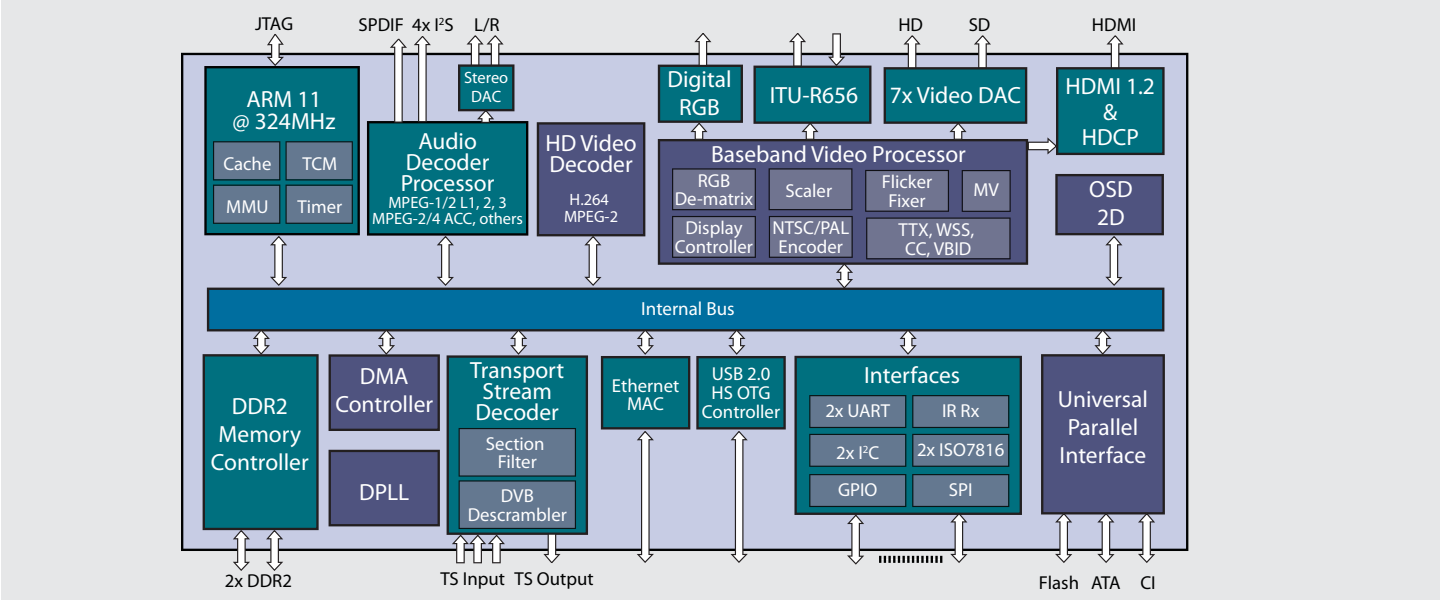
MB86H60 HD Multi-Standard Decoder



Description

The MB86H60 is a highly integrated System-on-Chip incorporating all the processing functions required by digital/HDTV receivers — including those for digital video, audio and graphics — making the chip ideal for HDTV sets and set-top boxes.

The MB86H60 incorporates the high-performance ARM® processor 1176JZF-S™ featuring an integrated memory management unit (MMU), a floating point co-processor, ARM's Jazelle® technology and Thumb® instruction set extensions for compact code. The ARM11 provides all the processing power needed to enable a whole host of middleware software. Just two 16-bit DDR2 memories are required for operation.

This cost-effective, low-power, high-definition media processor is able to decode both MPEG-2 and H.264/AVC compressed video up to HD resolution (1920 x 1080i). HD video can be provided either via the copy-protected HDMI output or analog component outputs.

Simultaneously, the video signal can be scaled down and offered in standard definition (SD) resolution. The picture quality on these SD component outputs can be optimized by using cross-color and cross-luminance filters. A digital RGB output and an ITU-R 656 input and output are also available.

The integrated audio processor can decode a wide variety of audio standards required by the broadcast market such as MPEG-1/2 Layers 1, 2, 3 and MPEG-2/4 AAC. Support for Dolby® Digital (AC-3) and Dolby Digital Plus is planned. Four I^2S, SPDIF and stereo-analog outputs are available.

Advanced connectivity is provided by a USB 2.0 high speed On-The-Go (OTG) controller, a 10/100 Base-T Ethernet MAC and a DMA ATA controller. Integrated peripherals include two serial ports, two ISO7816 smart card interfaces, two I2C controllers, LED and keypad controller, IR receiver, SPI output, PWM output and 96 GPIO pins. The number of usable GPIOs depends on the system configuration since they are shared among other IO functions.

Features

- Decodes up to HD H.264 High Profile Level 4.0 and HD MPEG-2 Main Profile / High Level (MP@HL)
- Supports current and next-generation European broadcasting standards
- Single-chip integration of all functions necessary for HDTV processing
- The CPU core, the ARM1176JZF-S, supports system control for TVs and set-top boxes, teletext, subtitles, and JPEG decoding.
- Ease-of-use facilitated by integrating the processing of audio, graphics, video and HD broadcast functions
- Two 16-bit-wide DDR2-SDRAMs complete functionality and reduce total cost
- Four video-transfer ports for connectivity to various devices

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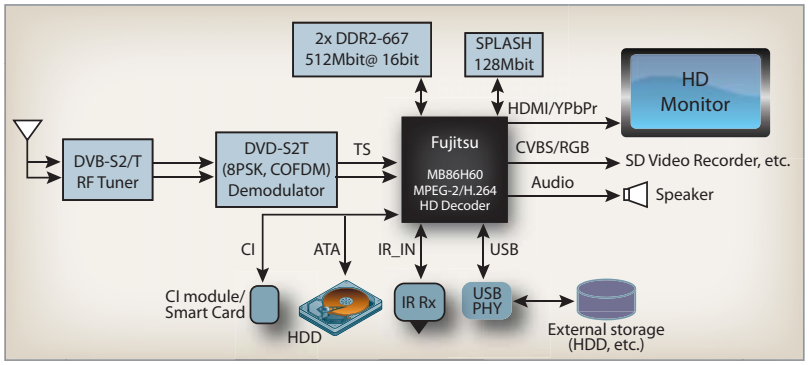
Applications

- Digital Cable/Satellite/Terrestrial Set-Top Boxes
- Integrated Digital TV (IDTV) Solutions
- HDTV Receivers



Sample Set-Top Box with HDD System Configuration

Specifications

CPU Core		ARM1176JZF-STM[1] CPU @ 324MHz with 16K-I/16K-D cache, 16K-I/16K-D TCM, FPU, MMU; bootable from NOR or serial flash
Video	*Spec*	H.264 HD high-profile / Level 4.0 Decoder and MPEG-2 HD/SD main profile / high-level decoder
	Resolution	1920 x 1080 x 60i/50i, 1440 x 1080 x 60i/50i,1280 x 720 x 60p/50p, 720 x 480 x 60i, 720 x 576 x 50i
	Video Encoder	Supports PAL/NTSC/SECAM; 3x DAC for HD output (YPbPr) and 4x DAC for SD video output; supports Teletext/WSS/PDC/CC/VBID
	Interface	Digital RGB888 output (HD) and ITU-R 656 I/O (SD)
Audio	*Format*	Programmable audio processor, audio firmware available or planned for MPEG-1/2 Layers 1, 2, and 3 (MP3), MPEG-2/4 AAC and MPEG-4 HE-AAC, Dolby® Digital and Dolby® Digital Plus
	Channels	5.1 channels
	Interface	4x I2S, SPDIF output, stereo audio DACs
TS Processing	*Format*	MPEG-2 TS standard
	Interface	4x transport streams (3x inputs, 1x output) and DVB descrambler
	Security	3DES encryption/decryption hardware acceleration
DDR2 Memory Interface		2 x 16-bit-width DDR2-SDRAM interface @ 324MHz
Display		Display controller supports 5 planes: video, 2x OSD (YCbCr or RGB), cursor, background; cross color and luminance filters
USB		USB 2.0 high-speed OTG Link controller
Ethernet		10/100 Base-T MAC
HDMI		HDMI 1.2 Link and PHY with HDCP
UPI		NOR flash, common interface, and ATA (multiword DMA @16MB/s)
Peripherals		2x UART, 2x ISO7816 smart card, 2x I2C, PWM, IR Rx, SPI output, serial flash, 96 shared GPIOs
Clock Frequency		Input: 27MHz; internal: 324MHz; DDR2 Interface: 324MHz; internal clock recovery (no external VCXO required)
Operating Clock Frequency		Internal: 324MHz, DDR2 memory interface: 324MHz
Power Consumption		1.2W (typ.)
Process		Fujitsu CMOS 90nm technology
Packaging		484-pin PBGA, 27mm x 27mm

[1]ARM1176JZF-S is a trademark, and ARM, Jazelle and Thumb are registered trademarks of ARM Limited.
[2]Dolby is a registered trademark of Dolby Laboratories.

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