

Spread Spectrum Clock Generator

MB88151

■ DESCRIPTION

MB88151 is a clock generator for EMI reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates frequency in modulation off as Middle Centered and down spread which modulates so as not to exceed frequency in modulation off.

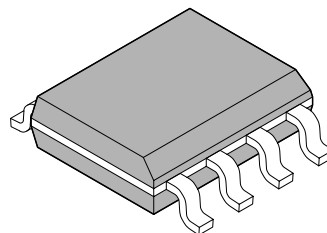
■ FEATURES

- Input frequency: 16.6 MHz to 33.4 MHz
- Multiplication rate: 1/2, 1, 2, 4
- Output frequency : 8.3 MHz to 16.7 MHz, 16.6 MHz to 33.4 MHz, 33.3 MHz to 66.7 MHz, 66.6 MHz to 133.4 MHz
- Modulation rate : $\pm 0.5\%$, $\pm 1.5\%$ (Center spread), $- 1.0\%$, $- 3.0\%$ (Down spread)
- Equipped with oscillation circuit : Range of oscillation 16.6 MHz to 33.4 MHz
- Modulation clock output Duty : 40% to 60%

(Continued)

■ PACKAGE

8-pin plastic SOP



(FPT-8P-M02)

MB88151

(Continued)

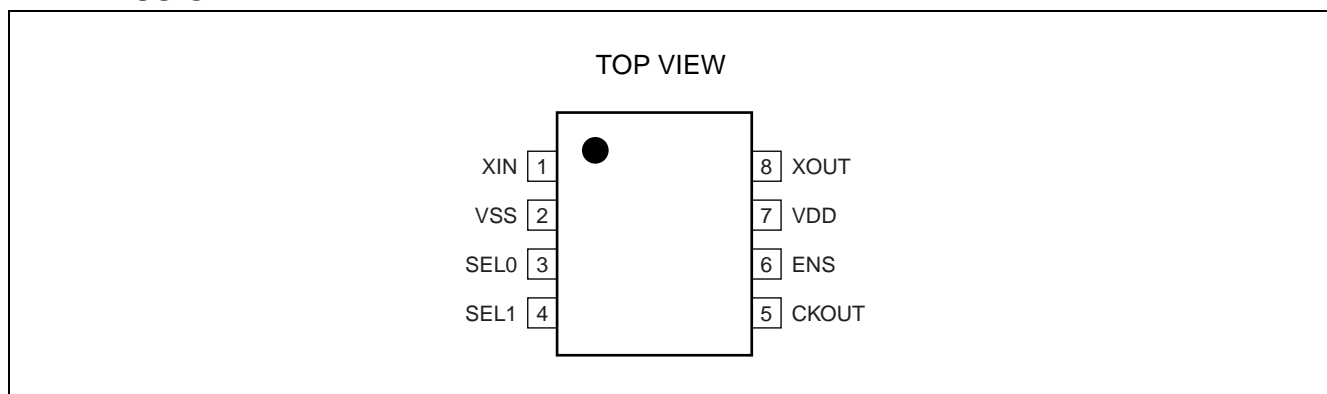
- Modulation clock
Cycle-Cycle Jitter
MB88151-100, 200 : Less than 100 ps,
MB88151-400 : Less than 150 ps,
MB88151-500 : Less than 200 ps
- Low current consumption by CMOS process: 5 mA@24 MHz (Typ-sample, no load)
- Power supply voltage : 3.3 V±0.3 V
- Operating temperature : – 40 °C to + 85 °C
- Package : SOP 8 pin

■ PRODUCT LINEUP

MB88151 has four kinds of multiplication type .

Product	Function
MB88151-100	Multiplied by 1, Output frequency range from 16.6 MHz to 33.4 MHz
MB88151-200	Multiplied by 2, Output frequency range from 33.3 MHz to 66.7 MHz
MB88151-400	Multiplied by 4, Output frequency range from 66.6 MHz to 133.4 MHz
MB88151-500	Multiplied by 1/2, Output frequency range from 8.3 MHz to 16.7 MHz

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
XIN	I	1	Resonator connection pin/clock input pin
VSS	—	2	GND pin
SEL0	I	3	Modulation rate setting pin
SEL1	I	4	Modulation rate setting pin
CKOUT	O	5	Modulated clock output pin
ENS	I	6	Modulation enable setting pin (with Pull-up Resistance)
VDD	—	7	Power supply voltage pin
XOUT	O	8	Resonator connection pin

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
SEL0 SEL1		<ul style="list-style-type: none"> • CMOS hysteresis input
ENS		<ul style="list-style-type: none"> • CMOS hysteresis input with pull-up resistor (50 kΩ)
CKOUT		<ul style="list-style-type: none"> • CMOS output • $I_{OL} = 4 \text{ mA}$

Note : For XIN and XOUT pins, see “■ OSCILLATION CIRCUIT”.

■ HANDLING DEVICES

Preventing Latchup

A latchup can occur if, on a CMOS IC, a voltage higher than VDD or a voltage lower than VSS is applied to an input or output pin or a voltage higher than the rating is applied between VDD and VSS. A latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

The attention when the external clock is used

Input the clock to XIN, and don't connect anything with XOUT if you use the external clock. And please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN.

Power supply pins

Please consider connecting the power supply terminal of this device by as lower impedance as possible from the current supply source.

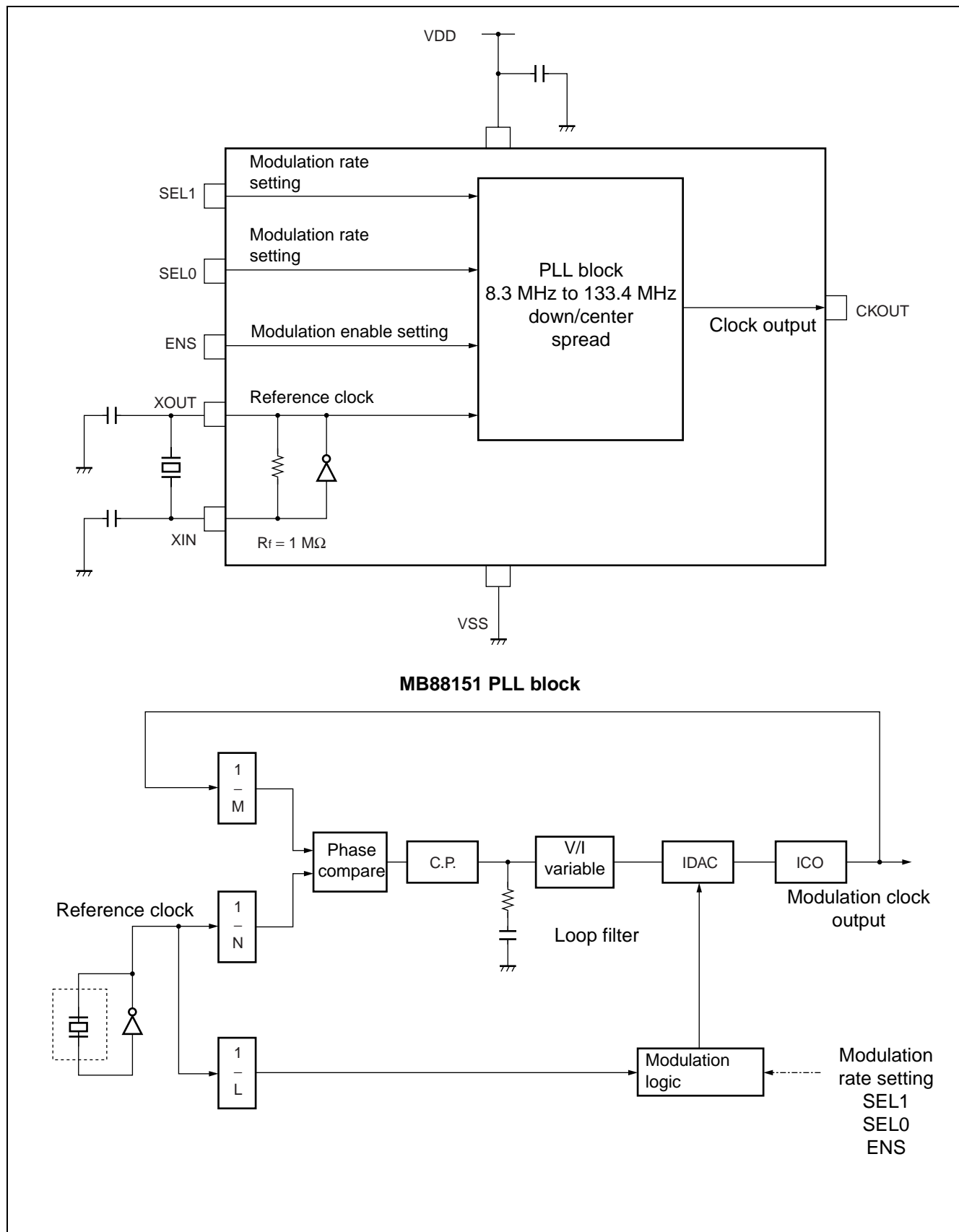
We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between VSS and VDD near the device, as a by-pass capacitor.

Oscillator Circuit

Noise near the XIN or Xout pin may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN and XOUT and resonator don't intersect other wiring.

It is strongly recommended that printed circuit board artwork that surrounds the XIN and XOUT pins with ground be used to increase the expectation of stable operation.

■ BLOCK DIAGRAM



■ PIN SETTING

When changing the pin setting, the stabilization wait time for the modulation clock is required. The stabilization wait time for the modulation clock take the maximum value of "■ ELECTRICAL CHARACTERISTICS Lock-Up time".

ENS modulation enable setting

ENS	Modulation
L	Modulation disable
H	Modulation enable

Note : Spectrum does not spread when "L" is set to ENS. The clock with low jitter can be obtained. Because of ENS has Pull-up resistance, spectrum spread when "H" is set to it or open the terminal.

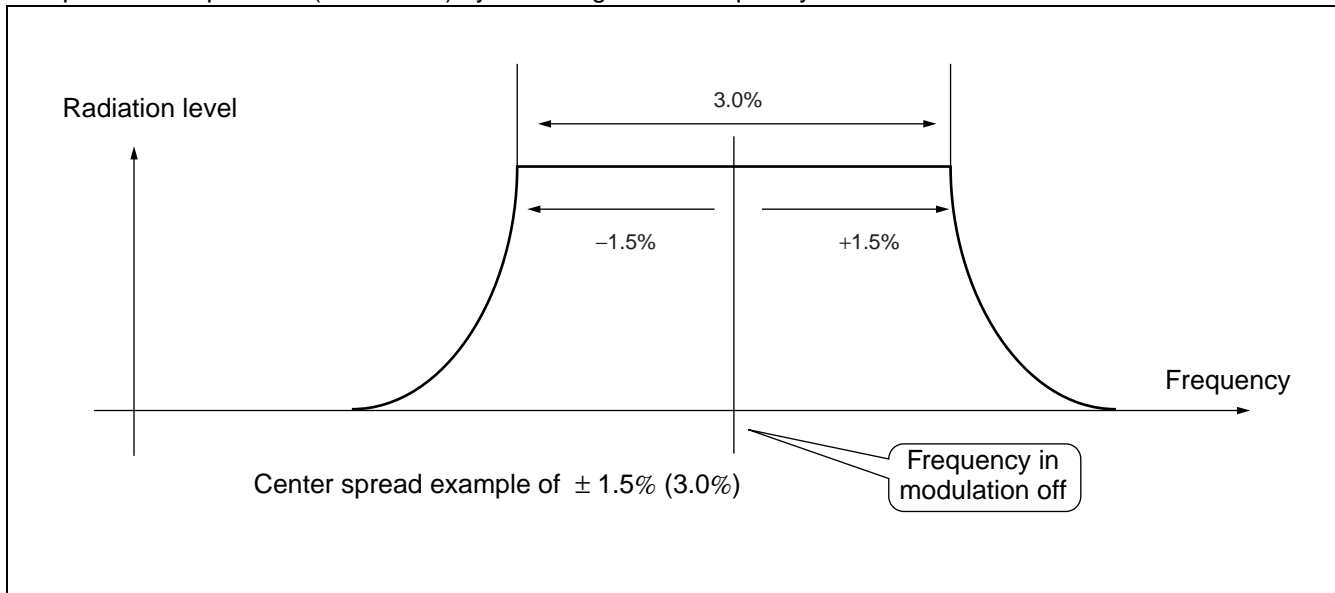
SEL0, SEL1 Modulation rate setting

SEL1	SEL0	Modulation rate	Modulation type
L	L	$\pm 1.5\%$	Center spread
L	H	$\pm 0.5\%$	Center spread
H	L	$- 1.0\%$	Down spread
H	H	$- 3.0\%$	Down spread

Note : The modulation rate can be changed at the level of the terminal.

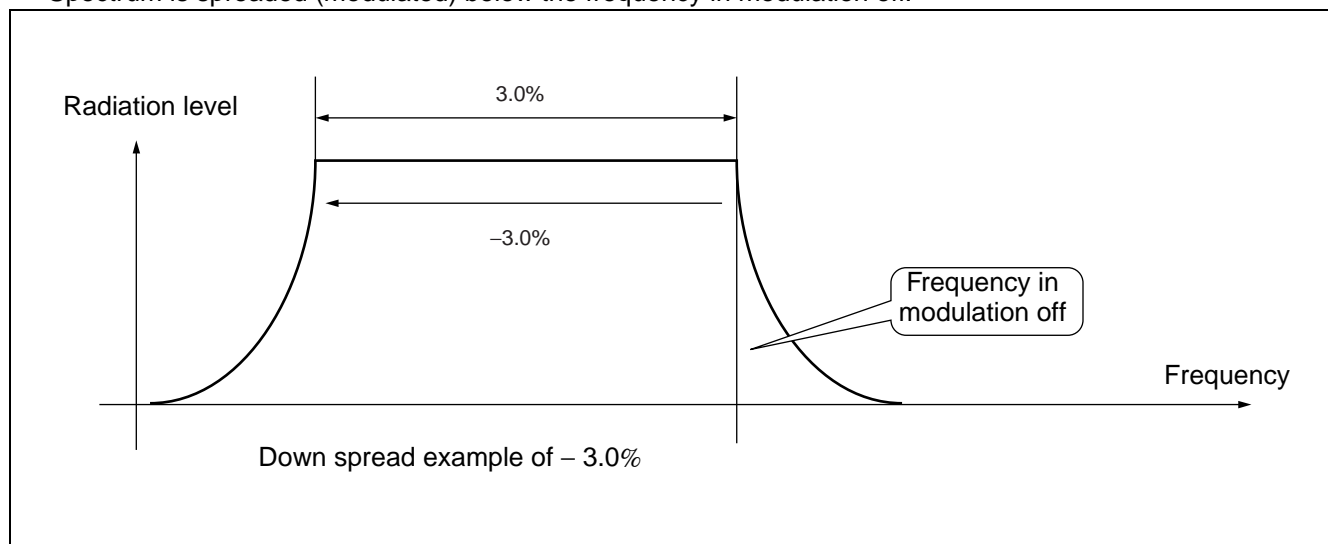
- Center spread

Spectrum is spreaded (modulated) by centering on the frequency in modulation off.



- Down spread

Spectrum is spreaded (modulated) below the frequency in modulation off.



■ ABSOLUTE MAXIMUM RATINGS

(VSS = 0.0 V)

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V _{DD}	- 0.5	+ 4.0	V
Input voltage	V _I	V _{SS} - 0.5	V _{DD} + 0.5	V
Output voltage	V _O	V _{SS} - 0.5	V _{DD} + 0.5	V
Storage temperature	T _{ST}	- 55	+ 125	°C
Operation junction temperature	T _J	- 40	+ 125	°C
Output current	I _O	- 14	+ 14	mA
Overshoot	—	—	V _{DD} + 1.0 (within 50 ns)	V
Undershoot	—	V _{SS} - 1.0 (within 50 ns)	—	V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V _{DD}	VDD	—	3.0	3.3	3.6	V
"H" level input voltage	V _{IH}	XIN, SEL0, SEL1, ENS	—	V _{DD} × 0.80	—	V _{DD} + 0.3	V
"L" level input voltage	V _{IL}		—	V _{SS}	—	V _{DD} × 0.20	V
Input clock Duty Cycle	T _{DCI}	XIN	16.6 MHz to 33.4 MHz	40	50	60	%
Operating temperature	T _a	—	—	- 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

($T_a = +25\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$)

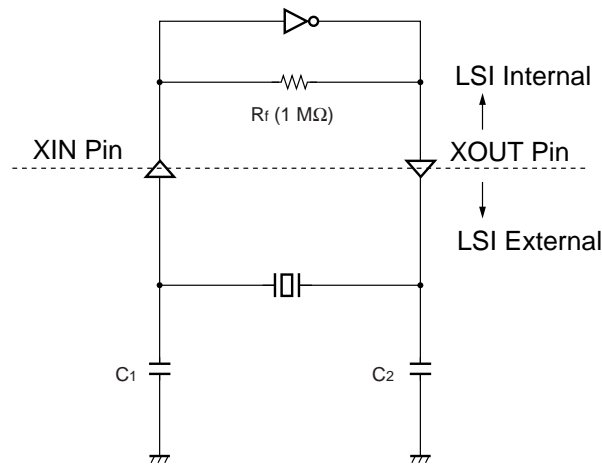
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	VDD	No load capacitance at output 24 MHz MB88151-100	—	5.0	7.0	mA
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation	16.6	—	33.4	MHz
Input frequency	f_{in}	XIN	External clock input	16.6	—	33.4	MHz
Output frequency	f_{OUT}	CKOUT	MB88151-100 (Multiply by 1)	16.6	—	33.4	MHz
			MB88151-200 (Multiply by 2)	33.3	—	66.7	
			MB88151-400 (Multiply by 4)	66.6	—	133.4	
			MB88151-500 (2-frequency division)	8.3	—	16.7	
Output voltage	V_{OH}	CKOUT	H level output, $I_{OH} = -4\text{ mA}$	$V_{DD} - 0.5$	—	V_{DD}	V
	V_{OL}		L level output, $I_{OL} = 4\text{ mA}$	V_{SS}	—	0.4	V
Output through rate	SR	CKOUT	0.4 V to 2.4 V	0.4	—	4.0	V/ns
Output impedance	Z_O	CKOUT	8.3 MHz to 133.4 MHz	—	45	—	Ω
Output clock Duty Cycle	T_{DCC}	CKOUT	1.5 V	40	—	60	%
Input capacitance	C_{IN}	XIN, SEL0, SEL1, ENS	$T_a = +25\text{ }^\circ\text{C}$, $V_{DD} = V_I = 0.0\text{ V}$, $f = 1\text{ MHz}$	—	—	16	pF
Load capacitance	C_L	CKOUT	8.3 MHz to 66.7 MHz	—	—	15	pF
			66.7 MHz to 100 MHz	—	—	10	
			100 MHz to 133.4 MHz	—	—	7	
Input pull-up resistance	R_{pu}	ENS	$V_{IL} = 0.0\text{ V}$	25	50	200	k Ω
Modulation frequency	F_{MOD}	CKOUT	—	—	12.5	—	kHz
Lock-Up time	T_{LK}	CKOUT	—	—	2	5	ms
Cycle-cycle jitter	T_{JC}	CKOUT	MB88151-100, 200 No load capacitance	—	—	100	ps
			MB88151-400 No load capacitance	—	—	150	
			MB88151-500 No load capacitance	—	—	200	

■ OSCILLATION CIRCUIT

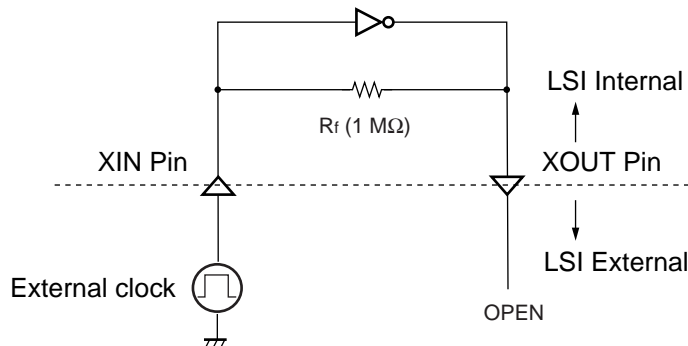
The figure below shows the connection example about general resonator. The oscillation circuit has the built-in resistance (1 MΩ). The value of capacity (C₁ and C₂) is required adjusting to the most suitable value of individual resonator.

Input the clock to XIN, and do not connect anything with XOUT if you use the external clock (you do not use the resonator).

- When using a resonator



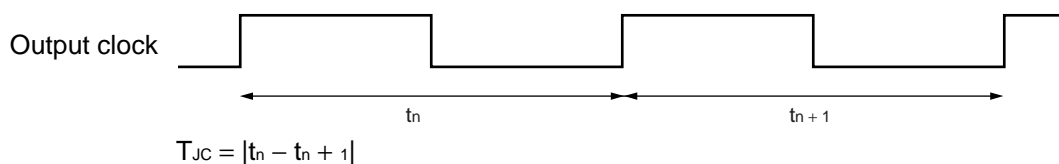
- When using an external clock



- Notes :
- Note that a jitter characteristic of an input clock may cause an affect a cycle-cycle jitter characteristic.
 - For more information on the resonator, contact the Fujitsu sales representative.

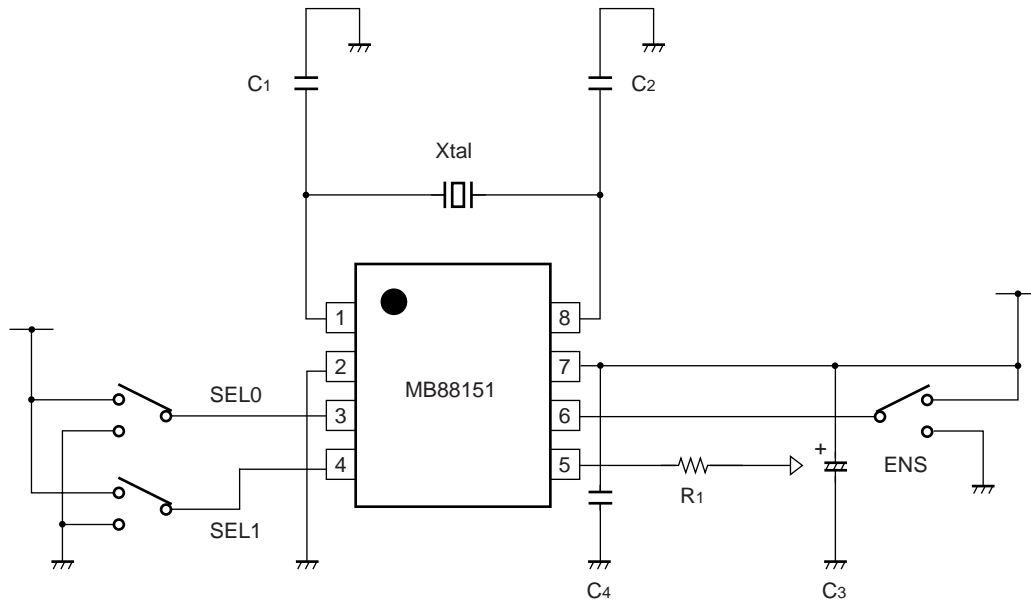
■ DEFINITION OF JITTER

- Cycle-cycle jitter



Cycle - cycle jitter is defined the difference between a certain cycle and immediately after (or, immediately before).

■ INTERCONNECTION CIRCUIT EXAMPLE



- C₁, C₂** : Oscillation stabilization capacitance (see ■ OSCILLATION CIRCUIT.)
C₃ : Ta condenser or electrolytic capacitor of 10 μF or higher
C₄ : Laminated ceramic capacitor about 0.01 μF (connect to close to this device)
R₁ : Impedance matching resistor for board pattern

MB88151

■ ORDERING INFORMATION

Part number	Multiplier ratio	Package	Remarks
MB88151PNF-G-100-JNE1 MB88151PNF-G-200-JNE1 MB88151PNF-G-400-JNE1 MB88151PNF-G-500-JNE1	Multiplied by 1 Multiplied by 2 Multiplied by 4 Multiplied by 1/2	8-pin plastic SOP (FPT-8P-M02)	
MB88151PNF-G-100-JN-EFE1 MB88151PNF-G-200-JN-EFE1 MB88151PNF-G-400-JN-EFE1 MB88151PNF-G-500-JN-EFE1	Multiplied by 1 Multiplied by 2 Multiplied by 4 Multiplied by 1/2	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (EF type)
MB88151PNF-G-100-JN-ERE1 MB88151PNF-G-200-JN-ERE1 MB88151PNF-G-400-JN-ERE1 MB88151PNF-G-500-JN-ERE1	Multiplied by 1 Multiplied by 2 Multiplied by 4 Multiplied by 1/2	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (ER type)

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