MP5001

5V, 1A- 5A Programmable Current Limit Switch

The Future of Analog IC Technology

DESCRIPTION

The MP5001 is a protection device designed to protect circuitry on the output (source) from transients on input (V_{CC}). It also protects V_{CC} from undesired shorts and transients coming from the source.

At start up, inrush current is limited by limiting the slew rate at the source. The slew rate is controlled by a small capacitor at the dv/dt pin. The dv/dt pin has an internal circuit that allows the customer to float this pin (no connect) and still receive a 1.5ms ramp time at the source.

The max load at the output (source) is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor from the I-Limit pin to the Source pin.

An internal charge pump drives the gate of the power device, allowing a very low on-resistance DMOS power FET of just 44mΩ.

The source is protected from the V_{CC} input being too low or too high. Under Voltage Lockout (UVLO) assures that V_{CC} is above the minimum operating threshold, before the power device is turned on. If V_{CC} goes above the high output threshold, the source voltage will be limited.

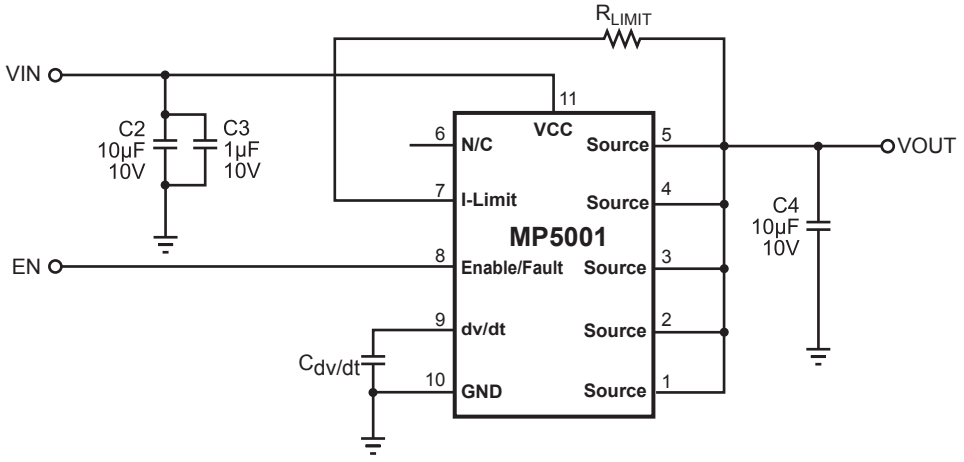
FEATURES

- Integrated 44mΩ Power FET withstand 20V
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit
- Thermal Protection
- Over Voltage Limit

APPLICATIONS

- Hot Swap
- PC Cards
- Cell Phones
- Laptops

TYPICAL APPLICATION

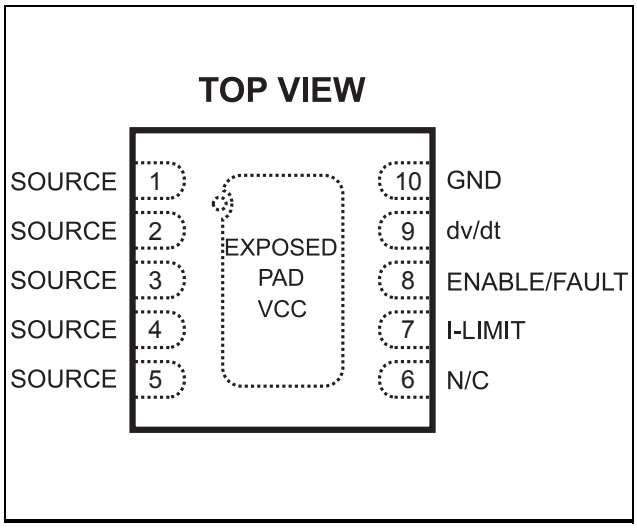


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP5001DQ	QFN10 (3x3)	W5	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP5001DQ–Z)
For RoHS Compliant Packaging, add suffix –LF (e.g. MP5001DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, SOURCE, I-LIMIT 22V
dv/dt, ENABLE/FAULT 6V
Junction Temperature…….–40°C to +150°C
Continuous Power Dissipation (T_A = +25°C)(2)
…….2.5W
Storage Temperature..... –65°C to +155°C

Recommended Operating Conditions

Input Voltage Operating Range…….4V to 10V
Operating Junct. Temp (T_J)…….–40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
QFN10	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, R_{LIMIT}=22Ω, C_{OUT}= 10µF, T_J=25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay Time	t_{DLY}	Enabling of chip to I_D=100mA with a 12Ω resistive load		0.2		ms
ON Resistance	R_{DSon}	T_J=25°C		44	82	mΩ
		Note 4, T_J=80°C		95		
Off State Output Voltage	V_{OFF}	V_{CC}=18V, Enable=0V, R_L=500Ω			120	mV
Continuous Current	I_D	0.5 in^2 pad, Note 4, T_J=25°C		4.2		A
		minimum copper, T_J=80°C		2.3		
Thermal Latch						
Shutdown Temperature	T_{SD}	Note 4		175		°C
Under/Over Voltage Protection						
Output Clamping Voltage	V_{CLAMP}	Overvoltage Protection V_{CC}=8V	5.95	6.65	7.35	V
Under Voltage Lockout	V_{UVLO}	Turn on, Voltage going high	3.2	3.6	4.0	V
Under Voltage Lockout (UVLO) Hysteresis	V_{HYST}			0.1		V
Current Limit						
Hold Current	I_{LIM-SS}	R_{LIMIT}=22Ω, Note 4	1.5	2.1	2.8	A
Trip Current	I_{LIM-OL}	R_{LIMIT}=22Ω, Note 4		3.3		A
dv/dt Circuit						
Slew Rate	dv/dt	Enable to V_{OUT}=4.7V, Note 5	0.8	1.5	2.5	ms
Enable/Fault						
Low Level Input Voltage	V_{IL}	Output Disabled			0.5	V
Intermediate Level Input Voltage	$V_{I\ (INT)}$	Thermal Fault, Output Disabled	0.82	1.6	2.0	V
High Level Input Voltage	V_{IH}	Output Enabled	2.5			V
High State Maximum Voltage	$V_{I\ (MAX)}$			4.8		V
Low Level Input Current (Sink)	I_{IL}	V_{ENABLE}=0V		-28	-50	µA
Maximum Fanout for Fault Signal		Total number of chips that can be connected for simultaneous shutdown			3	Units
Maximum Voltage on Enable Pin	V_{MAX}	Note 6			VCC	V
Total Device						
Bias Current	I_{BIAS}	Device Operational		1.5	2.0	mA
		Thermal Shutdown		0.4		
Minimum Operating Voltage for UVLO	V_{MIN}	Enable<0.5V			3.0	V

Notes:

4) Guaranteed by design.
5) Measure at (30% to 90%)/0.6.
6) Maximum Input Voltage to be≤6.0V if Vcc ≥ 6.0V. Maximum Input Voltage to be Vcc if Vcc ≤ 6.0V.

PIN FUNCTIONS

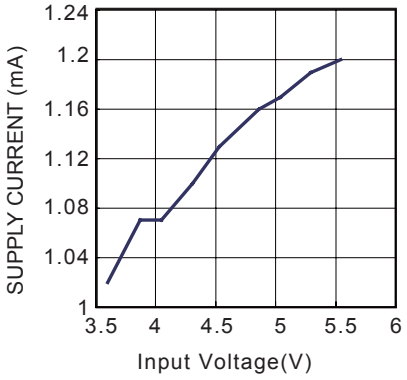
Pin #	Name	Description
1-5	SOURCE	This pin is the source of the internal power FET and the output terminal of the IC.
6	N/C	DO NOT CONNECT, The pin must be float.
7	I-Limit	A resistor between this pin and the Source pin sets the overload and short circuit current limit levels.
8	Enable/Fault	The Enable/Fault pin is a tri-state, bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over the period of 1.5ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
10	GND	Negative Input Voltage to the Device. This is used as the internal reference for the IC.
11	V_{CC}	Positive input voltage to the device (Exposed Pad).

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{EN} =3.3V, R_{LIMIT}=22Ω, C_{OUT}=10uF, Cdv/dt=1nF, T_A=25°C, unless otherwise noted.

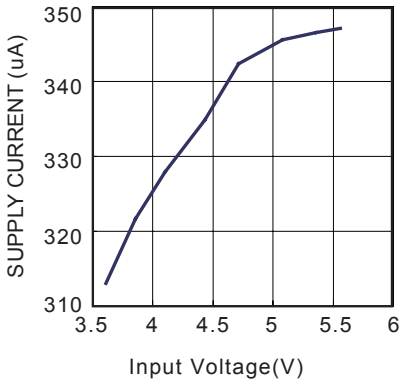
Supply Current,Output Enabled vs. Input Voltage

no load



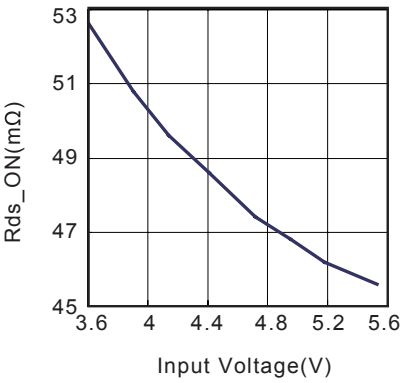
Supply Current,Output Disabled vs. Input Voltage

V_{EN}=0

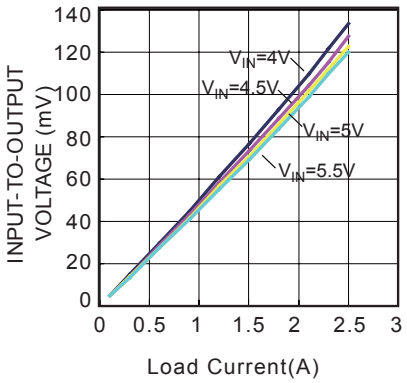


Static Drain-Source On-State Resisitance vs. Input Voltage

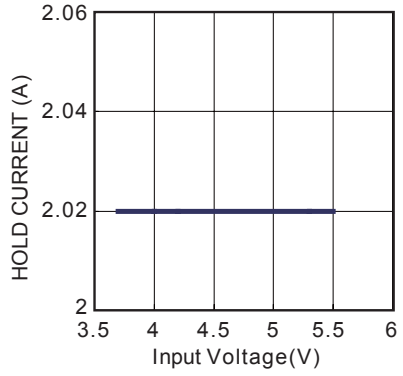
I_{OUT}=0.5A



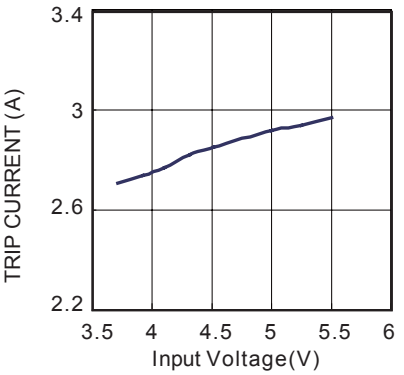
Input to Output Voltage vs. Load Current



Hold Current vs. Input Voltage

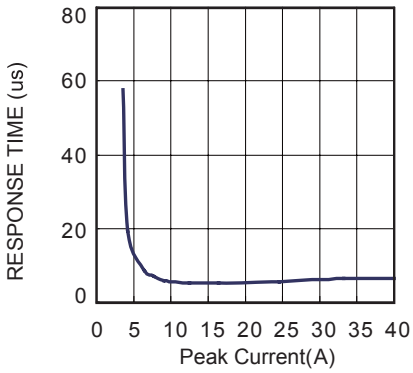


Trip Current vs. Input Voltage

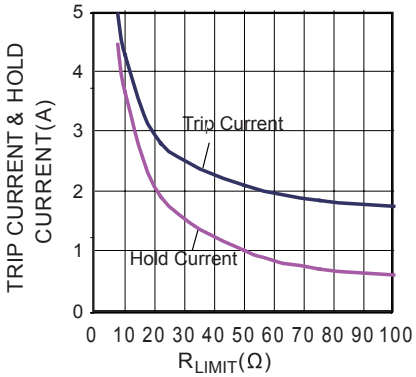


Current Limit Response vs. Peak Currrent

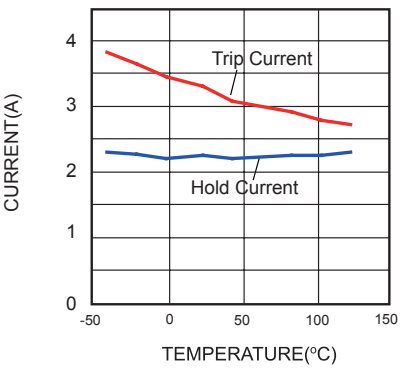
no C_{OUT}



Trip and Hold Current vs. R_{LIMIT}



Trip and Hold Current vs. Temperature

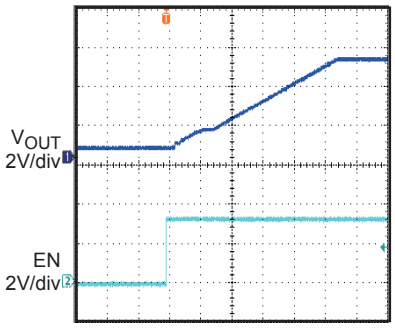


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} =3.3V, R_{LIMIT} =22Ω, C_{OUT} =10uF, Cdv/dt=1nF, T_A =25°C, unless otherwise noted.

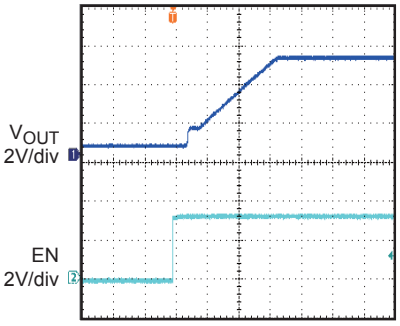
Turn on Delay and Rise Time with 1uF Load

C_{OUT}=1uF,no load



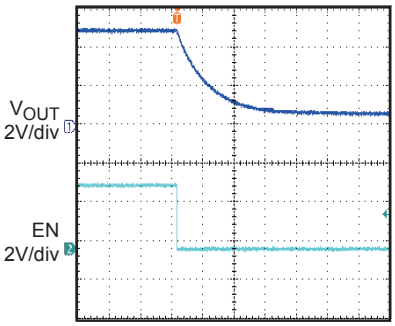
Turn on Delay and Rise Time with 1uF Load,no Cdv/dt

C_{OUT}=1uF,no load



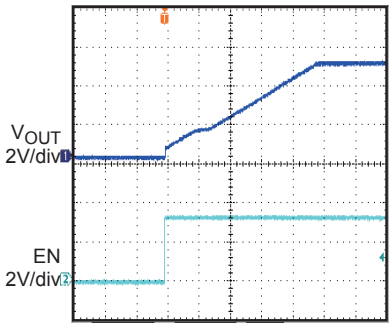
Turn off Delay and Fall Time with 1uF Load

C_{OUT}=1uF,no load



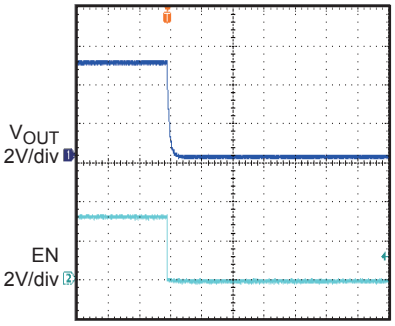
Turn on Delay and Rise Time with 10uF Load

R_{LOAD}=2.64Ω

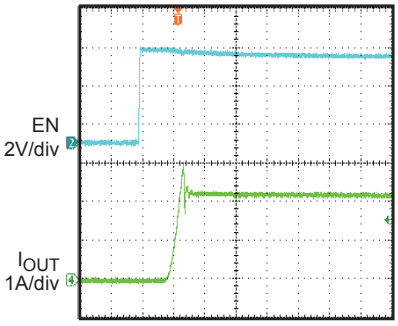


Turn off Delay and Fall Time with 10uF Load

R_{LOAD}=2.64Ω

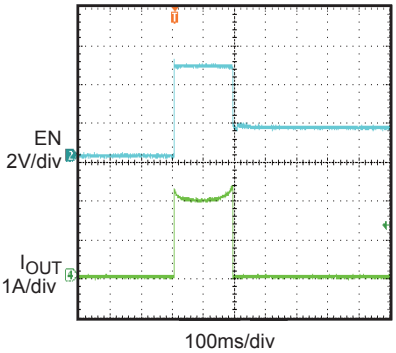


Short Circuit Current,Device Enabled into Short

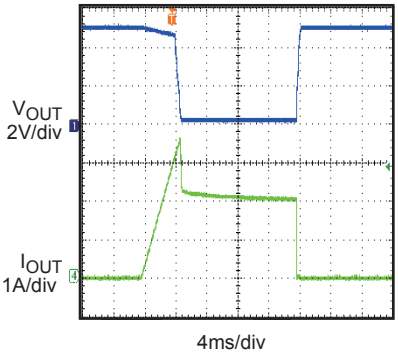


Short Circuit Current,Device Enabled into Short, and Thermal Shut down

EN floating

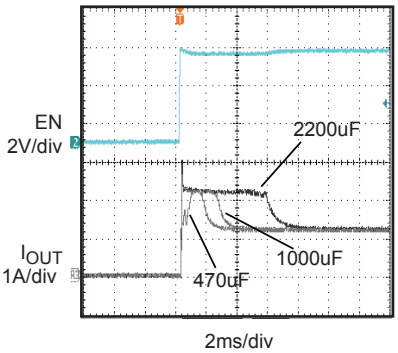


Trip Current with Ramped Load on Enabled Device



Inrush Current with Different Load Capacitance

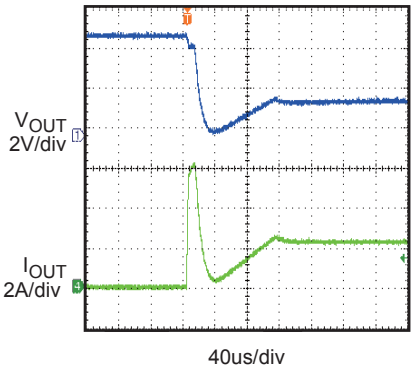
R_{LOAD}=3.9Ω ,no Cdv/dt,EN floating



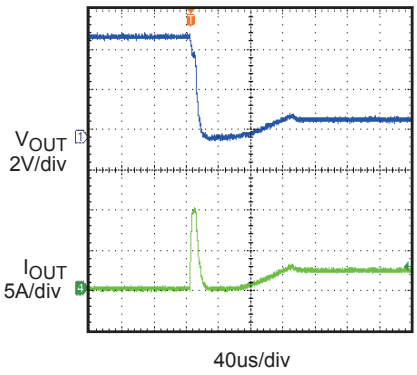
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} =3.3V, R_{LIMIT} =22Ω, C_{OUT} =10uF, Cdv/dt=1nF, T_A =25°C, unless otherwise noted.

0.66Ω Load Connected to Enabled Device

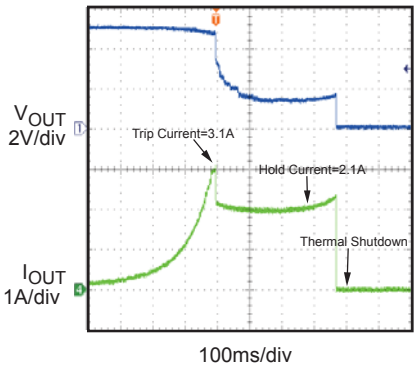


0.33Ω Load Connected to Enabled Device



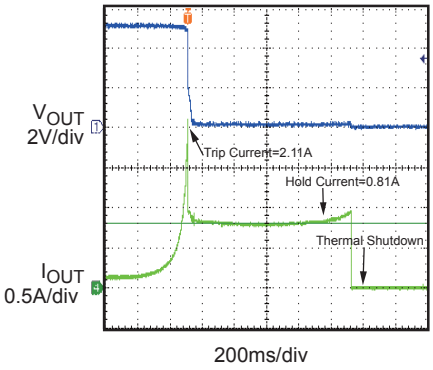
Current Limit

R_{LIMIT}=22Ω



Current Limit

R_{LIMIT}=60Ω



BLOCK DIAGRAM

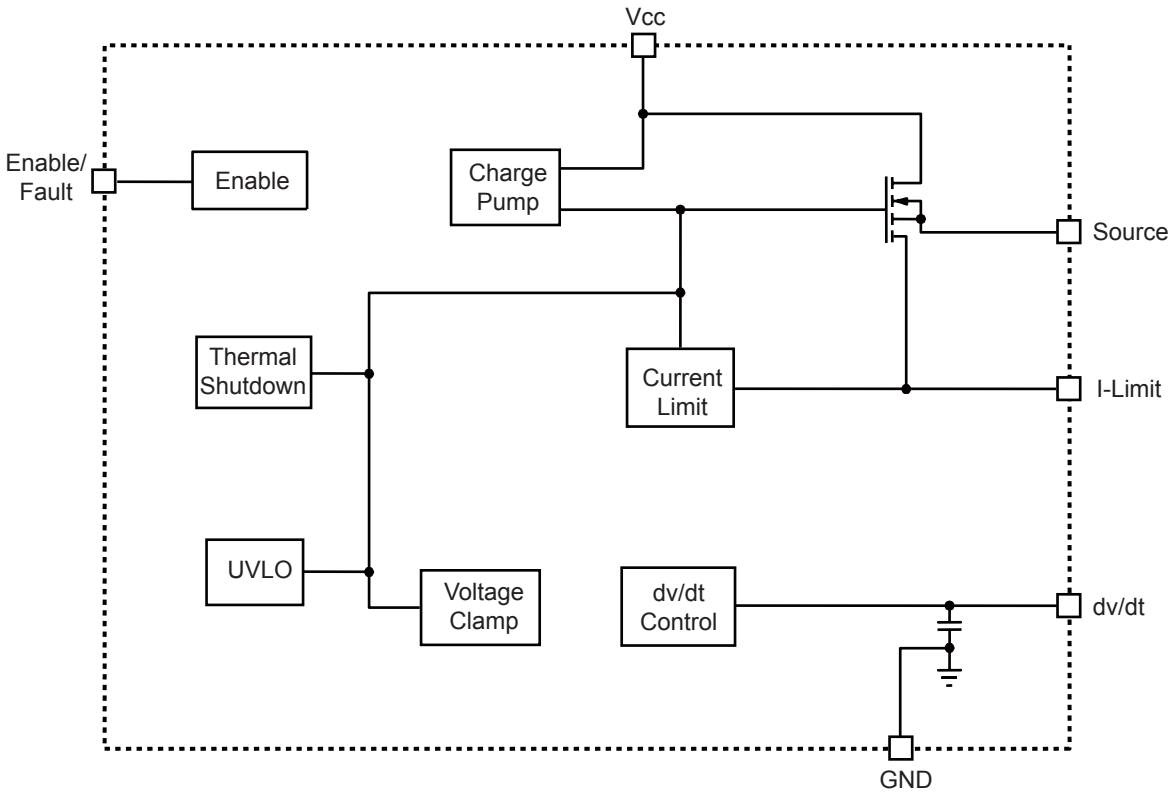


Figure 1—Functional Block Diagram

CURRENT LIMIT

The desired current limit is a function of the external current limit resistor.

Table 1—Current Limit vs. Current Limit Resistor (V_{CC}=5V)

Current Limit Resistor (Ω)	22	50	100
Trip Current (A)	3.3	2.1	1.75
Hold Current (A)	2.1	1	0.6

The hold current refers to the current limit. However, the current limit is set to the "trip current" level when the output (source voltage) is near Vcc. As the output decreasing, the current limit is decreased to the "hold current" level.

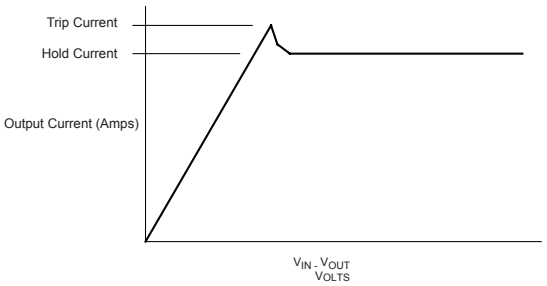


Figure 2—Load Current vs. Voltage Drop

In a typical application using a current limit resistor of 22Ω, the trip current will be 3.3A and the hold current will be 2.1A. If the device is in its normal operating state and passing 2.1A it will need to dissipate only 194mW with the very low on resistance of 44mΩ. For the package dissipation of 50°C/Watt, the temperature rise will only be + 9.7°C. Combined with a 25°C ambient, this is only 34.7°C total package temperature.

During a short circuit condition, the device now has 5V across it and the hold current clamps at 2.1A and therefore must dissipate 10.5W. At 50°C/watt, if uncontrolled, the temperature would rise above the thermal protection threshold (+175°C) and the device will shutdown to cause the temperature to drop.

Proper heat sink must be used if the device is intended to supply the hold current and not shutdown. Without a heat sink, hold current should be maintained below 600mA at + 25°C and below 360mA at +85°C to prevent the device from activating the thermal shutdown feature.

RISE TIME

The rise time is a function of the capacitor (Cdv/dt) on the dv/dt pin.

Table 2—Rise Time vs. Cdv/dt

Cdv/dt	none	50pF	500pF	1nF
Rise Time* (TYPICAL) (ms)	1.4	2.8	15.4	29.4

* **Notes:** Rise Time = K_{RT}*(50pF+$C_{dv/dt}$), K_{RT} =28E6

The "start-up rise time" is measured by taking the 10% to 90% time and multiplied by 1.25 to get the "interpolated" 0% to 100% rise time.

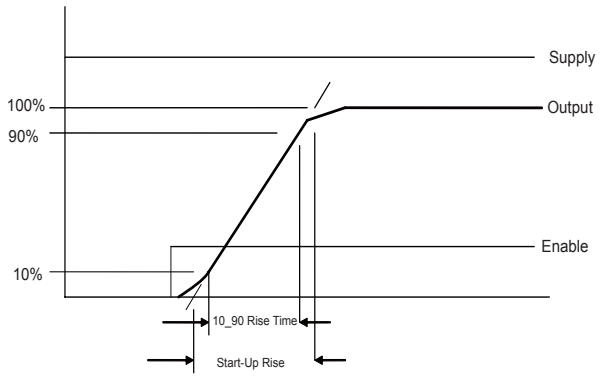


Figure 3—Start-up Rise Time

FAULT AND ENABLE PIN

The Enable/Fault Pin is a Bi-Directional three levels I/O with a weak pull up current (25uA typical). The three levels are low, mid and high. It functions to enable/disable the part and to relay Fault information.

Enable pin as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

Enable pin as an output:

1. The pull up current may (if not over ridden) allow a "wired nor" pull up to enable the part.
2. An under voltage will cause a low on the enable pin, and will clear the fault flag.
3. A thermal fault will cause a mid level on the enable pin, and will set the fault flag.

The Enable/Fault line must be above the mid level for the output to be turned on.

The fault flag is a internal flip-flop that can be set or reset under various conditions:

1. Thermal Shutdown: set fault flag
2. Under Voltage: reset fault flag
3. Low voltage on Enable/Fault pin: reset fault flag
4. Mid voltage on Enable/Fault pin: no effect

Under a fault, the Enable/Fault pin is driven to the mid level.

There are 4 types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag. In a typical application there are one or more chips in a system. The Enable/Fault lines will typically be connected together.

Table 3—Fault Function Influence in Application

Fault description	Internal action	Effect on Fault Pin	Effect on Flag	Effect on secondary Part
Short/over current	Limit current	none	none	none
Under Voltage	Output is turned off	Internally drives Enable/Fault pin to Logic low	Flag is reset	Secondary part output is disabled, and fault flag is reset.
Over Voltage	Limit output voltage	None	None	None
Thermal Shutdown	Shutdown part. The part is latched off until a UVLO or externally driven to ground.	Internally drives Enable/Fault pin to mid level	Flag is Set	Secondary part output is disabled.

UNDER VOLTAGE LOCK OUT OPERATION

If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

When the supply goes above the UVLO threshold, the output is enabled and the fault line is released. When the fault line is released it will be pulled high by a 25uA current source. No external pull up resistor is required. In addition, the pull up voltage is limited to 5 volts.

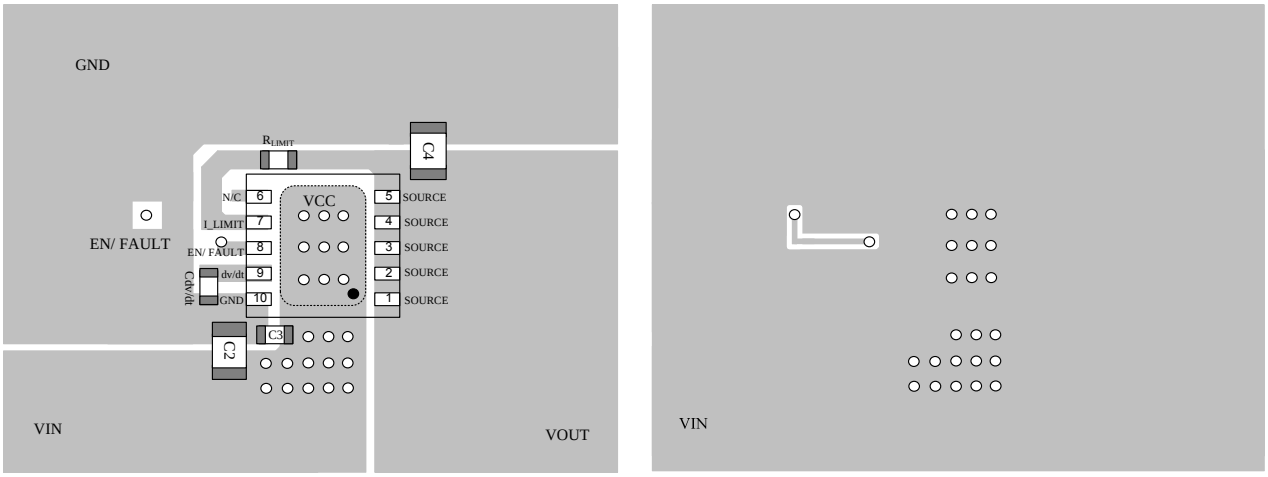
THERMAL PROTECTION

When thermal protection is triggered, the output is disabled and the fault line is driven to the mid level. The thermal fault condition is latched (meaning the fault flag is set), and the part will remain latched off until the fault (enable) line is brought low. Cycling the power below the UVLO threshold will also reset the fault flag.

PCB LAYOUT

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference.

Place Rlimit close to I_limit pin, Cdv/dt close to dv/dt pin and input cap close to Vcc (Exposed Pad). Keep the N/C pin float. Put vias in thermal pad and ensure enough copper area near Vcc and source to achieve better thermal performance.

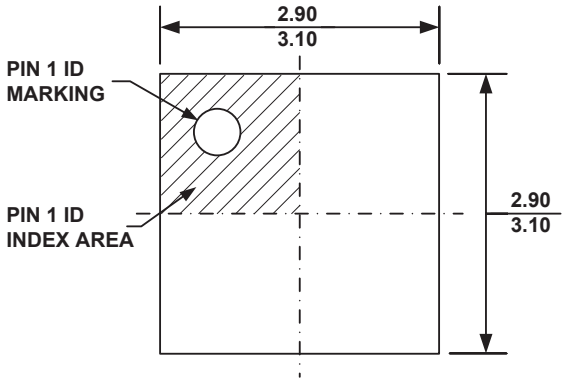


Top Layer **Bottom Layer**

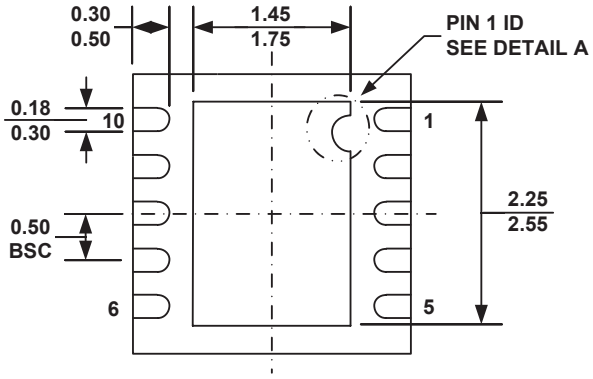
Figure 4—PCB Layout

PACKAGE INFORMATION

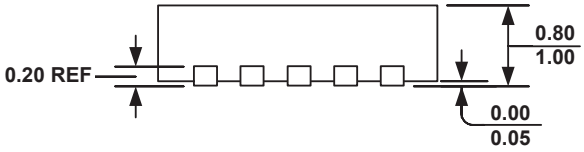
QFN10 (3mm x 3mm)



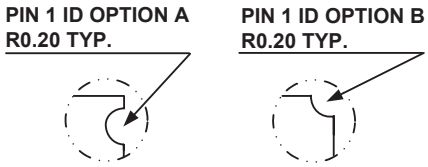
TOP VIEW



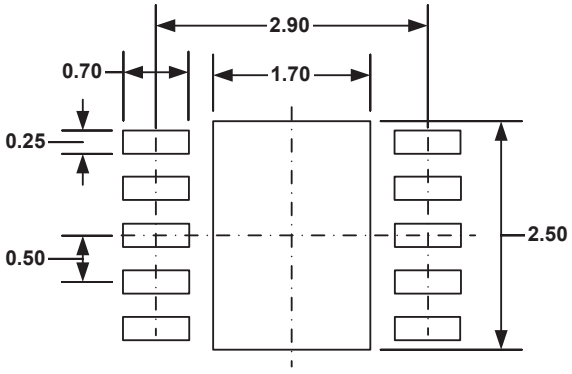
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.