

# MB15U36

## Dual PLL Frequency Synthesizer with On-Chip Prescaler



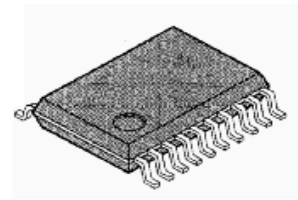
### Description

The Fujitsu MB15U36 dual PLL is a serial input frequency synthesizer with 2.0 GHz and 1.2 GHz prescalers. The prescalers both have a selectable dual modulus division ratio of 64/65 or 128/129 enabling pulse swallow operation. The MB15U36 utilizes a refined charge pump design (Fujitsu's Super Charger) that provides fast tuning along with low spurious noise and phase noise characteristics. The MB15U36 is ideally suited for digital mobile communications, including GSM, DCS1800, PCS1900, IS-136, IS-95 and ISM-band applications.

### Features

- Very low spurious and phase noise characteristics
- Wide operating voltage: 3.0 to 5.5 volts
- Low operating current: 6.0 mA @ Vcc = 3 volts (typical)
- Power-saving current: 10µA (typical)
- Wide operating temperature: -40 to +85°C
- Plastic 20-pin SSOP package
- Reference counter:
  - 15-bit programmable divider: 3 to 32767
- 18-bit programmable divider:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2047
- Software selectable charge pump current:
  - Do output ±1.0 or ±4.0 mA @ Vcc = 3V
- Evaluation Kits available

### Packages



20-pin plastic SSOP,  
FPT-20P-M03

Parameter	MB15U36
RF frequency of operation, max.	2.0 GHz
IF/RF frequency of operation, max	1.2 GHz
Low power supply voltage	3 - 5.5V
Low power supply current	6.0 mA @ 3V
Prescaler divide ratios	RF1, RF2 = 64/65 or 128/129
Power-saving function	10µA typical

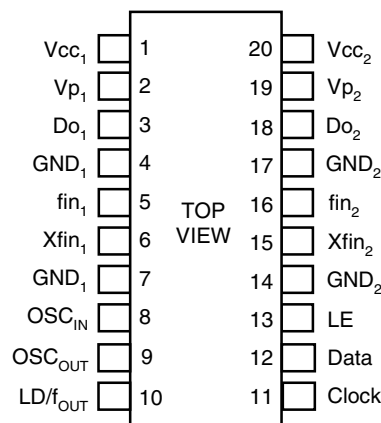
## Table of Contents

Pin Descriptions: MB15U36.....	4
Block Diagram: MB15U36.....	5
Absolute Maximum Ratings.....	6
Recommended Operating Conditions.....	6
Handling Precautions.....	6
Electrical Characteristics.....	7
Measurement Circuit (fin, OSCIN Input Sensitivity).....	9
Typical Electrical Characteristics.....	10
Reference Information.....	13
Functional Descriptions.....	14
Serial Data Input.....	14
Table 1: Control Bits.....	14
Shift Register Configuration for the Programmable Reference Counter.....	14
Shift Register Configuration for the Programmable Counter.....	15
Table 2: Binary 14-bit Programmable Reference Counter Data Setting.....	15
Table 3: Phase Comparator Phase Switching Data Setting.....	15
Table 4: Charge Pump Current Setting.....	16
Table 5: Charge Pump Output Impedance Setting.....	16
Table 6: LD/fOUT Output Select Data Setting.....	16
Table 7: Binary 11-bit Programmable Counter Data Setting.....	16
Table 8: Binary 7-bit Swallow Counter Data Setting.....	17
Table 9: Prescaler Data Setting.....	17
Power Saving Mode (Intermittent Mode Control Circuit).....	17
Table 10: Power Save Internal Shutdown Logic.....	17
Serial Data Input Timing.....	18
Table 11: Timing Parameters.....	18
Power-ON Timing Diagram.....	18
Phase Detector Output Waveform.....	19
Application Example.....	20
Application Example: Fastlock Mode.....	21
Ordering Information.....	22
Package Dimensions.....	23

# Dual PLL Frequency Synthesizer with On-Chip Prescaler

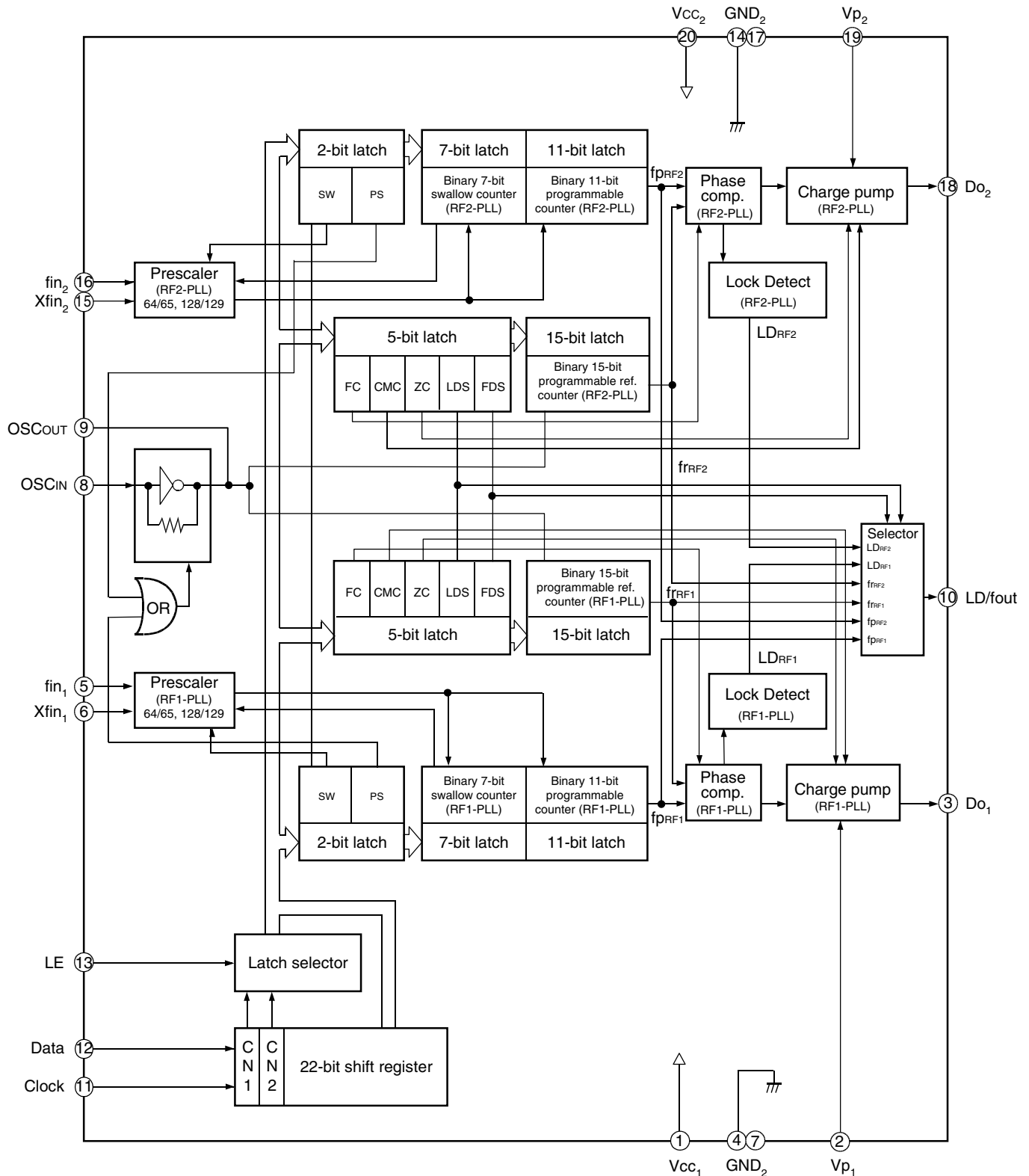
## Pin Descriptions: MB15U36

Pin No. SSOP	Pin Name	I/O	Descriptions
1	V <sub>CC1</sub>	–	Power supply voltage input pin for the RF1-PLL section, the shift register, and the oscillator input buffer. When power is OFF, latched data for RF1-PLL is lost.
2	V <sub>p1</sub>	I	Power supply for the RF1-PLL charge pump. (Independent of pin 19)
3	Do <sub>1</sub>	O	Charge pump output for the RF1-PLL section. Phase detector characteristics can be reversed using the FC-bit.
4	GND1	–	Ground for the RF1-PLL section.
5	fin <sub>1</sub>	I	Prescaler input for the RF1-PLL. Connection to an external VCO should be via AC coupling.
6	Xfin <sub>1</sub>	I	Prescaler complimentary input for the RF1-PLL section. This pin should be grounded via a small capacitor.
7	GND1	–	Ground for the RF1-PLL section.
8	OSC <sub>IN</sub>	I	External TCXO reference oscillator input or connection to crystal. TCXO should be connected via AC coupling.
9	OSC <sub>OUT</sub>	O	Oscillator output or connection to crystal.
10	LD/f <sub>OUT</sub>	O	Lock detect signal output (LD) or phase comparator monitoring output (f <sub>out</sub> ). The output signal is selected by the LDS and FDS bits in the serial programming data.
11	Clock	I	Clock input for the 22-bit shift register. One bit of data is shifted into the shift register on a rising edge of the clock.
12	Data	I	Serial data input. Data is transferred to the corresponding latch (RF1-ref counter, RF1-prog. counter, RF2-ref. counter, RF2-prog. counter) according to the control bits settings in the serial programming data.
13	LE	I	Load enable signal input. When the LE bit is set to "H", data in the shift register is transferred to the corresponding latch according to the control bits settings in the serial programming data.
14	GND2	–	Ground for the RF2-PLL section.
15	Xfin <sub>2</sub>	I	Prescaler complimentary input for the RF2-PLL section. This pin should be grounded via a small capacitor.
16	fin <sub>2</sub>	I	Prescaler input for the RF2-PLL. Connection to an external VCO should be via AC coupling.
17	GND2	–	Ground for the RF2-PLL section.
18	Do <sub>2</sub>	O	Charge pump output for the RF2-PLL section. Phase detector characteristics can be reversed using the FC-bit.
19	V <sub>p2</sub>	I	Power supply for the RF2-PLL charge pump. (Independent of pin 2)
20	V <sub>CC2</sub>	–	Power supply voltage input pin for the RF2-PLL section. When power is OFF, latched data for RF2-PLL is lost.



(FPT-20P-M03)

## Block Diagram: MB15U36



# Dual PLL Frequency Synthesizer with On-Chip Prescaler

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	$V_{CC1,2}$	-0.5 to +6.5	V	
	$V_{P1,2}$	-0.5 to +6.5	V	
Input voltage	$V_I$	-0.5 to +6.5	V	
Output voltage	$V_O$	-0.5 to +6.5	V	
Storage temperature	$T_{STG}$	-55 to +125	°C	

WARNING: Semiconductor devices can be permanently damaged by the application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power supply voltage	$V_{CC}$	3.0	5.0	5.5	V	$V_{CC1} = V_{CC2}$
	$V_P$	3.0	5.0	5.5	V	$V_{CC1} = V_{CC2}$ *1
Input voltage	$V_I$	GND	–	$V_{CC}$	V	
Operating temperature	$T_a$	-40	–	+85	°C	

\*1: Prescaler divide ratio is only 64/65 (SW = "L") at RF1.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Fujitsu representative beforehand.

## Handling Precautions

- This device should be transported and stored in anti-static containers
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

## Electrical Characteristics

( $V_{CC} = 3.0$  to  $5.5V$ ,  $T_a = -40$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Value			Unit		
			Min.	Typ.	Max.			
Power supply current	I <sub>CC1</sub> *1	f <sub>in1</sub> = 2000 MHz f <sub>osc</sub> = 12 MHz	V <sub>CC</sub> = 5V	–	6.0	–	mA	
			V <sub>CC</sub> = 3V	–	3.5	–	mA	
	I <sub>CC2</sub> *2	f <sub>in2</sub> = 1200 MHz f <sub>osc</sub> = 12 MHz	V <sub>CC</sub> = 5V	–	3.0	–	mA	
			V <sub>CC</sub> = 3V	–	2.5	–	mA	
Power saving current	I <sub>PS1</sub>	V <sub>CC1</sub> current at PS bit <sub>RF1, RF2</sub> = "H"	–	0.1*3	10	μA		
	I <sub>PS2</sub>	V <sub>CC1</sub> current at PS bit <sub>RF2</sub> = "H"	–	0.1*3	10	μA		
Operating frequency	f <sub>in1</sub> *4	RF1-PLL	100	–	2000	MHz		
	f <sub>in2</sub> *4	RF2-PLL	50	–	1200	MHz		
	f <sub>OSC</sub>	500mVp-p minimm	3	–	40	MHz		
Input sensitivity	f <sub>in</sub> RF1-PLL	P <sub>fin</sub> RF1- PLL 50Ω load system (Refer to measurement circuit.)	–10	–	+2	dBm		
	f <sub>in</sub> RF2-PLL	P <sub>fin</sub> RF2-PLL 50Ω load system (Refer to measurement circuit.)	–10	–	+2	dBm		
	OSC <sub>IN</sub>	V <sub>OSC</sub>	0.5	–	V <sub>CC</sub>	Vp-p		
Input voltage	Data, Clock, LE	V <sub>IH</sub>	V <sub>CC</sub> × 0.8		–	V		
		V <sub>IL</sub>	–	–	V <sub>CC</sub> × 0.2			
Input current	Data, Clock, LE	I <sub>IH</sub> *5	V <sub>IH</sub> = V <sub>CC</sub>	–1.0	–	+1.0	μA	
		I <sub>IL</sub> *5	V <sub>IL</sub> = V <sub>CC</sub>	–1.0	–	+1.0		
	OSC <sub>IN</sub>	I <sub>IH</sub>	V <sub>IH</sub> = V <sub>CC</sub>	0	–	+100	μA	
		I <sub>IL</sub> *5	V <sub>IL</sub> = V <sub>CC</sub>	–100	–	0		
Output voltage	LD/f <sub>OUT</sub>	V <sub>OH</sub>	I <sub>OH</sub> = –1 mA	V <sub>CC</sub> – 0.4		–	V	
		V <sub>OL</sub>	I <sub>OL</sub> = 1 mA	–	–	0.4		
	D <sub>01</sub> , D <sub>02</sub>	V <sub>DOH</sub>	I <sub>OH</sub> = –0.5 mA	V <sub>CC</sub> – 0.4		–	V	
		V <sub>DOL</sub>	I <sub>OL</sub> = 0.5 mA	–	–	0.4		
High impedance cutoff current	D <sub>01</sub> , D <sub>02</sub>	I <sub>OFF</sub>	V <sub>CC</sub> = V <sub>p</sub> = 5.0V 0.5V ≤ V <sub>DO</sub> ≤ V <sub>p</sub> – 0.5V	–	–	3.0	nA	
		LD/f <sub>OUT</sub>	I <sub>OH</sub> *5	V <sub>CC</sub> = 5.0V	–1.0	–	–	mA
Output current	LD/f <sub>OUT</sub>		I <sub>OL</sub>	V <sub>CC</sub> = 5.0V	–	–	1.0	mA
		I <sub>DOH</sub> *5	V <sub>CC</sub> = V <sub>p</sub> = 5.0V	CMC bit = "L"	–	–1.25	–	mA
	V <sub>CC</sub> = V <sub>p</sub> = 3.0V		CMC bit = "L"	–	–1.0	–	mA	
	D <sub>01</sub> , D <sub>02</sub>	I <sub>DOL</sub>	V <sub>CC</sub> = V <sub>p</sub> = 5.0V	CMC bit = "L"	–	1.25	–	mA
			V <sub>CC</sub> = V <sub>p</sub> = 3.0V	CMC bit = "L"	–	1.0	–	mA
	I <sub>DOH</sub> *5	V <sub>CC</sub> = V <sub>p</sub> = 5.0V	CMC bit = "H"	–	–5.0	–	mA	
		V <sub>CC</sub> = V <sub>p</sub> = 3.0V	CMC bit = "H"	–	–4.0	–	mA	
	I <sub>DOL</sub>	V <sub>CC</sub> = V <sub>p</sub> = 5.0V	CMC bit = "H"	–	5.0	–	mA	
V <sub>CC</sub> = 3.0V		CMC bit = "H"	–	4.0	–	mA		

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Parameter	Symbol	Condition	Value			Unit	
			Min.	Typ.	Max.		
Charge pump current characteristics	$I_{DOL}/I_{DOH}$	$I_{DOMT}^{*6}$	$V_{D0} = V_{CC}/2$	–	3	–	%
	$I_{D0}$ vs $V_{D0}$	$I_{DOVD}^{*7}$	$0.5V \leq V_{D0} \leq V_{CC} - 0.5V$	–	15	–	%
	$I_{D0}$ vs $T_a$	$I_{DOTA}^{*8}$	$-40^{\circ}C \leq T_a \leq +85^{\circ}C$ , $V_{D0} = V_{p}/2$	–	10	–	%

\*1: Conditions:  $V_{CC1} = 5.0V$ ,  $T_a = +25^{\circ}C$ , in locking state.

\*2: Conditions:  $V_{CC2} = 5.0V$ ,  $T_a = +25^{\circ}C$ , in locking state.

\*3: Conditions:  $V_{CC} = 5.0V$ ,  $f_{OSC} = 12.8MHz$  (-2dBm),  $T_a = +25^{\circ}C$

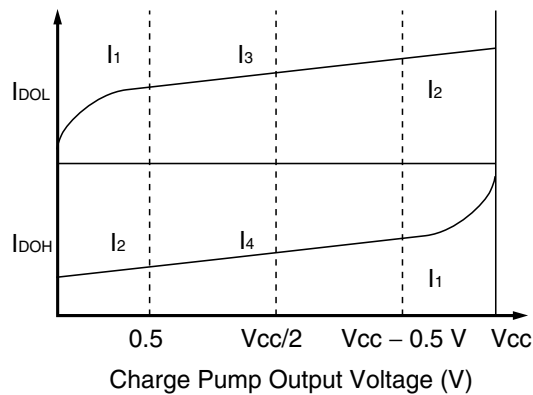
\*4: AC coupling, 1000pF capacitor is connected under the condition of min. operating frequency.

\*5: The symbol “-” (minus) means direction of current flow.

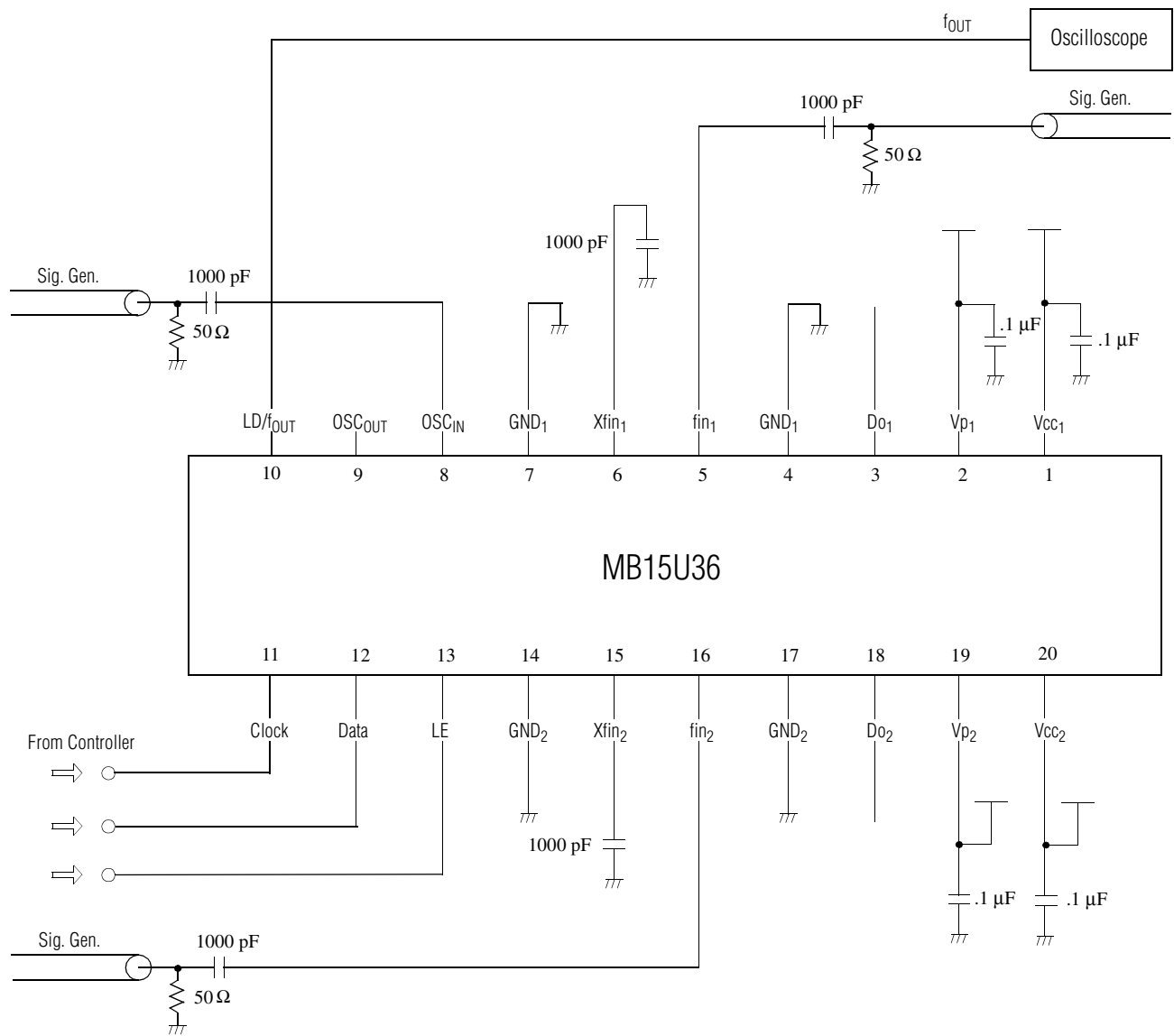
\*6:  $V_{CC} = 5.0V$ ,  $T_a = +25^{\circ}C$   $(|I_3| - |I_4|)/(|I_3| + |I_4|)/2 \times 100(\%)$

\*7:  $V_{CC} = 5.0V$ ,  $T_a = +25^{\circ}C$   $(|I_2| - |I_1|)/(|I_1| + |I_2|)/2 \times 100(\%)$  (Applied to each  $I_{DOL}$ ,  $I_{DOH}$ )

\*8:  $V_{CC} = 5.0V$ ,  $(|I_{D0}(85^{\circ}C) - I_{D0}(-40^{\circ}C)|/2)/(|I_{D0}(85^{\circ}C) + I_{D0}(-40^{\circ}C)|/2) \times 100(\%)$  (Applied to each  $I_{DOL}$ ,  $I_{DOH}$ )



## Measurement Circuit (For Measuring Input Sensitivity of fin and OSCin)

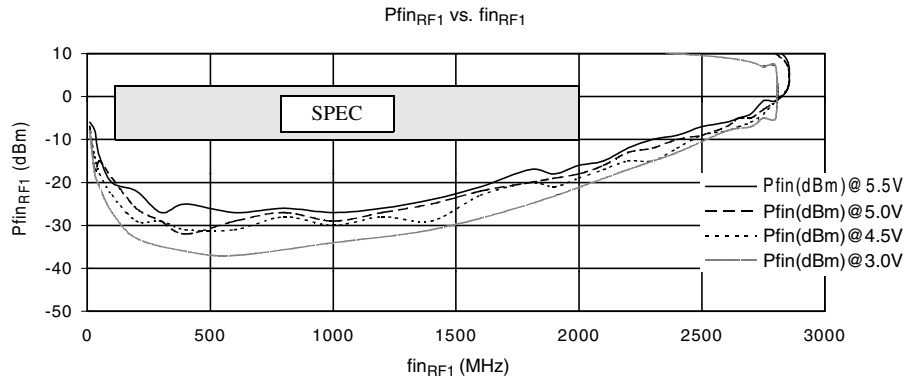




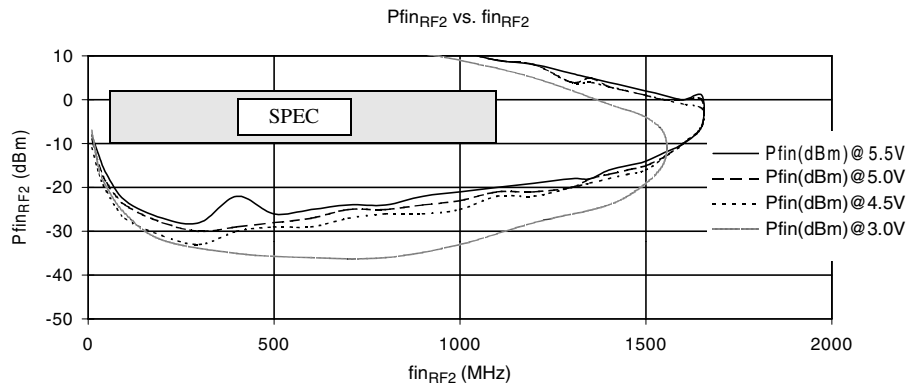
# Dual PLL Frequency Synthesizer with On-Chip Prescaler

## Typical Electrical Characteristics: MB15U36

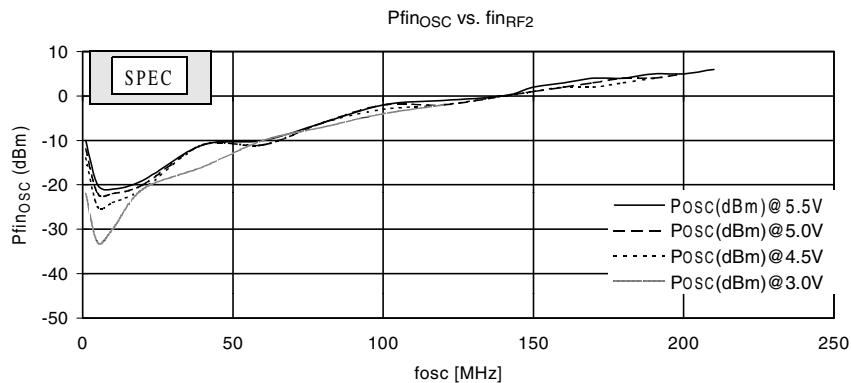
### Input Sensivity of fin (RF1) versus Input Frequency



### Input Sensivity of fin (RF2) versus Input Frequency



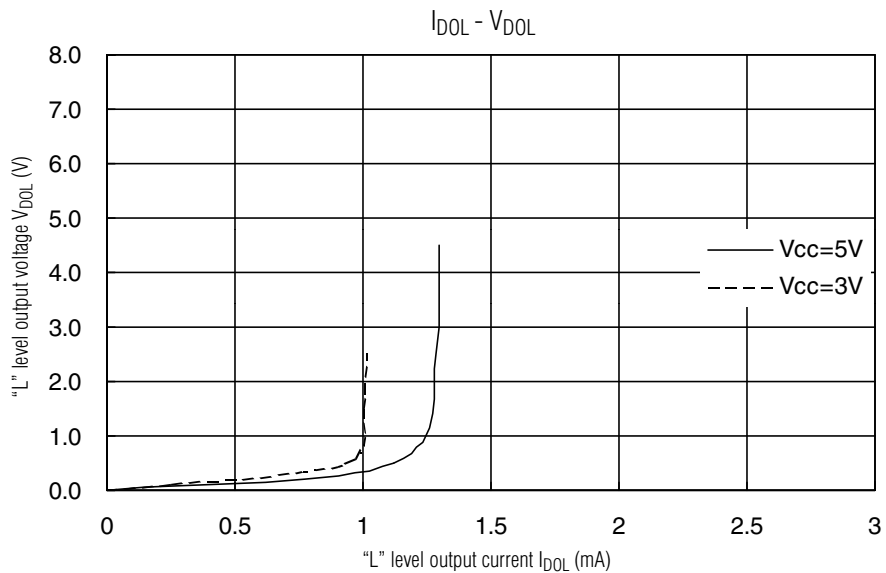
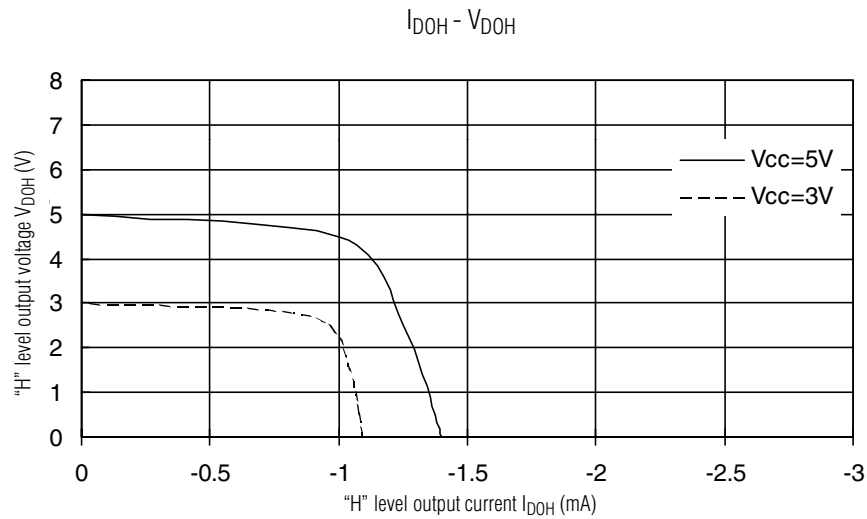
### Input Sensivity of OSC<sub>IN</sub> versus Input Frequency



## Typical Electrical Characteristics: MB15U36

Conditions:  $T_a = +25^\circ\text{C}$

Do output current: 1 x Do mode

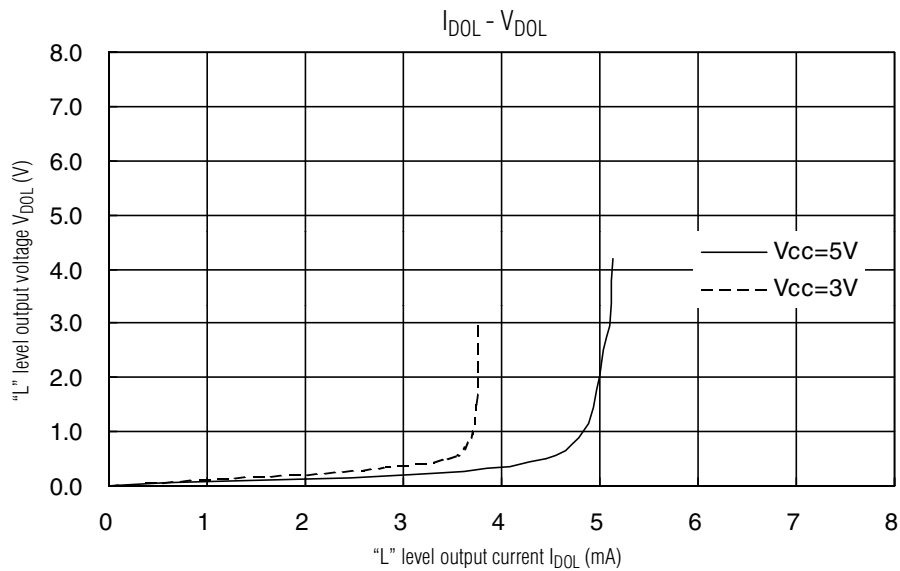
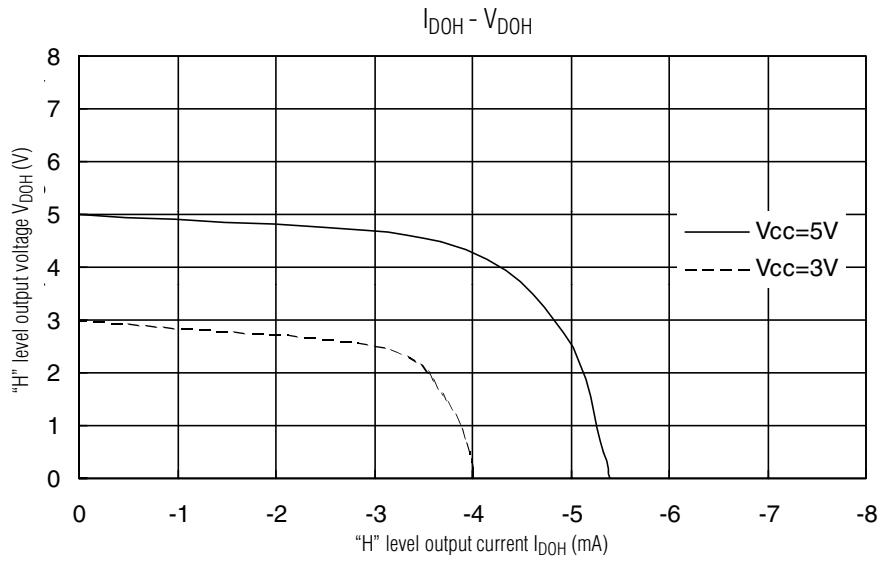


# Dual PLL Frequency Synthesizer with On-Chip Prescaler

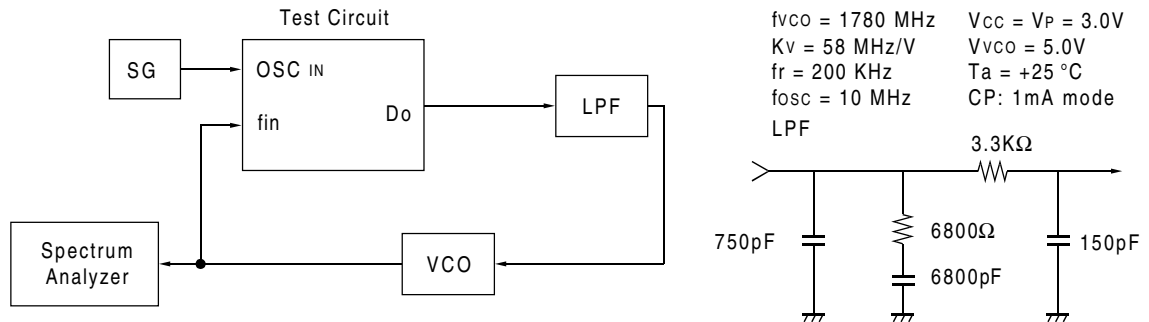
## Typical Electrical Characteristics: MB15U36

Conditions:  $T_a = +25^\circ\text{C}$

Do output current: 4 x Do mode

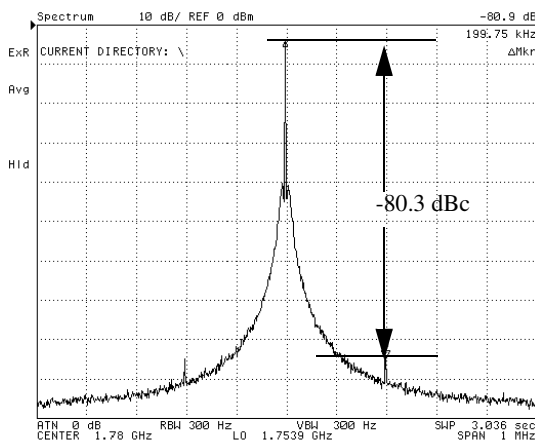


## Reference Information: MB15U36

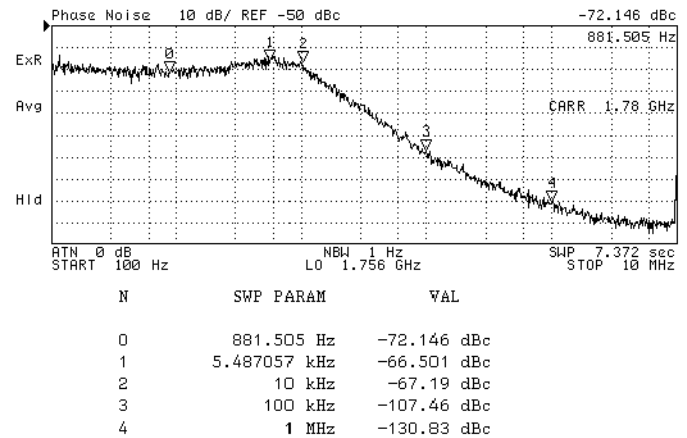


Typical plots measure with the test circuit are shown below. Each plot shows lock up time, phase noise, and reference leakage.

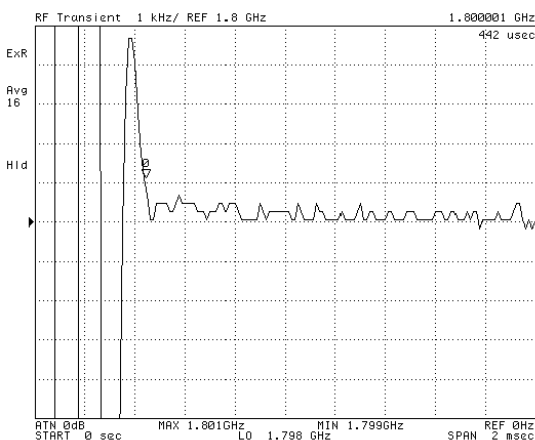
**RF PLL Reference Leakage**  
@ 200 kHz offset = -80.3 dBc



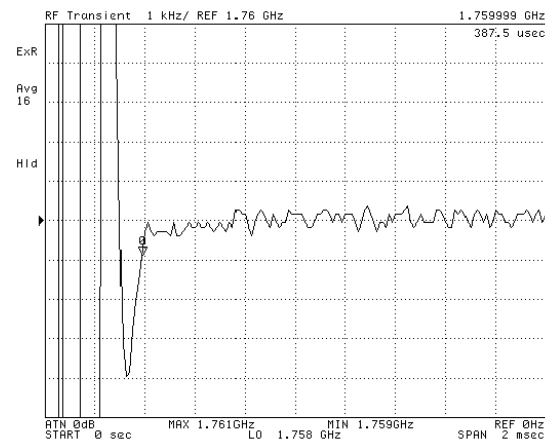
**RF PLL Phase Noise**  
@ max within loop band = -66.5 dBc/Hz



**RF PLL Lock Up Time = 442μs**  
(1760.000 MHz → 1800.000 MHz, within ± 1kHz)



**RF PLL Lock Up Time = 387μs**  
(1800.000 MHz → 1760.000 MHz, within ± 1kHz)



# Dual PLL Frequency Synthesizer with On-Chip Prescaler

## Functional Descriptions

The VCO output frequency can be calculated using the following equation:

$$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$$

- $f_{VCO}$ : Output frequency of external voltage controlled oscillator (VCO)
- M: Preset divide ratio of dual modulus prescaler (64 or 128 for RF1-PLL or RF2-PLL2)
- N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A: Preset divide ratio of binary 7-bit swallow counter ( $0 \leq A \leq 127$ )
- $f_{OSC}$ : Reference oscillation frequency
- R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 32,767)

## Serial Data Input

Serial data is entered using the Data, Clock, and LE pins. The serial data controls the programmable reference counters and the programmable counters separately.

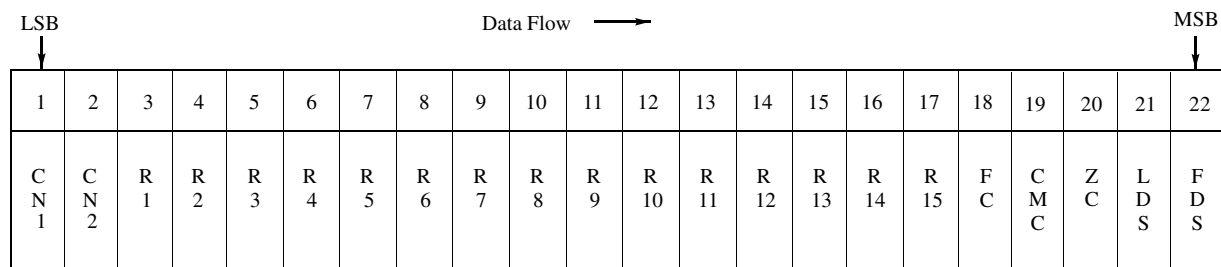
Binary serial data is entered through the Data pin when the LE pin is held low. One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, entered data is latched into the appropriate counters according to the control bit settings as follows:

**Table 1. Control Bits**

Control Bits		Destination of Serial Data
CN1	CN2	
L	L	The programmable reference counter for the RF2-PLL
L	H	The programmable reference counter for the RF1-PLL
H	L	The programmable counter and the swallow counter for the RF2-PLL
H	H	The programmable counter and the swallow counter for the RF1-PLL

## Shift Register Configuration

### Programmable Reference Counter

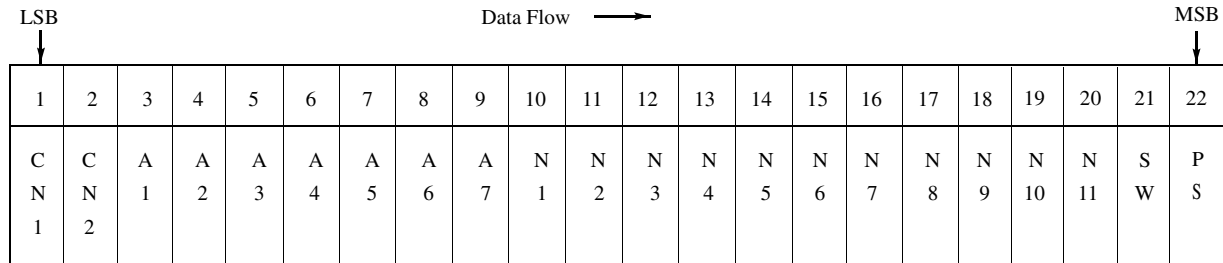


- CN1, 2 Control bits [Table 1]
- R1 to R15 Divide ratio setting bits for the programmable reference counter (3 to 32,767) [Table 2]
- FC Phase control bit for the phase detector [Table 3]
- CMC Charge pump current select bit [Table 4]
- ZC Forced high impedance control for the charge pump [Table 5]
- LDS/FDS LD/ $f_{OUT}$  signal select bits [Table 6]

Note: Input Data with MSB first.

## Functional Descriptions

### Programmable Counter



CNT1, 2      Control bits      [Table 1]  
 N1 to N11      Divide ratio setting bits for the programmable counter (3 to 2,047)      [Table 7]  
 A1 to A7      Divide ratio setting bits for the swallow counter (0 to 127)      [Table 8]  
 SW      Divide ratio setting bit for the prescalers (64/65 or 128/129 for the RF1-PLL and RF2-PLL)      [Table 9]  
 PS      Power saving mode control bit      [Table 10]

Note: Input Data with MSB first.

**Table 2. Binary 15-bit Programmable Reference Counter Data Setting**

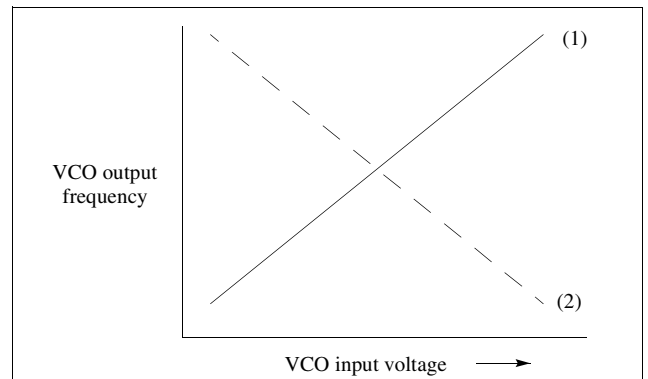
Divide Ratio (R)	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

**Table 3. Phase Comparator Phase Switching Data Setting**

	D <sub>RF1-PLL,RF2-PLL</sub>	
	FC <sub>RF1-PLL,RF2-PLL</sub> = "H"	FC <sub>RF1-PLL,RF2-PLL</sub> = "L"
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	(1)	(2)

Notes: 1) Z = High-impedance  
 2) The FC bit should be set depending upon the VCO and LPF polarity



# Dual PLL Frequency Synthesizer with On-Chip Prescaler

## Functional Descriptions

**Table 4. Charge Pump Current Setting (CMC)**

CMC	Current Value
L	1 x Do
H	4 x Do

**Table 5. Charge Pump Output Impedance Setting (ZC)**

ZC	Do Output Impedance
L	Normal output
H	High impedance

**Table 6. LD/f<sub>OUT</sub> Output Select Data Setting**

LDS <sub>RF1</sub>	LDS <sub>RF2</sub>	FDS <sub>RF1</sub>	FDS <sub>RF2</sub>	LD/f <sub>OUT</sub> Output Signal
L	L	L	L	Disabled
L	H	L	L	LD signal (RF2 lock detect)
H	L	L	L	LD signal (RF1 lock detect)
H	H	L	L	LD signal (RF1/RF2 lock detect)
X	L	L	H	f <sub>OUT</sub> (Output f <sub>RF2</sub> )
X	L	H	L	f <sub>OUT</sub> (Output f <sub>RF1</sub> )
X	H	L	H	f <sub>OUT</sub> (Output f <sub>PRF2</sub> )
X	H	H	L	f <sub>OUT</sub> (Output f <sub>PRF1</sub> )
L	L	H	H	Fastlock
L	H	H	H	RF2 counter reset
H	L	H	H	RF1 counter reset
H	H	H	H	RF1/RF2 counter reset

Note: X = Don't care

**Table 7. Binary 11-bit Programmable Counter Data Setting**

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
...	...	...	...	...	...	...	...	...	...	...	...
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

## Functional Descriptions

**Table 8. Binary 7-bit Swallow Counter Data Setting**

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

**Table 9. Prescaler Data Setting (SW)**

Prescaler Divide Ratio	SW = "L"	SW = "H"
RF1-PLL	64/65	128/129
RF2-PLL	64/65	128/129

### Power-Saving Mode (Intermittent Mode Control)

- The intermittent mode control circuit greatly reduces the PLL power consumption by shutting down various internal functions, as shown in Table 10, depending upon the settings of the power save (PS) bits. Setting the PS bits to "H" enters the corresponding PLL into the power-saving mode. See the Electrical Characteristics chart for the specific value of current when in the power-saving mode.
- The phase detector output, Do, becomes high impedance.
- Serial data can be entered while in the power-saving mode.
- Setting the PS pins "L" releases the power-saving mode, returning the selected PLL to normal operation.

Note: When power ( $V_{CC}$ ) is first applied, the device must be in standby mode, PS = High, for at least 1 $\mu$ s.

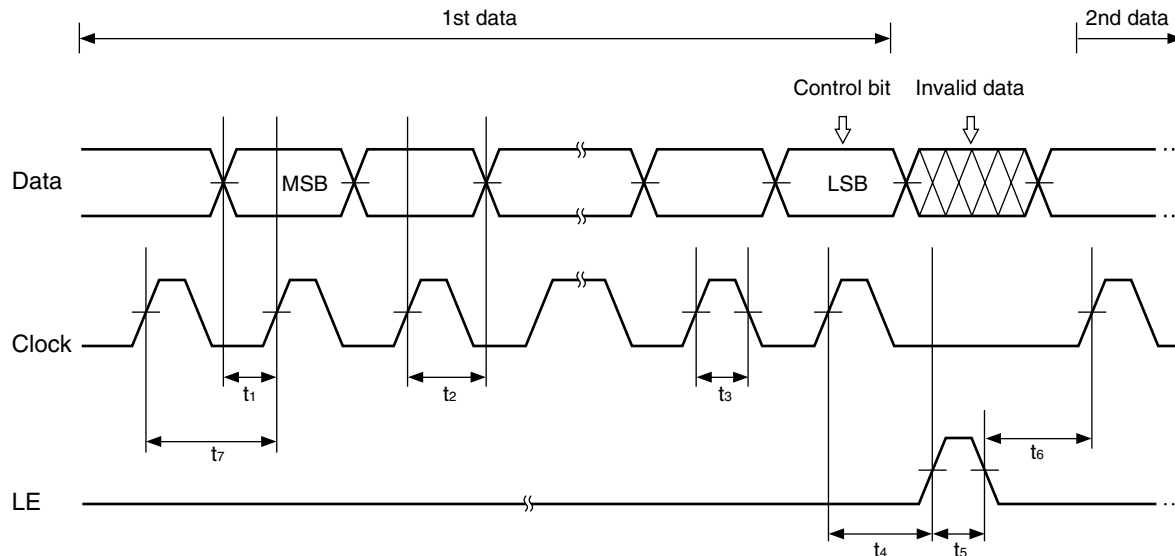
**Table 10. Power Save Internal Shutdown Logic (PS)**

PS <sub>RF2</sub>	PS <sub>RF1</sub>	RF2-PLL Counters	RF1-PLL Counters	OSC Input Buffer
H	H	OFF	OFF	OFF
L	H	ON	OFF	ON
H	L	OFF	ON	ON
L	L	ON	ON	ON



# Dual PLL Frequency Synthesizer with On-Chip Prescaler

## Serial Data Input Timing

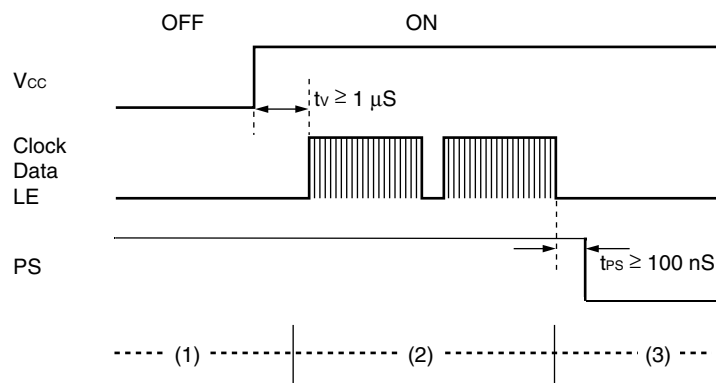


**Table 11. Timing Parameters**

Parameter	Min.	Typ.	Max.	Unit	Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns	t5	100	–	–	ns
t2	20	–	–	ns	t6	20	–	–	ns
t3	30	–	–	ns	t7	100	–	–	ns
t4	30	–	–	ns					

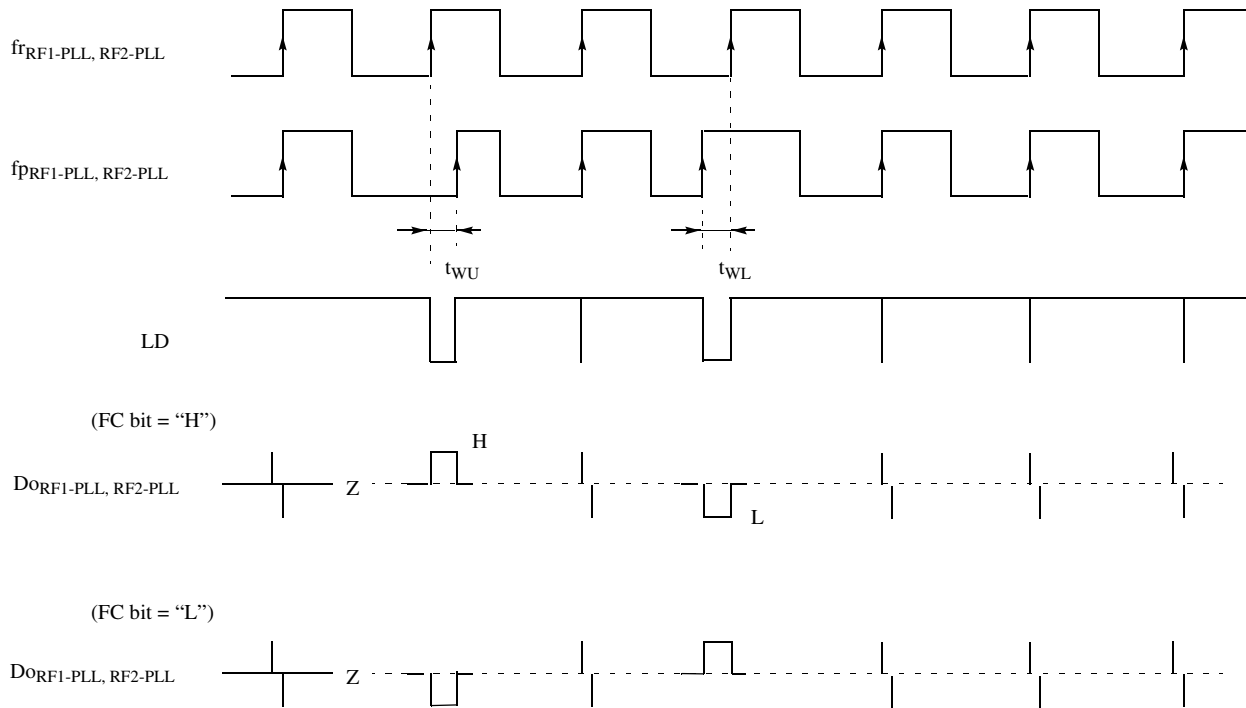
Notes: 1) On the rising edge of the clock, one bit of the data is transferred into the shift register.  
 2) LE should be set to "L" when the data is transferred into the shift register.

## Power-ON Timing



(1) PS = H (power-saving mode) at Power-ON  
 (2) Input serial data 1µs later after power supply remains stable ( $V_{CC} \geq 2.2V$ ).  
 (3) Release power-saving mode (PS: H → L) 100ns later after setting serial data.

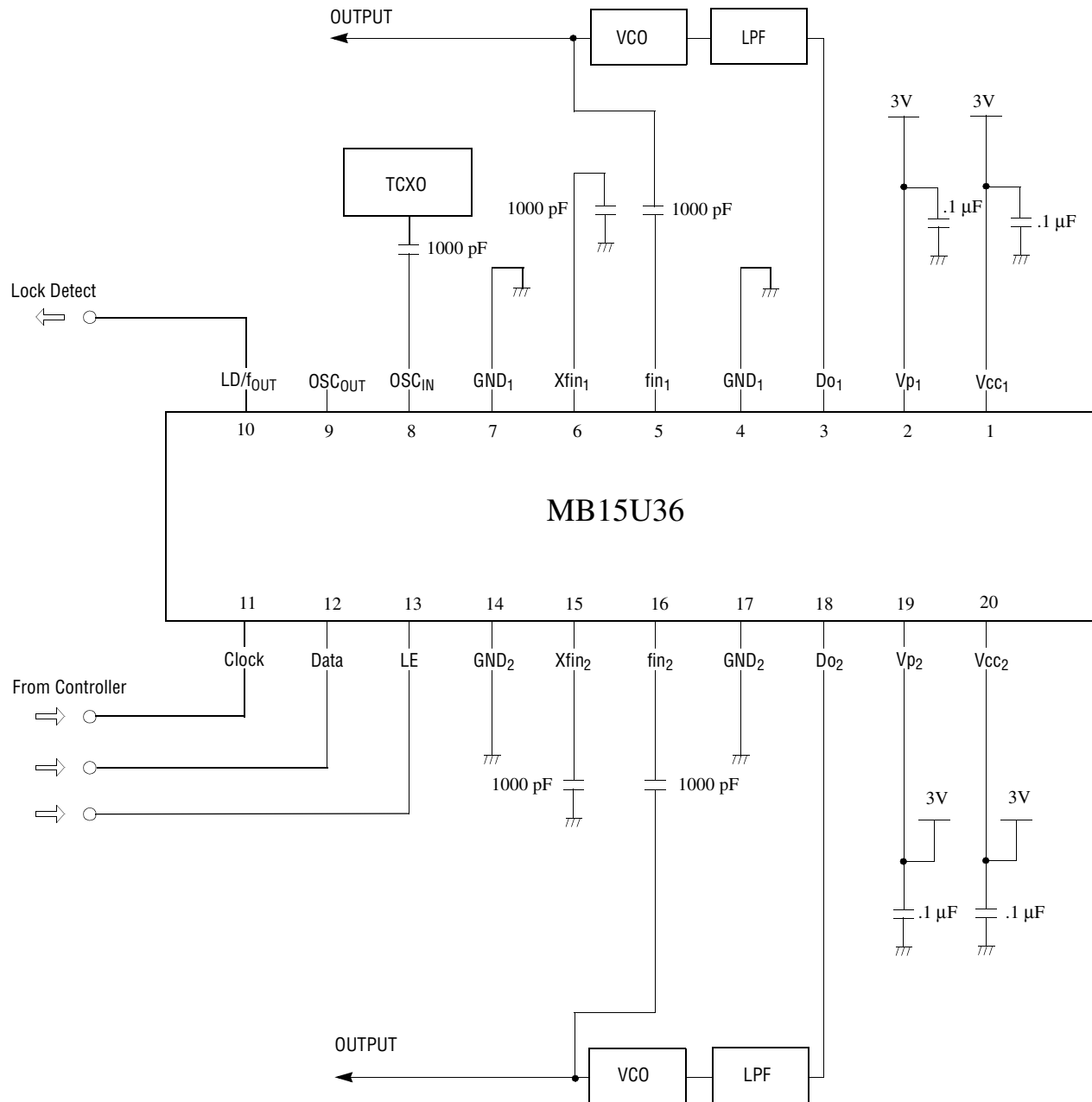
## Phase Detector Output Waveform



- Notes:
- 1) Phase error detection range:  $-2\pi$  to  $+2\pi$
  - 2) Pulses on Do signal during locked state are output to prevent dead zone.

# Dual PLL Frequency Synthesizer with On-Chip Prescaler

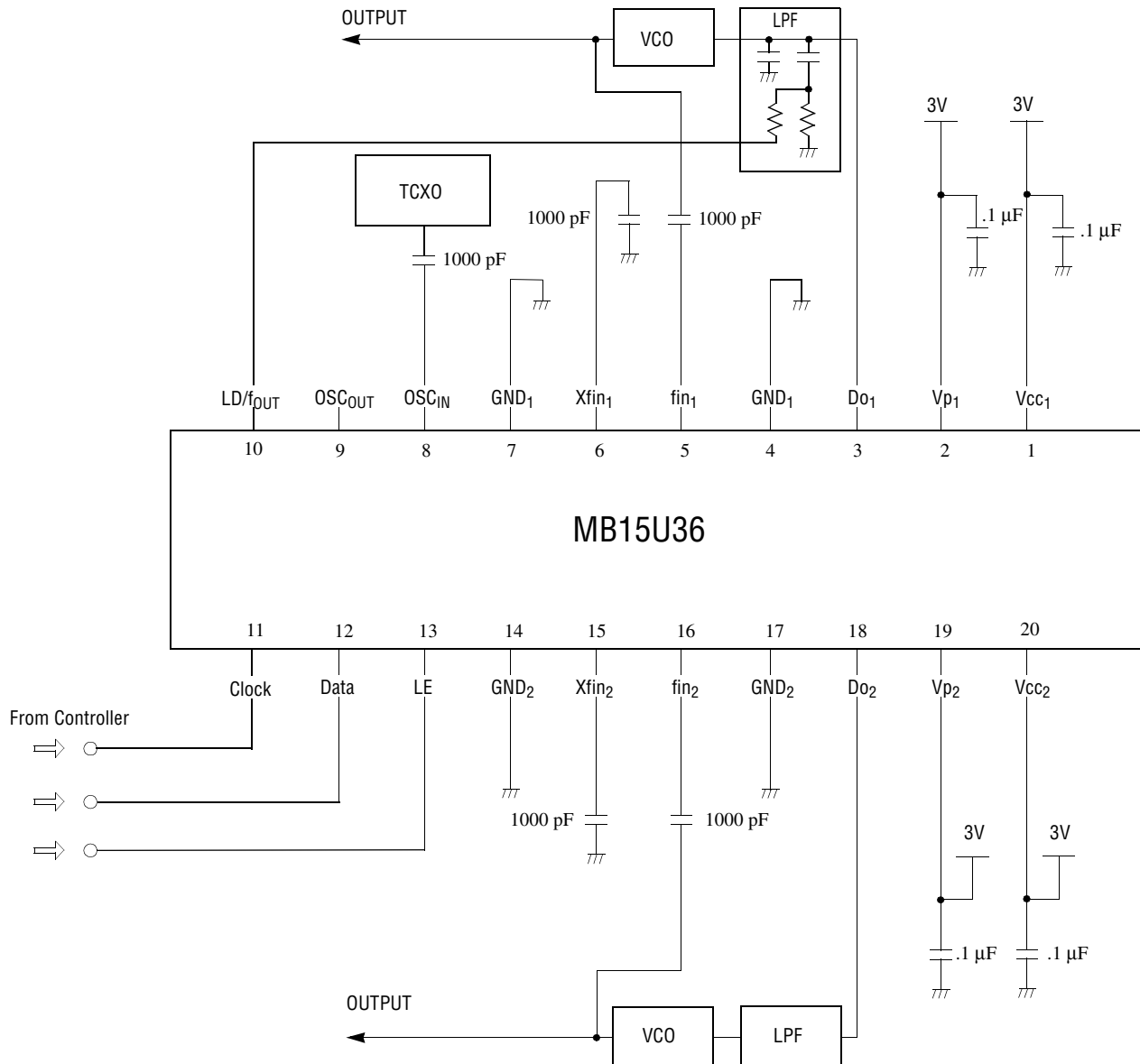
## Application Example



Notes: 1) Package Type: 20-pin SSOP

2) Clock, Data, LE: Insert a pull-down or pull-up resistor as needed to prevent oscillation when the terminals are left open.

## Application Example: Fastlock Mode



Notes: 1) Package Type: 20-pin SSOP

2) Clock, Data, LE: Insert a pull-down or pull-up resistor as needed to prevent oscillation when the terminals are left open

3) The Fastlock mode is controlled by the LDS/FDS bits and the  $CMC_{RF1}$  bit. When the  $CMC_{RF1}$  bit is set to "H" (the RF1 charge pump current is increased 4x normal mode), the LD/fout pin (open drain output) is "L", enabling the parallel resistor in the loop filter. This effectively increases the LPF bandwidth, allowing the loop to lock faster. After the loop has locked onto a new frequency, the  $CMC_{RF1}$  bit is set to "L", forcing the LD/fout output pin into a high impedance state and returning the LPF bandwidth back to its original value.

# Dual PLL Frequency Synthesizer with On-Chip Prescaler

## Usage Precautions

To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet when transporting a board mounted device.

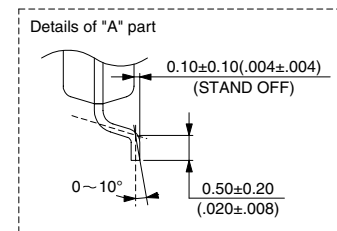
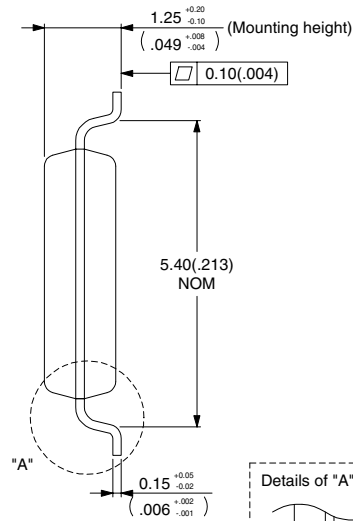
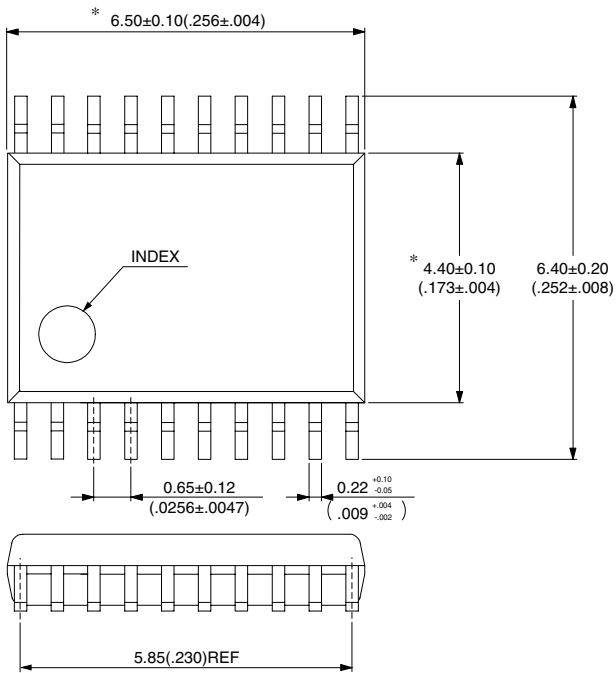
## Ordering Information

Part Number	Package
MB15U36PFV	20-pin, Plastic SSOP (FPT-20P-M03)

## Package Dimensions

20-pin, Plastic SSOP  
(FPT-20P-M03)

\* These dimensions do not include resin protrusion



Dimensions in mm (inches)

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