

### FEATURES

- ±10 V Tracking Outputs
- Kelvin Connections
- Low Tracking Error – 1.5 mV
- Low Initial Error – 2.0 mV
- Low Drift – 1.5 ppm/°C
- Low Noise – 6 μV p-p
- Flexible Output Force and Sense Terminals
- High Impedance Ground Sense
- Machine Insertable DIP Packaging
- MIL-STD-883 Compliant Versions Available

### PRODUCT DESCRIPTION

The AD688 is a high precision ±10 V tracking reference. Low tracking error, low initial error and low temperature drift give the AD688 reference absolute ±10 V accuracy performance previously unavailable in monolithic form. The AD688 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD688 includes the basic reference cell and three additional amplifiers. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high current loads, delivering the full accuracy of the AD688 where it is required in the application circuit.

The low initial error allows the AD688 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD688 can provide a known voltage for system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD688 and calibration software.

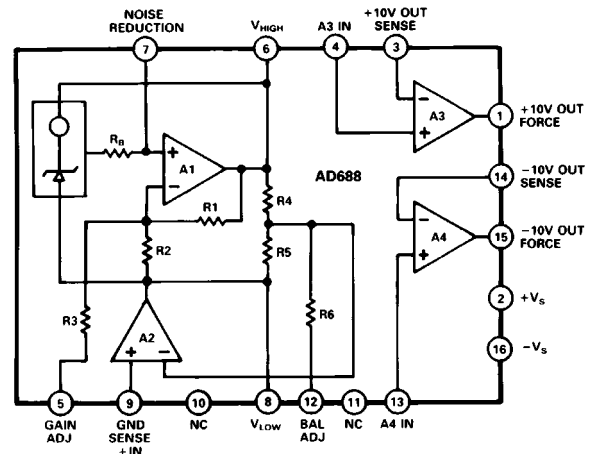
The AD688 is available in three versions. The AD688AQ and BQ grades are packaged in 16-pin cerdip (0.3") packages and are specified for operation from –40°C to +85°C. The AD688SQ grade is specified for operation from –55°C to +125°C.

\*Covered by Patent Number 4,644,253.

### REV. A

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### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT HIGHLIGHTS

1. The AD688 offers precision tracking ±10 V Kelvin output connections with no external components. Tracking error is less than 1.5 mV and a fine-trim is available for applications requiring exact symmetry between the +10 V and –10 V outputs.
2. The AD688 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
3. Output noise of the AD688 is low – typically 6 μV p-p. A pin is provided for broadband noise filtering using an external capacitor.
4. The AD688 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD688/883B data sheet for detailed specifications.

# AD688—SPECIFICATIONS (typical @ +25°C, +10 V output, $V_S = \pm 15$ V unless otherwise noted<sup>1</sup>)

	AD688AQ/SQ			AD688BQ			Units
	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE ERROR +10 V, -10 V Outputs	-5		+5	-2		+2	mV
±10 V TRACKING ERROR	-3		+3	-1.5		+1.5	mV
OUTPUT VOLTAGE DRIFT +10 V, -10 V Outputs 0°C to +70°C (A, B) -40°C to +85°C (A, B) -55°C to +125°C (S)		±2		-1.5 -3		+1.5 +3	ppm/°C ppm/°C ppm/°C
GAIN ADJ AND BAL ADJ <sup>2</sup> Trim Range Input Resistance		±5 150			±5 150		mV kΩ
LINE REGULATION $T_{MIN}$ to $T_{MAX}$ <sup>3</sup>	-200		+200	-200		+200	μV/V
LOAD REGULATION $T_{MIN}$ to $T_{MAX}$ +10 V Output, $0 < I_{OUT} < 10$ mA -10 V Output, $-10 < I_{OUT} < 0$ mA			±50 ±50			±50 ±50	μV/mA μV/mA
SUPPLY CURRENT $T_{MIN}$ to $T_{MAX}$ Power Dissipation		9 270	12 360		9 270	12 360	mA mW
OUTPUT NOISE (ANY OUTPUT) 0.1 Hz to 10 Hz Spectral Density, 100 Hz		6 140			6 140		μV p-p nV√Hz
LONG TERM STABILITY (@ +25°C)		15			15		ppm/1000 hours
BUFFER AMPLIFIERS Offset Voltage Offset Voltage Drift Bias Current Open Loop Gain Output Current A3, A4 Common Mode Rejection (A3, A4) $V_{CM} = 1$ V p-p Short-Circuit Current		100 1 20 110 -10 100 50			100 1 20 110 -10 100 50		μV μV/°C nA dB mA dB mA
TEMPERATURE RANGE Specified Performance A, B Grades S Grade		-40 -55	+85 +125		-40	+85	°C °C °C

## NOTES

<sup>1</sup>See Figure 2a for output configuration. Specifications tested using +10 V output unless otherwise indicated.

<sup>2</sup>Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

<sup>3</sup>Test Condition:  $+V_S = +18$  V,  $-V_S = -18$  V;  $+V_S = +13.5$  V,  $V_S = -13.5$  V.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

$+V_S$  to  $-V_S$  ..... 36 V

Power Dissipation (+25°C)

Q Package ..... 600 mW

Storage Temperature ..... -65°C to +150°C

Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Package Thermal Resistance

Q ( $\theta_{JA}/\theta_{JC}$ ) ..... 120/35°C/W

Output Protection: All outputs safe if shorted to ground

\*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ORDERING GUIDE

Part Number <sup>1</sup>	Initial Error	Temperature Coefficient	Temperature Range - °C	Package Option <sup>2</sup>
AD688AQ	5 mV	3 ppm/°C	-40 to +85	Q-16
AD688BQ	2 mV	3 ppm/°C	-40 to +85*	Q-16
AD688SQ	5 mV	6 ppm/°C	-55 to +125	Q-16

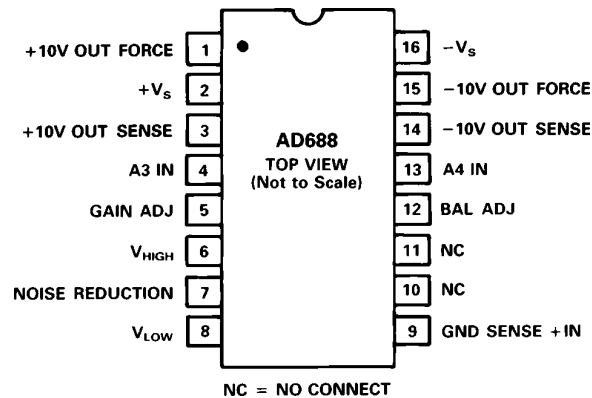
### NOTES

<sup>1</sup>For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the *Analog Devices Military Products Databook* or current AD688/883B data sheet.

<sup>2</sup>Q = Cerdip.

\*Temperature coefficient specified from 0 to +70°C.

## PIN CONFIGURATION



## THEORY OF OPERATION

The AD688 consists of a buried Zener diode reference, amplifiers and associated thin-film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5 ppm/°C or less.

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage to the required 20 volts. In addition, A1 also provides for external adjustment of the 20 V output through Pin 5, the GAIN ADJUST. Using the bias compensation resistor between the Zener output and the noninverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (Pin 7) to form a low pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 12 kΩ nominal thin-film resistors (R4 and R5) divide the 20 V output in half.

Ground sensing for the circuit is provided by Amplifier A2. The noninverting input (Pin 9) senses the system ground and forces the midpoint of resistors R4 and R5 to be a virtual ground. Pin 12 (BALANCE ADJUST) can be used for fine adjustment of this midpoint transfer.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at Pins 6 and 8 as well as to provide a full Kelvin output. Thus, the AD688 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

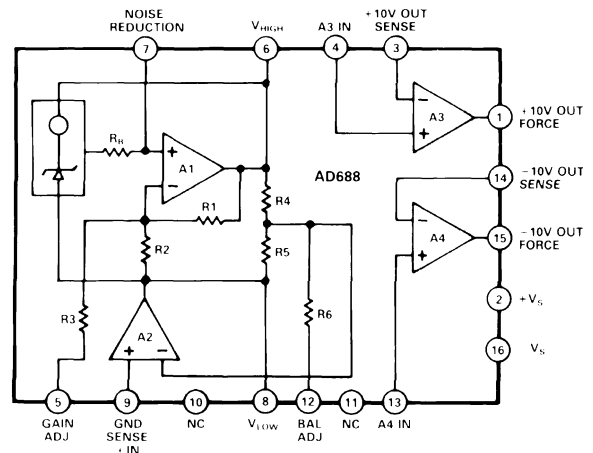


Figure 1. AD688 Functional Block Diagram

# AD688

## APPLYING THE AD688

The AD688 can be configured to provide  $\pm 10$  V reference outputs as shown in Figure 2a. The architecture of the AD688 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD688 is specified and tested in the configuration shown in Figure 2a. The user may choose to take advantage of other configuration options available with the AD688; however performance in these configurations is not guaranteed to meet the stringent data sheet specifications.

Unbuffered outputs are available at Pins 6 and 8. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD688 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 2a. When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage polarity may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on Pin 6 or 8. Performance in these dual output configurations will typically meet data sheet specifications.

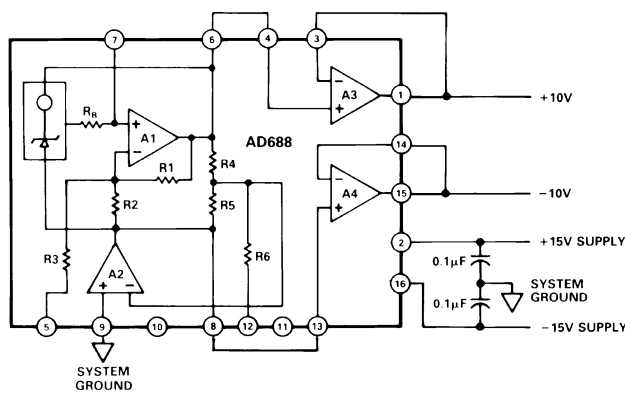


Figure 2a. +10 V and -10 V Outputs

## CALIBRATION

Generally, the AD688 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 2 mV and output noise specs of 6  $\mu$ V p-p allow for accuracies of 12-16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. The provision for trimming has been made through the use of the GAIN ADJUST and BALANCE ADJUST pins (Pins 5 and 12, respectively).

The AD688 provides a precision 20 V span with a center tap which is used with the buffer and ground sense amplifiers to achieve the  $\pm 10$  V output configuration. The GAIN ADJUST and BALANCE ADJUST can be used to trim the magnitude of the 20 V span voltage and the position of the center tap within the span. The GAIN ADJUST should be performed first. Although the trims are not interactive within the device, the GAIN trim will move the BALANCE trim point as it changes the magnitude of the span.

Figure 2b shows the GAIN and BALANCE trims of the AD688. A 100 k $\Omega$  20-turn potentiometer is used for each trim. The potentiometer for the GAIN trim is connected between Pins 6 ( $V_{HIGH}$ ) and 8 ( $V_{LOW}$ ) with the wiper connected to Pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly

20 V between Pins 1 and 15, the amplifier outputs. The BALANCE potentiometer, also connected between Pins 6 and 8 with the wiper to Pin 12 (BAL ADJ), is then adjusted to center the span from +10 V to -10 V.

Input impedance on both the GAIN ADJUST and the BALANCE ADJUST pins is approximately 150 k $\Omega$ . The GAIN ADJUST trim network effectively attenuates the 20 V across the trim potentiometer by a factor of about 1150 to provide a trim range of -5.8 mV to +12.0 mV with a resolution of approximately 900  $\mu$ V/turn (20 turn potentiometer). The BALANCE ADJUST trim network attenuates the trim voltage by a factor of about 1250, providing a trim range of  $\pm 8$  mV with a resolution of 800  $\mu$ V/turn.

Trimming the AD688 introduces no additional errors over temperature, so precision potentiometers are not required.

In cases when BALANCE ADJUST is not necessary, Pin 12 should be left floating. If GAIN ADJUST is not required, Pin 5 should also be left floating.

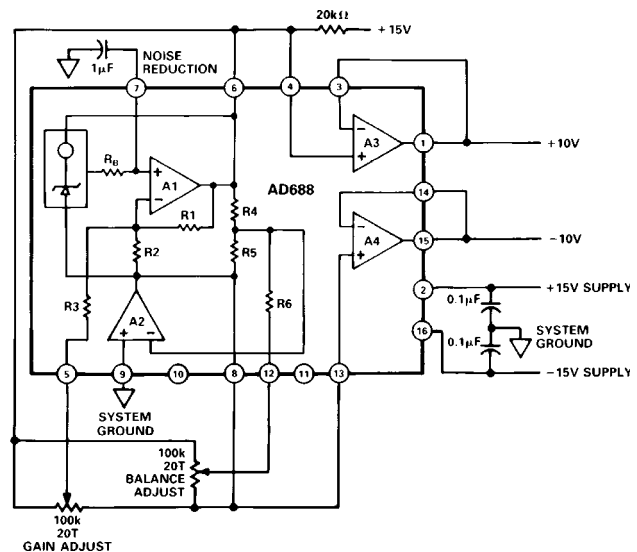


Figure 2b. Gain and Balance Adjust with Noise Reduction

## NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD688 is typically less than 6  $\mu$ V p-p over the 0.1 Hz to 10 Hz band. Noise in a 1 MHz bandwidth is approximately 840  $\mu$ V p-p. The dominant source of this noise is the buried Zener which contributes approximately 140 nV/ $\sqrt{\text{Hz}}$ . In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1 Hz to 10 Hz noise of a typical AD688.

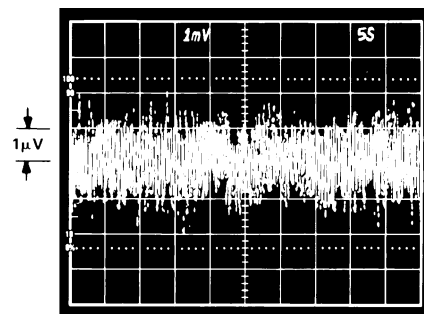


Figure 3. 0.1 Hz to 10 Hz Noise

If further noise reduction is desired, an optional capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2b. This will form a low pass filter with the 5 kΩ R<sub>B</sub> on the output of the Zener cell. A 1 μF capacitor will have a 3 dB point at 32 Hz and will reduce the high frequency noise (to 1 MHz) to about 250 μV p-p. Figure 4 shows the 1 MHz noise of a typical AD688 both with and without a 1 μF capacitor.

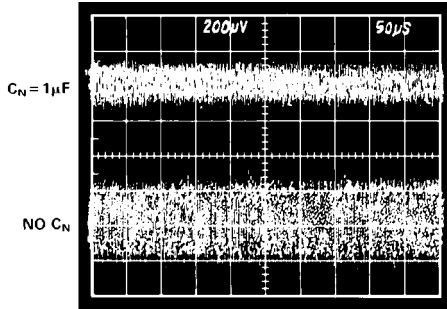
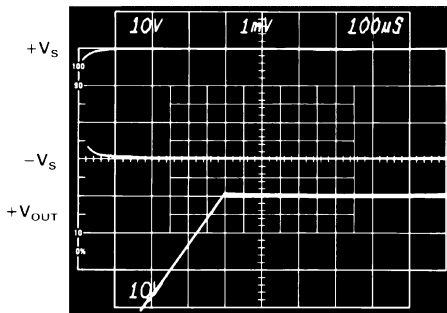


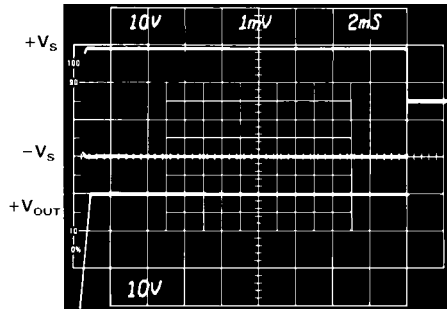
Figure 4. Effect of 1 μF Noise Reduction Capacitor on Broadband Noise

**TURN-ON TIME**

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error is the turn-on settling time. Two components normally associated with this are: time for active circuits to settle and time for thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD688. It shows the settling time to be about 600 μs. Note the absence of any thermal tails when the horizontal scale is expanded to 2 ms/cm in Figure 5b.



a. Electrical Turn-On



b. Extended Time Scale

Figure 5. Turn-On Characteristics

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1 μF capacitor, the initial turn-on time is approximately 100 ms (see Figure 6).

When the NOISE REDUCTION feature is used, a 20 kΩ resistor between Pins 6 and 2 is required for proper startup.

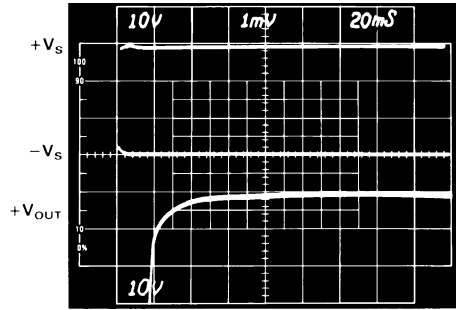


Figure 6. Turn-On With 1 μF C<sub>N</sub>

**TEMPERATURE PERFORMANCE**

The AD688 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 7 shows the typical output voltage drift for the AD688SQ and illustrates the test methodology. The box in Figure 7 is bounded on the sides by the operating temperature extremes and on top and bottom by the maximum and minimum +10 V output error voltages measured over the operating temperature range. The slopes of the diagonals drawn for both the +10 V and -10 V outputs determine the performance grade of the device.

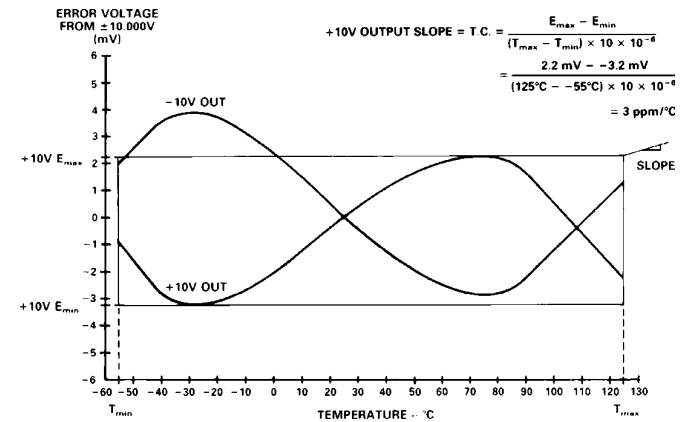


Figure 7. Typical AD688SQ Temperature Drift

Each AD688A and B grade unit is tested at -40°C, -25°C, 0°C, +25°C, +50°C, +70°C and +85°C. Each AD688S grade unit is tested at -55°C, -25°C, +25°C, +70°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 8.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE mV	
	0 TO +70°C	-40°C TO +85°C -55°C TO +125°C
AD688AQ	1.40 (typ)	3.75
AD688BQ	1.05	3.75
AD688SQ		10.80

Figure 8. Maximum +10 V or -10 V Output Change

# AD688

Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD688 will produce curves similar to those in Figure 7, but output readings may vary depending on the test methods and equipment utilized.

## KELVIN CONNECTIONS

Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 9a, the load

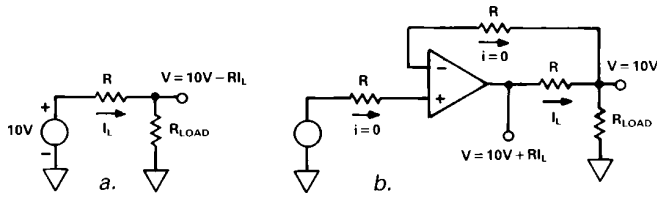


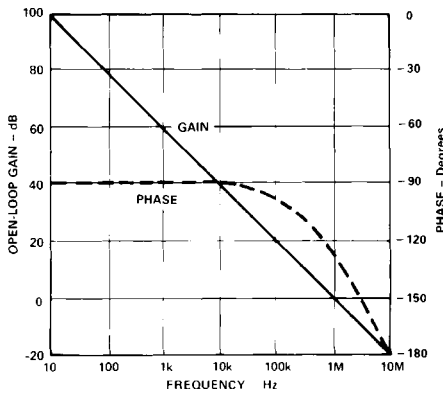
Figure 9. Advantage of Kelvin Connection

current and wire resistance produce an error ( $V_{ERROR} = R \times I_L$ ) at the load. The Kelvin connection of Figure 9b overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 volts +  $V_{ERROR}$  and the voltage at the load would be the desired 10 volts.

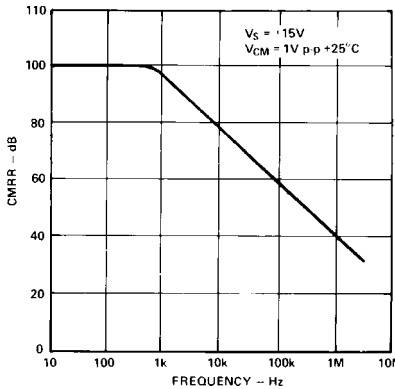
The AD688 has three amplifiers which can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function while uncommitted amplifiers A3 and A4 are free for other force-sense chores.

In some applications, one amplifier may be unused. In such cases, the unused amplifier should be connected as a unity-gain follower (force and sense pins tied together) and the input should be connected to ground.

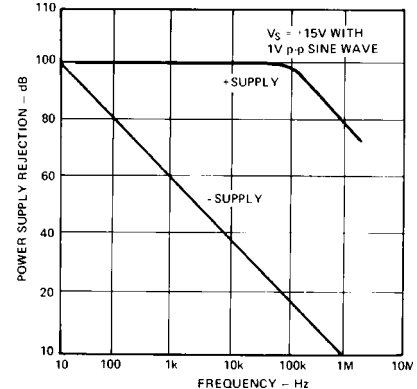
An unused amplifier may be used for other circuit functions as well. The curves on this page show the typical performance of A3 and A4.



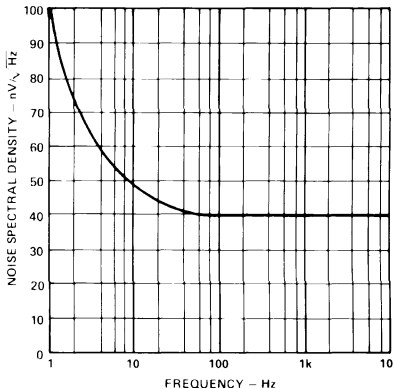
A3, A4 Open-Loop Frequency Response



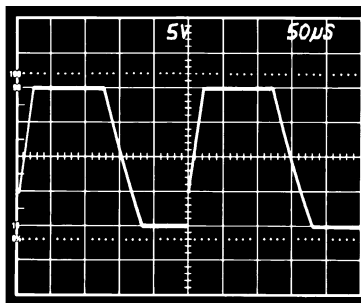
A3, A4 CMR vs. Frequency



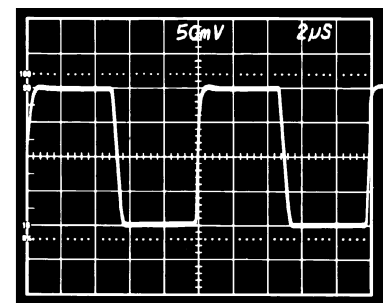
A3, A4 PSR vs. Frequency



Input Noise Voltage Spectral Density



Unity-Gain Follower Pulse Response (Large Signal)



Unity-Gain Follower Pulse Response (Small Signal)

## DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD688 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 10 displays the characteristic of the AD688 output amplifier driving a 0-to-10 mA load.

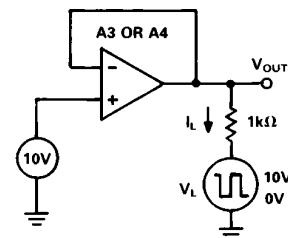


Figure 10a. Transient Load Test Circuit



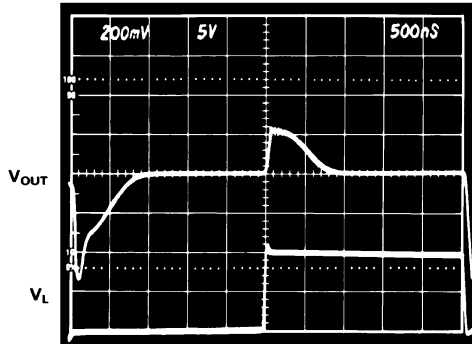


Figure 10b. Large-Scale Transient Response

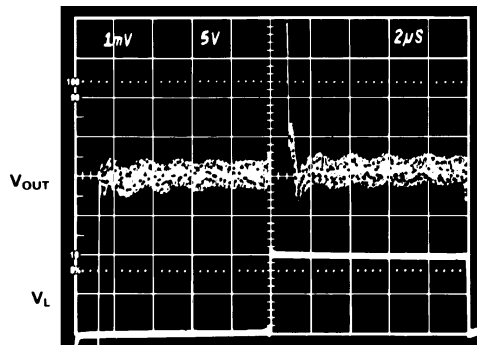


Figure 10c. Fine-Scale Settling for Transient Load

Figure 11 displays the output amplifier characteristic driving a 5 mA-to-10 mA load, a common situation found when the reference is shared among multiple converters or is used to provide bipolar offset current.

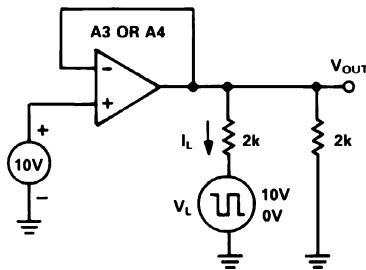


Figure 11a. Transient and Constant Load Test Circuit

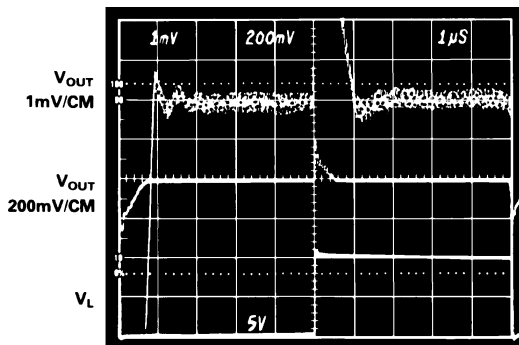


Figure 11b. Transient Response 5-10 mA Load

In some applications, a varying load may be both resistive and capacitive in nature, or be connected to the AD688 by a long capacitive cable. Figure 12 displays the output amplifier characteristics driving a 1,000 pF, 0-to-10 mA load.

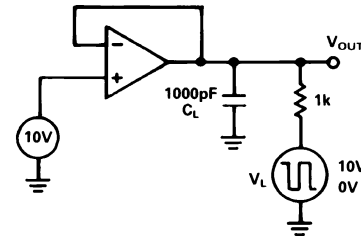


Figure 12a. Capacitive Load Transient Response Test Circuit

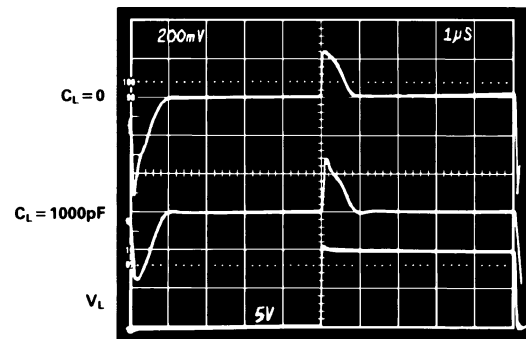


Figure 12b. Output Response with Capacitive Load

Figure 13 displays the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 volts, while the output of A3 is subjected to a 0-to-10 mA load current step. The transient at A4 settles in about 1 µs, and the load-induced offset is about 100 µV.

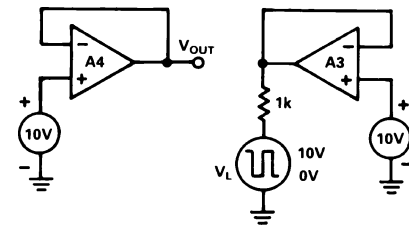


Figure 13a. Load Crosstalk Test Circuit

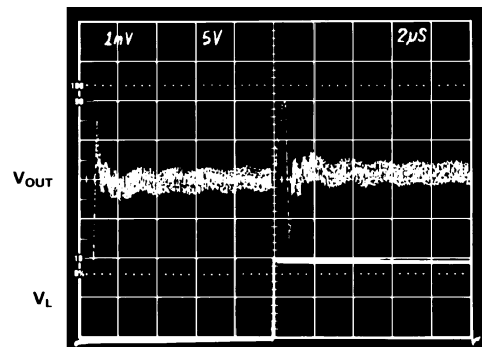


Figure 13b. Load Crosstalk

# AD688

Attempts to drive a large capacitive load (in excess of 1,000 pF) may result in ringing or oscillation, as shown in the step response photo (Figure 14a). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin. The recommended method of driving capacitive loads of this magnitude is shown in Figure 14b. The 150 Ω resistor isolates the capacitive load from the output stage, while the 10 kΩ resistor provides a dc feedback path and preserves the output accuracy. The 1 μF capacitor provides a high frequency feedback loop. The performance of this circuit is shown in Figure 14c.

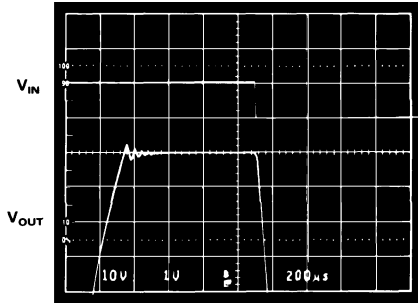


Figure 14a. Output Amplifier Step Response,  $C_L = 1 \mu F$

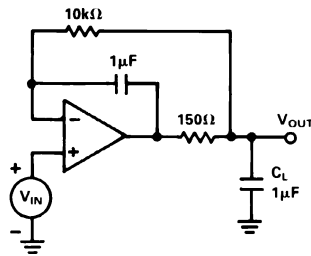


Figure 14b. Compensation for Capacitive Loads

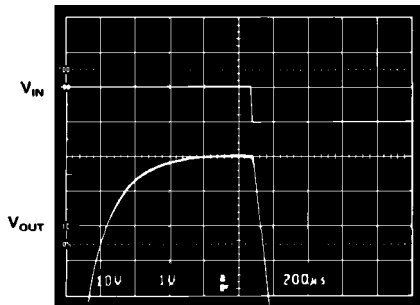


Figure 14c. Output Amplifier Step Response Using Figure 14b Compensation

## BRIDGE DRIVER CIRCUIT

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of 4 two-terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal.

In this unipolar drive configuration, the output voltage of the bridge is riding on a common-mode voltage signal equal to approximately  $V_{IN}/2$ . Further processing of this signal may necessarily be limited to high common-mode rejection techniques such as instrumentation or isolation amplifiers. However, if the bridge is driven from a pair of bipolar supplies, then the common-mode voltage is ideally eliminated and the restrictions on any processing elements that follow are relaxed.

As shown in Figure 15, the AD688 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistors Q1 and Q2 serve as series pass elements to boost the current drive capability to the 57 mA required by the typical 350 Ω bridge. A differential gain stage may still be required if the bridge balance is not perfect.

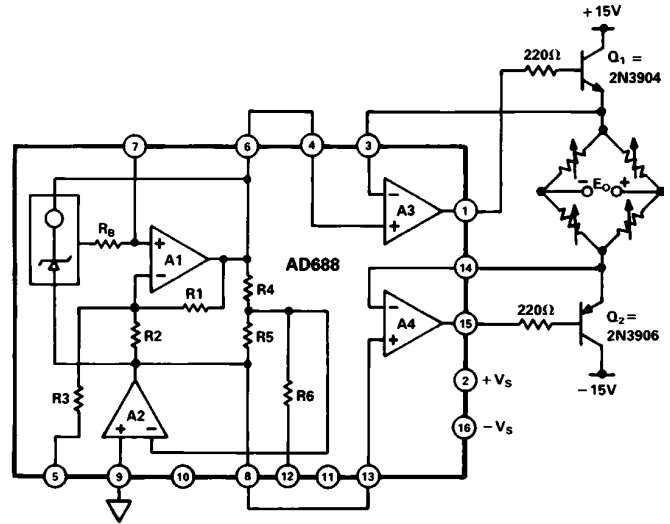


Figure 15. Bipolar Bridge Drive

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

