

**Description**

Available in PGA (Puma 2), JLCC (Puma 67) and Gullwing (Puma 77) footprints, the Puma \*\*E4001 is a 4 Mbit EEPROM module user configurable as 128K x 32, 256K x 16 or 512K x 8. Available with access times of 120, 150 and 200ns, the device features hardware and software data protection, 10,000 cycle Write/Erase capability and 10 year data retention time.

An option of independant (A version) or single  $\overline{WE}$  control is available.

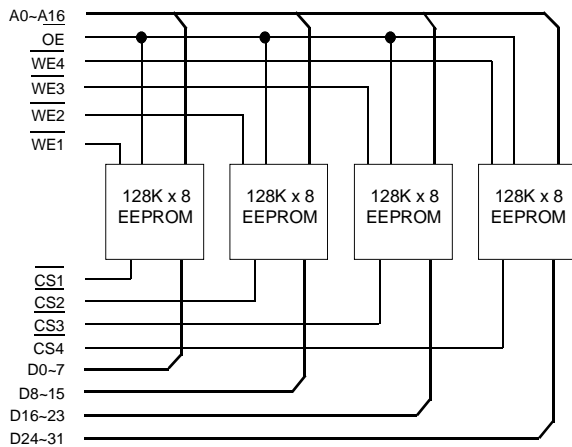
Parts may be screened in accordance with MIL-STD-883

**Features**

- 4 Megabit EEPROM module.
- Access Times of 120/150/200 ns.
- Output Configurable as 32/ 16/ 8 bit wide.
- Upgradeable footprint
- Operating Power 1600/ 830/ 445 mW (Max).  
Low Power Standby 2.2 mW (Max).
- Byte and Page Write (128 Bytes) in 5ms typical with DATA Polling and Toggle bit indication of end of Write.
- Hardware and Software Data Protection.
- Puma 2 - 66 pin Ceramic PGA.
- Puma 67 - 68 Lead Ceramic JLCC.
- Puma 77 - 68 Lead Ceramic Gullwing.
- May be screened in accordance with MIL-STD-883.
- 100,000 W/E cycle endurance option

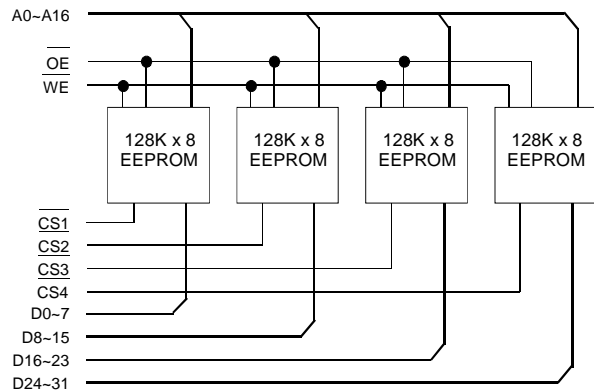
**Block Diagram**

PUMA 2E4001, 67E4001A and 77E4001A



**Block Diagram**

PUMA 67E4001 and 77E4001



**Pin Functions**

**A0~A16** Address Input  
**CS1~4** Chip Select  
 **$\overline{OE}$**  Output Enable  
**GND** Ground

**D0~D31** Data Inputs/Outputs  
**WE1~4** Write Enables  
**Vcc** Power (+5V)

**DC OPERATING CONDITIONS****Absolute Maximum Ratings** <sup>(1)</sup>

Operating Temperature	$T_{OPR}$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	$V_{IN}$	-0.6 to +6.25	V
Output voltages with respect to GND	$V_{OUT}$	-0.6 to $V_{CC}+0.6$	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

		<i>min</i>	<i>typ</i>	<i>max</i>	
DC Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input Low Voltage	$V_{IL}$	-1.0	-	0.8	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{CC}+1$	V
Operating Temp Range	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C (I Suffix)
	$T_{AM}$	-55	-	125	°C (M, MB Suffix)

**DC Electrical Characteristics** ( $T_A=-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC}=5\text{V} \pm 10\%$ )

Parameter	Symbol	Test Condition	<i>min</i>	<i>max</i>	Unit
Input Leakage Current	$I_{LI1}$	$V_{IN} = \text{GND to } V_{CC}+1$	-	40	$\mu\text{A}$
Output Leakage Current	32 bit $I_{LO}$	$V_{IO} = \text{GND to } V_{CC}$ , $\overline{\text{CS}}^{(1)}=V_{IH}$	-	40	$\mu\text{A}$
Operating Supply Current	32 bit $I_{CC32}$	$\overline{\text{CS}}^{(1)}=\overline{\text{OE}}=V_{IL}$ , $\overline{\text{WE}}=V_{IH}$ , $I_{OUT}=0\text{mA}$ , $f=5\text{MHz}^{(2)}$	-	320	mA
	16 bit $I_{CC16}$	As above	-	166	mA
	8 bit $I_{CC8}$	As above	-	89	mA
Standby Supply Current	TTL levels $I_{SB1}$	$\overline{\text{CS}}^{(1)} = 2.0\text{V to } V_{CC}+1\text{V}$	-	12	mA
	CMOS levels $I_{SB2}$	$\overline{\text{CS}}^{(1)} = V_{CC}-0.3\text{V to } V_{CC}+1\text{V}$	-	1.2	mA
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$ .	-	0.45	V
Output High Voltage	$V_{OH}$	$I_{OH} = -400\mu\text{A}$ .	2.4	-	V

Notes (1)  $\overline{\text{CS}}$  above are accessed through  $\overline{\text{CS}}1\sim4$ . These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Also for  $\overline{\text{WE}}1\sim4$  on the PUMA 2E4001, 67E4001A, 77E4001A versions. Additionally,  $\overline{\text{WE}}1\sim4$  are accessed as in note (1) above.

**Capacitance** ( $T_A=25^{\circ}\text{C}$ ,  $f=1\text{MHz}$ ) Note: These parameters are calculated, not measured.

Parameter	Symbol	Test Condition	<i>typ</i>	<i>max</i>	Unit
Input Capacitance	$\overline{\text{CS}}1\sim4$ , $\overline{\text{WE}}1\sim4^{(1)}$	$C_{IN1}$ $V_{IN}=0\text{V}$	-	20	pF
	Other Inputs	$C_{IN2}$ $V_{IN}=0\text{V}$	-	22	pF
Output Capacitance	$C_{OUT}$	$V_{OUT}=0\text{V}$	-	22	pF

Notes: (1) On the PUMA 2E4001, 67E4001A, 77E4001A versions only.

**AC OPERATING CONDITIONS****Read Cycle**

Parameter	Symbol	12		15		20		Unit
		min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	120	-	150	-	200	-	ns
Address Access Time	$t_{AA}$	-	120	-	150	-	200	ns
Chip Select Access Time	$t_{CS}$	-	120	-	150	-	200	ns
Output Enable Access Time	$t_{OE}$	0	60	0	70	0	80	ns
$\overline{CS}$ or $\overline{OE}$ to Output Float (2)	$t_{DF}$	0	60	0	70	0	80	ns
Output Hold from Address Change	$t_{OH}$	0	-	0	-	0	-	ns

Notes: (1)  $t_{HZ}$  max. and  $t_{OLZ}$  max. are measured with  $CL = 5pF$ , from the point when Chip Select or Output Enable return high (whichever occurs first) to the time when the outputs are no longer driven.  $t_{HZ}$  and  $t_{OHZ}$  are shown for reference only: they are characterized and not tested.

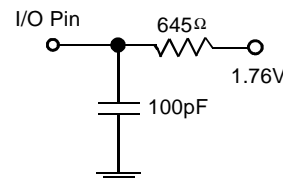
(2) This parameter is characterised and is not 100% tested.

**Write Cycle**

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	$t_{WC}$	-	-	10	ms
Address Set-up Time	$t_{AS}$	0	-	-	ns
Address Hold Time	$t_{AH}$	50	-	-	ns
Output Enable Set-up Time	$t_{OES}$	0	-	-	ns
Output Enable Hold Time	$t_{OEH}$	0	-	-	ns
Chip Select Set-up Time	$t_{CS}$	0	-	-	ns
Chip Select Hold Time	$t_{CH}$	0	-	-	ns
Write Pulse Width	$t_{WP}$	100	-	-	ns
Write Enable High Recovery	$t_{WPH}$	50	-	-	ns
Data Set-up Time	$t_{DS}$	50	-	-	ns
Data Hold Time	$t_{DH}$	0	-	-	ns
Byte Load Cycle	$t_{BLC}$	-	-	150	$\mu s$

**AC Test Conditions**

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 10ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: 1 TTL gate + 100pF
- \*  $V_{CC} = 5V \pm 10\%$

**Output Test Load**

**Data Polling Characteristics (1)**

<i>Parameter</i>	<i>Symbol</i>	<i>min</i>	<i>typ</i>	<i>max</i>	<i>Unit</i>
Data Hold Time	$t_{DH}$	10	-	-	ns
$\overline{OE}$ Hold Time	$t_{OE\overline{H}}$	10	-	-	ns
$\overline{OE}$ to Output Delay (2)	$t_{OE}$	-	-	-	ns
Write Recovery Time	$t_{WR}$	0	-	-	ns

Notes: (1) These parameter are characterised and is not 100% tested.

(2) See AC Read Characteristics.

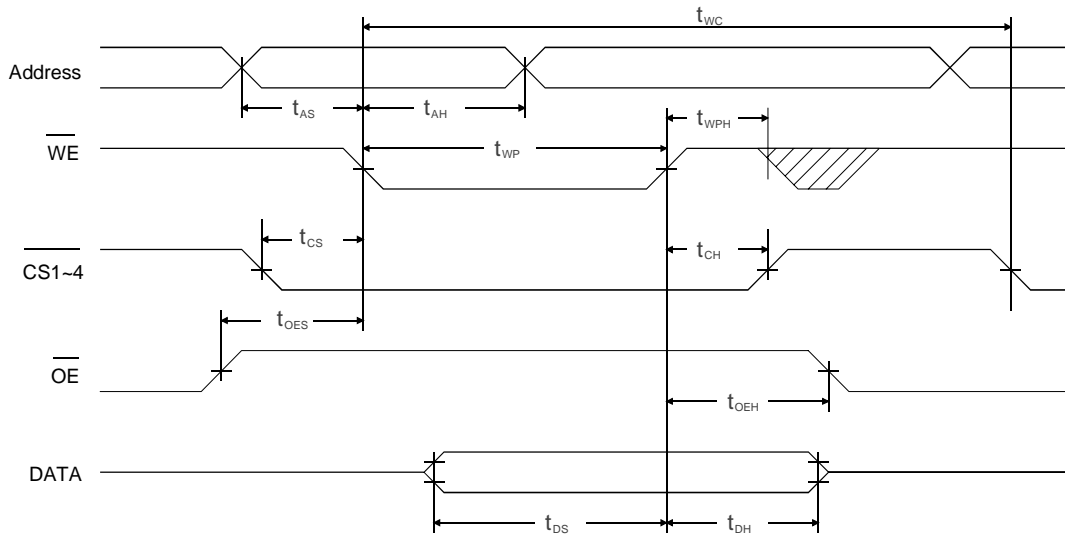
**Toggle Bit Characteristics (1)**

<i>Parameter</i>	<i>Symbol</i>	<i>min</i>	<i>typ</i>	<i>max</i>	<i>Unit</i>
Data Hold Time	$t_{DH}$	10	-	-	ns
$\overline{OE}$ Hold Time	$t_{OE\overline{H}}$	10	-	-	ns
$\overline{OE}$ to Output Delay (2)	$t_{OE}$	-	-	-	ns
OE High Pulse	$t_{OEHP}$	150	-	-	ns
Write Recovery Time	$t_{WR}$	0	-	-	ns

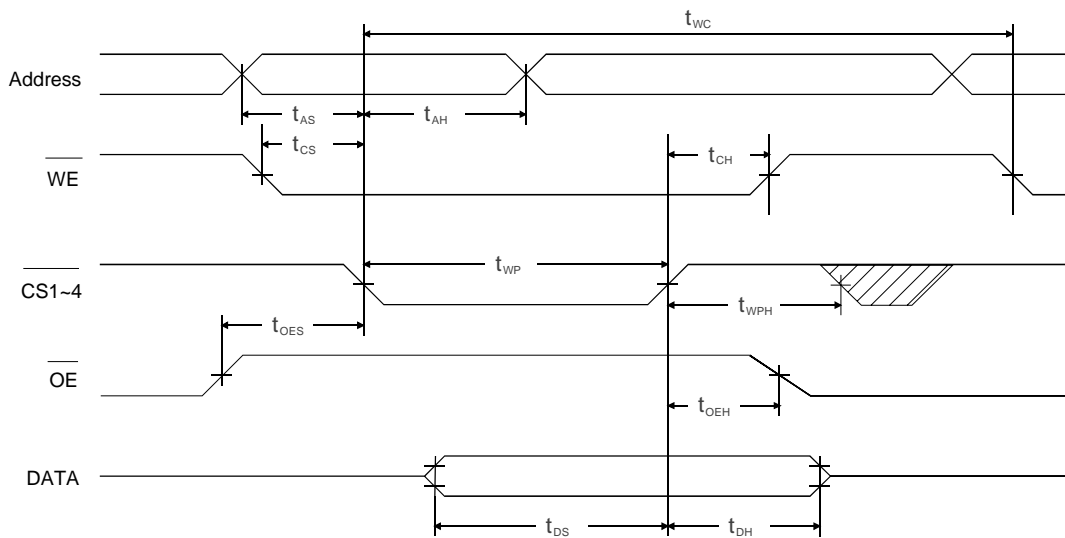
Notes: (1) These parameter are characterised and is not 100% tested.

(2) See AC Read Characteristics.

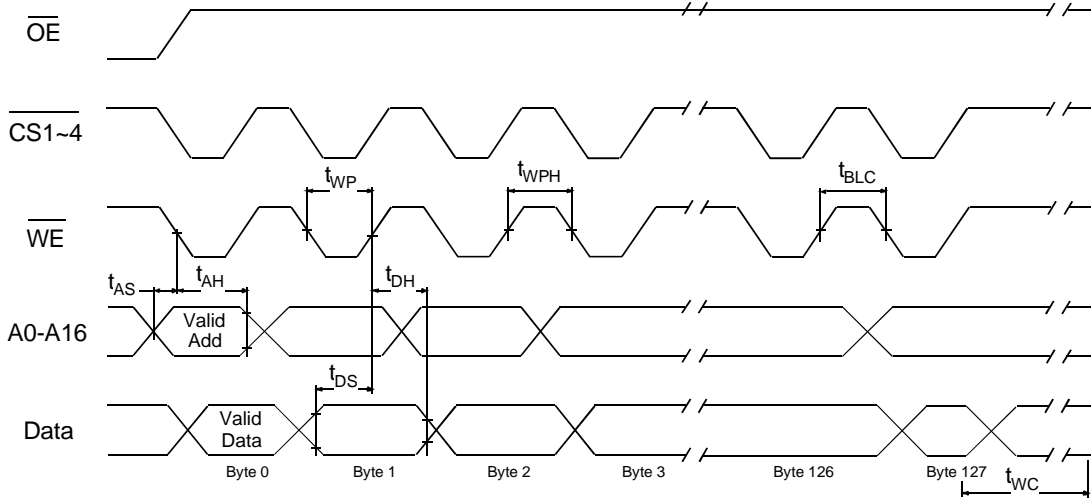
**AC Write Waveform -  $\overline{\text{WE}}$  Controlled**



**AC Write Waveform -  $\overline{\text{CS}}$  Controlled**

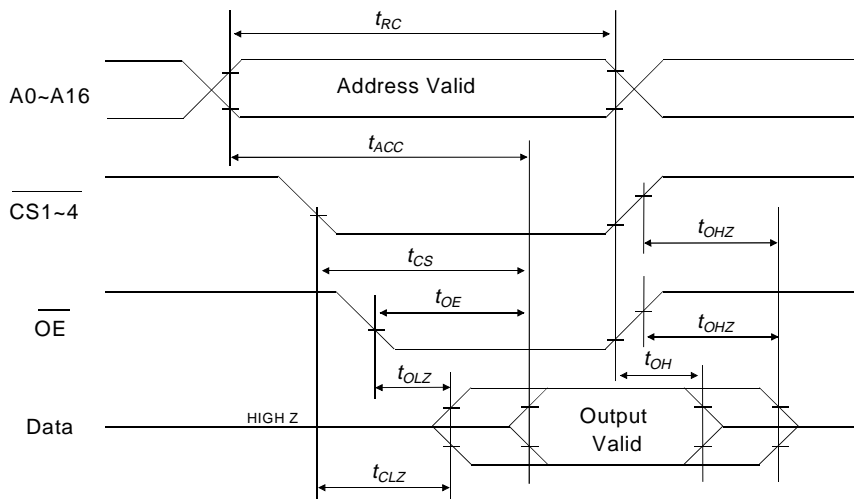


**Page Mode Write Waveform**

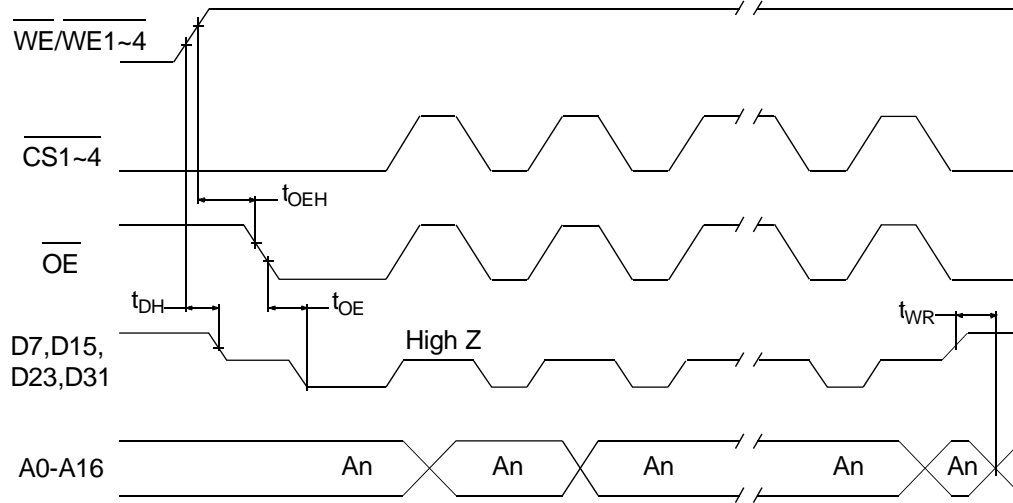


Note: A8 through A16 must specify the page address during each high to low transition of Write Enable (or Chip select). Output Enable must be high only when Write Enable and Chip Select are both low.

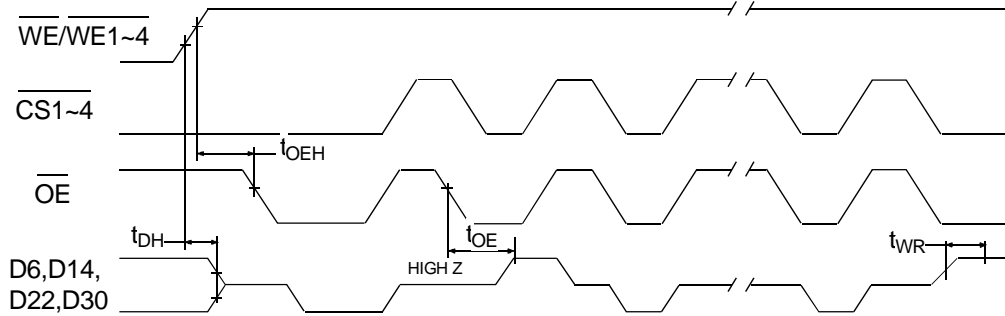
**Read Cycle Timing Waveform**



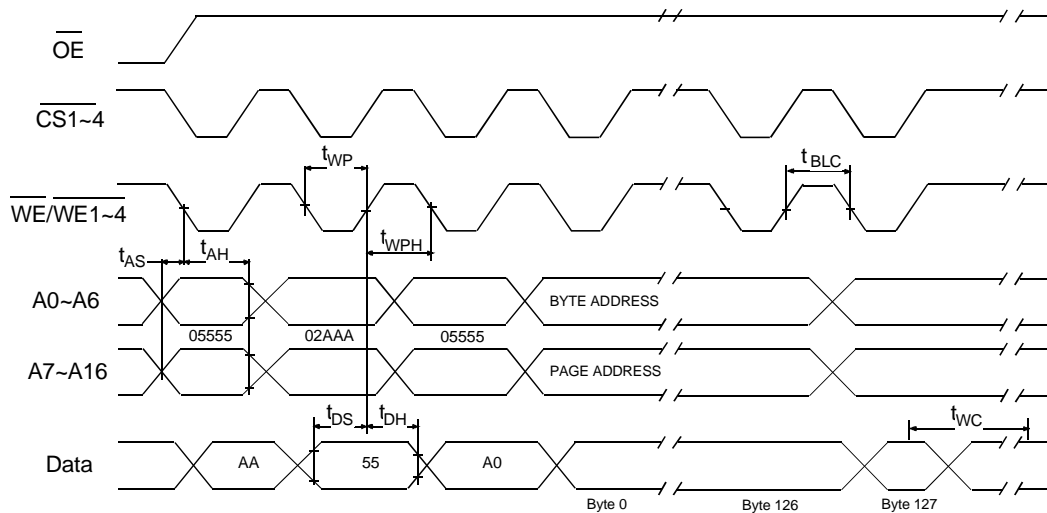
**DATA Polling Waveform**



**Toggle Bit Waveform**



**Software Protected Write Waveform**



## Device Operation

The following description deals with the device, with the references to  $\overline{WE}$  meaning  $\overline{WE1-4}$  on the 'A' parts.

### Read

The device read operations are initiated by both Output Enable and Chip Select LOW. The read operation is terminated by either Chip Select or Output Enable returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either Output Enable or Chip Select is HIGH.

### Write

Write operations are initiated when both Chip Select and Write Enable are LOW and Output Enable is HIGH. The device supports both a Chip Select and Write Enable controlled write cycle. That is, the address is latched by the falling edge of either Chip Select or Write Enable, whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select or Write Enable, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

### Page Mode Write

The page write feature of the device allows the entire memory to be written in 5 seconds. Page Write allows 128 bytes of data to be written prior to the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A8 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write up to 128 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the Write Enable HIGH to LOW transition, must begin within 150  $\mu$ s of the falling edge of the preceding Write Enable. If a subsequent Write Enable HIGH to LOW transition is not detected within 150  $\mu$ s, the internal automatic programming cycle will commence.

### DATA Polling

The device features  $\overline{DATA}$  Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on D7. Once the programming is complete, D7 will reflect the true data. Note: If the device is in a protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### TOGGLE bit

In addition to  $\overline{DATA}$  polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

### Hardware Data Protection

The device provides three hardware features to protect nonvolatile data from inadvertent writes.

- Noise Protection - A Write Enable pulse less than 15 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense - All functions are inhibited when  $V_{CC} < 3.6$  V.
- Write Inhibit - Holding either Output Enable LOW, Write Enable HIGH or Chip Select HIGH will prevent an inadvertent write cycle during power on or power off, maintaining data integrity.



## Software Data Protection

The device can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the device is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

## Operating Modes

The table below shows the logic inputs required to control the operation of the device.

MODE	$\overline{\text{CS1-4}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	1	0	Data in
Standby	1	X	X	Floating
Write Inhibit	X	X	1	
	X	0	X	

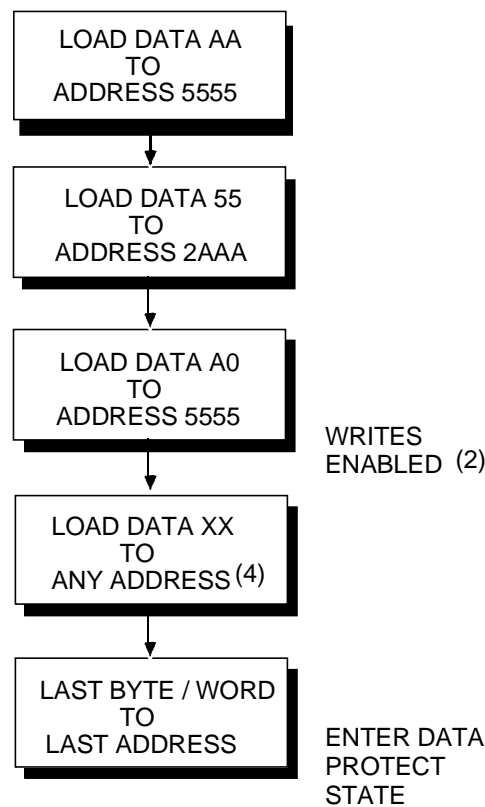
0 =  $V_{\text{IL}}$  : 1 =  $V_{\text{IH}}$  : X =  $V_{\text{IH}}$  or  $V_{\text{IL}}$

## Software Algorithms

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specific addresses. The three byte sequence opens the page write window enabling the host to write from 1 to 128 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state

### Software Data Protection Algorithm

Regardless of whether the device has been protected or not, once the software data protected algorithm is used and the data is written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and any subsequent power-up.

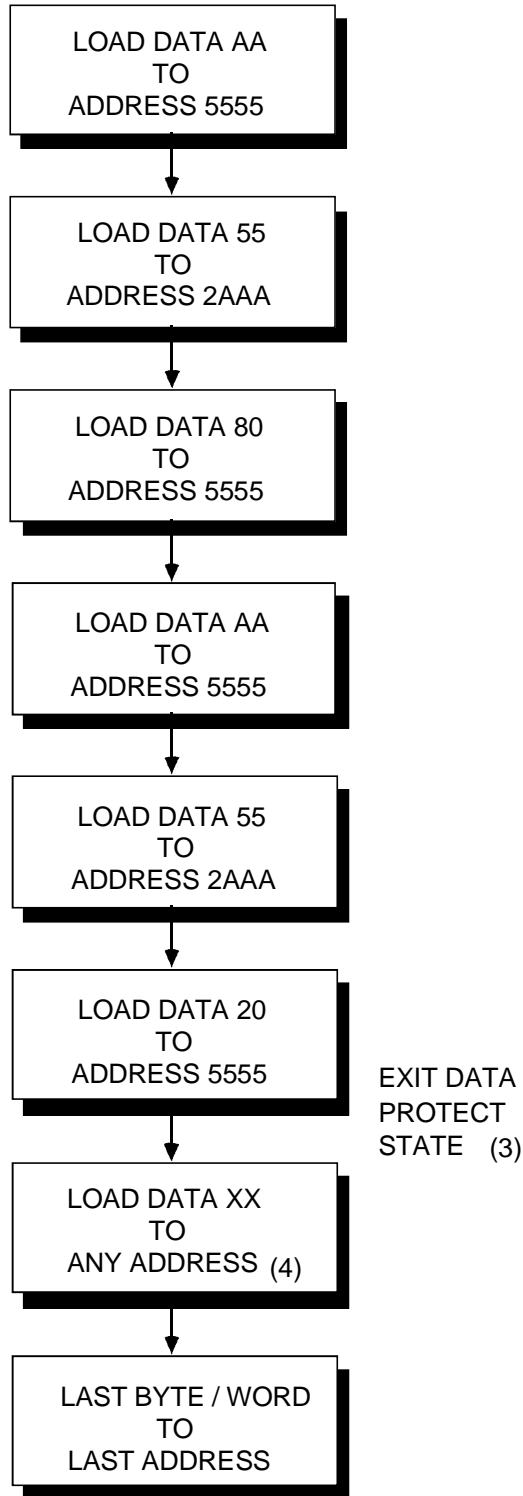


#### Notes:

- (1) Data Format I/O7-I/O0 (Hex);  
**Once initiated, this sequence of write operations should not be interrupted.**
- (2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.
- (3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.
- (4) 1 to 128 bytes of data may be loaded.

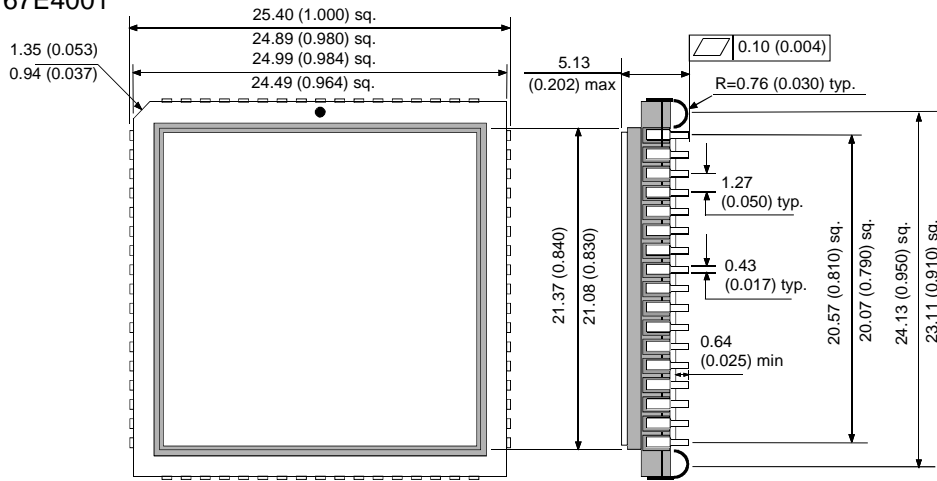
**Software Data Protect Disable**

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer. The following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the device will be in standard operating mode.

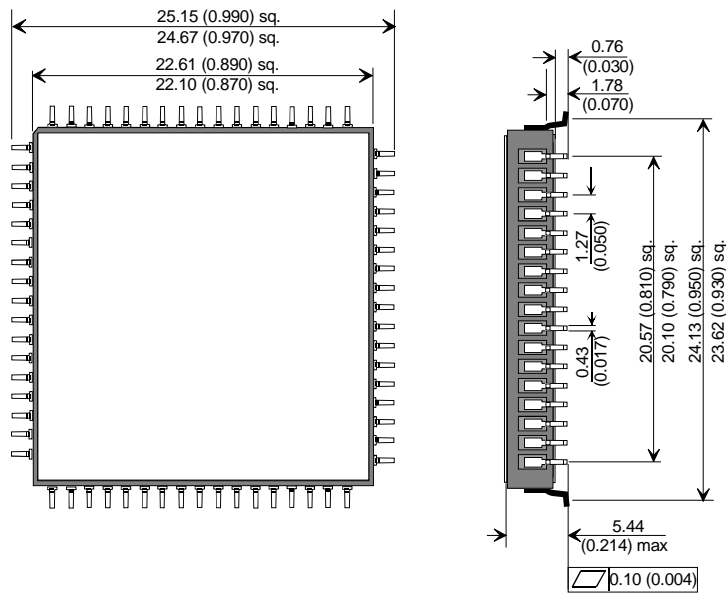


**Package Details**

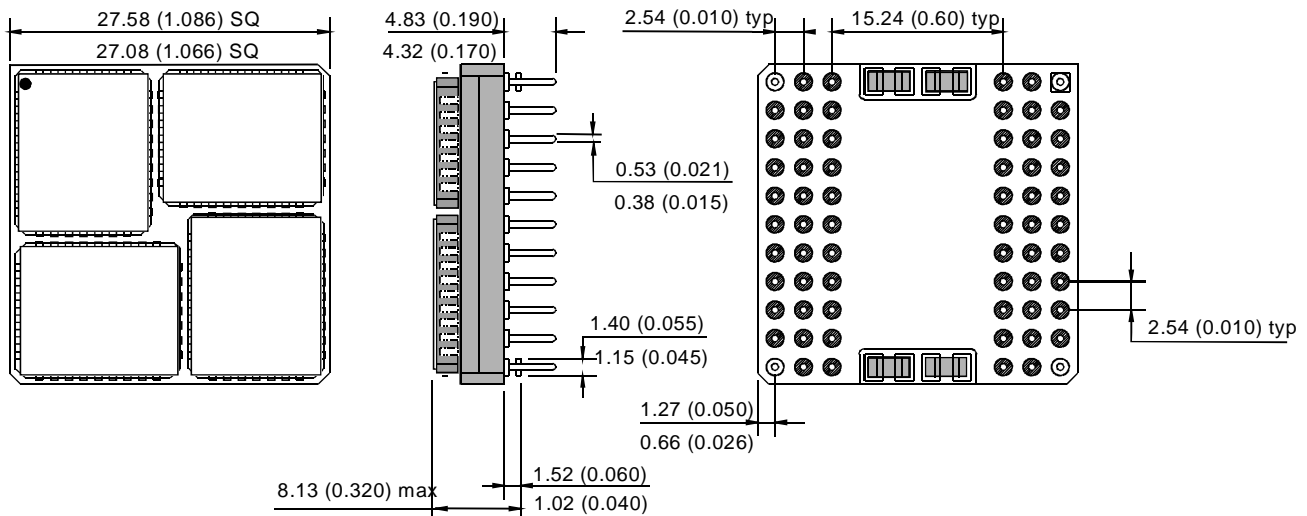
**PUMA 67E4001**



**PUMA 77E4001**

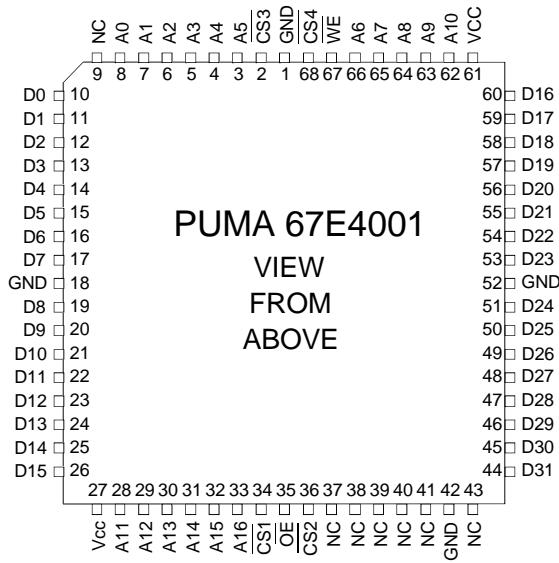


**PUMA 2E4001**

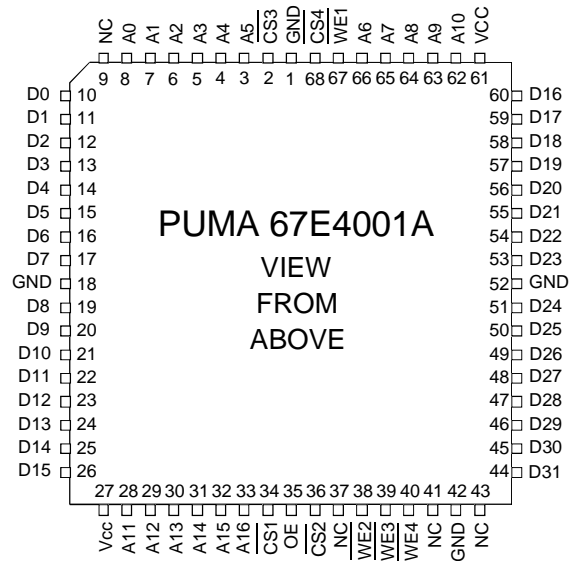


**Pin Definitions**

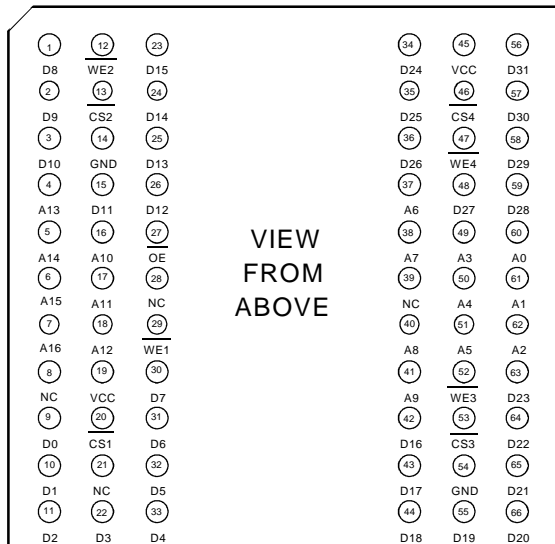
PUMA 67E4001 / PUMA 77E4001



PUMA 67E4001A / PUMA 77E4001PUMA



PUMA 2E4001



**Military Screening Procedure**

<b>MultiChip Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .</b>		
<b>MB MULTICHIP MODULE SCREENING FLOW</b>		
<b>SCREEN</b>	<b>TEST METHOD</b>	<b>LEVEL</b>
<b>Visual and Mechanical</b> Internal visual Temperature cycle Constant acceleration	2010 Condition B or manufacturers equivalent 1010 Condition C (10 Cycles, -65°C to +150°C) 2001 Condition B (Y1 & Y2) (10,000g)	100% 100% 100%
<b>Endurance</b> Write Cycle endurance and Data Retention performance	As per Internal Specification.	
<b>Burn-In</b> Pre-Burn-in electrical Burn-in	Per applicable device specifications at $T_A=+25^\circ\text{C}$ $T_A=+125^\circ\text{C}$ , 160hrs min	100% 100%
<b>Final Electrical Tests</b> Static (DC)  Functional  Switching (AC)	Per applicable Device Specification a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100% 100%
<b>Percent Defective allowable (PDA)</b>	Calculated at post-burn-in at $T_A=+25^\circ\text{C}$	10%
<b>Hermeticity</b> Fine Gross	1014 Condition A Condition C	100% 100%
<b>Quality Conformance</b>	Per Applicable Device Specification	Sample
<b>External Visual</b>	2009 Per vendor or customer specification	100%

## Ordering Information

### PUMA 2E4001AMB-12E

	<p>Blank = 10,000 W/E cycle endurance E = 100,000 W/E cycle endurance</p> <p>12 = 120 ns 15 = 150 ns 20 = 200 ns</p> <p>Blank = Commercial Temperature I = Industrial Temperature M = Military Temperature MB = Processed in accordance with MIL-STD-883</p> <p>Blank = <u>Single WE</u> (PUMA 67 / 77 only) <u>WE1~4</u> (PUMA 2 only) A = <u>WE1~4</u> (PUMA 67 / 77 only)</p> <p>4001 = 128Kx 32, user configurable as 256K x 16 and 512K x 8</p> <p>E = EEPROM MEMORY</p> <p>PUMA 2 = JEDEC 66 Pin Ceramic PGA package</p> <p>PUMA 67 = JEDEC 68 J-Leaded Ceramic Surface Mount package</p> <p>PUMA 77 = JEDEC 68 Leaded Gull Wing Ceramic Surface Mount package</p>
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#### Note :

Although this data is believed to be accurate, the information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed at any time without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.