1.1GHz Dual Modulus Prescaler

The MC12022A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

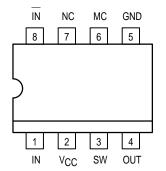
The MC12022B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5V
- Low-Power 7.5mA Typical
- Operating Temperature Range of -40 to +85°C
- Short Setup Time (tset) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL. Maximum Input Voltage Should Be Limited to 6.5Vdc

Pinout: 8–Lead Plastic (Top View)



FUNCTIONAL TABLE

SW	MC	Divide Ratio		
Н	Н	64		
Н	L	65		
L	н	128		
L	L	129		

Note: SW: $H = V_{CC}$, L = Open

MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V

MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
VCC	Power Supply Voltage, Pin 2	-0.5 to + 7.0	Vdc
TA	Operating Temperature Range	-40 to + 85	°C
T _{stg}	Storage Temperature Range	-65 to + 150	°C
MC	Modulus Control Input, Pin 6	-0.5 to + 6.5	Vdc

1/97



MC12022A MC12022B

MECL PLL COMPONENTS

+64/65, +128/129 DUAL MODULUS PRESCALER

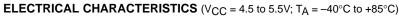


P SUFFIX 8–LEAD PLASTIC PACKAGE CASE 626–05



D SUFFIX 8–LEAD PLASTIC SOIC PACKAGE CASE 751–05

Symbol	Characteristic	Min	Тур	Max	Unit
ft	Toggle Frequency (Sine Wave Input)	0.1	1.6	1.1	GHz
lcc	Supply Current Output Unloaded (Pin 2)		7.5	10	mA
V _{IH1}	Modulus Control Input High (MC)	2.0		V _{CC}	V
V _{IL1}	Modulus Control Input Low (MC)			0.8	V
V _{IH2}	Divide Ratio Control Input High (SW)	V _{CC}	V _{CC}	V _{CC}	Vdc
V _{IL2}	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
V _{out}	Output Voltage Swing (C _L = 12pF; R _L = $2.2k\Omega$)	1.0	1.6		V _{p-p}
t _{set}	Modulus Setup Time MC to Out		11	16	ns
V _{in}	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp
IO	Output Current (C _L = 12pF; R _L = 2.2k Ω)		1.5	4.0	mA



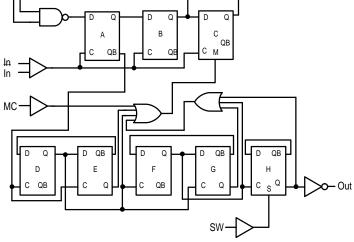
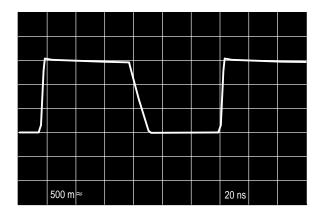
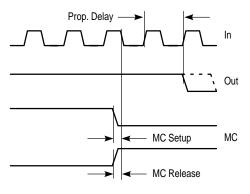


Figure 1. Logic Diagram (MC12022A)

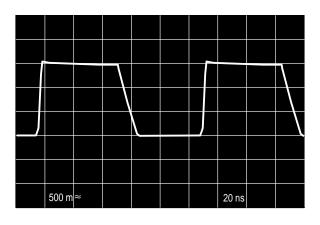


(+64, 500MHz Input Frequency, V_{CC} = 5.0V, T_{A} = 25^{\circ}C, Output Loaded)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time



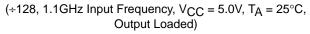
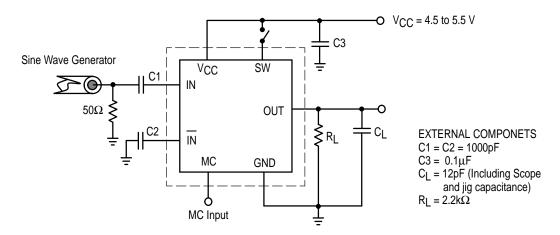
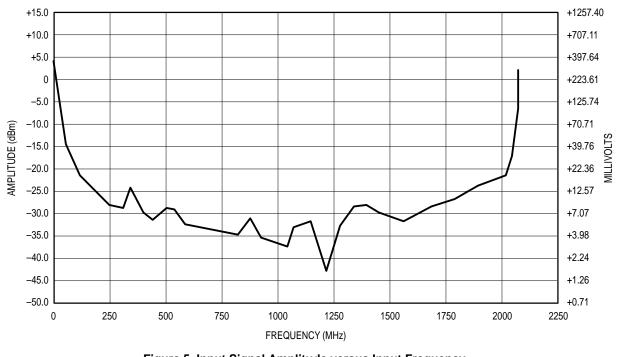
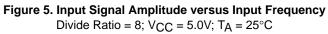


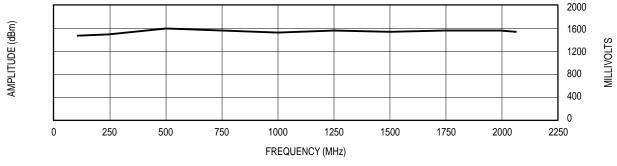
Figure 3. Typical Output Waveforms













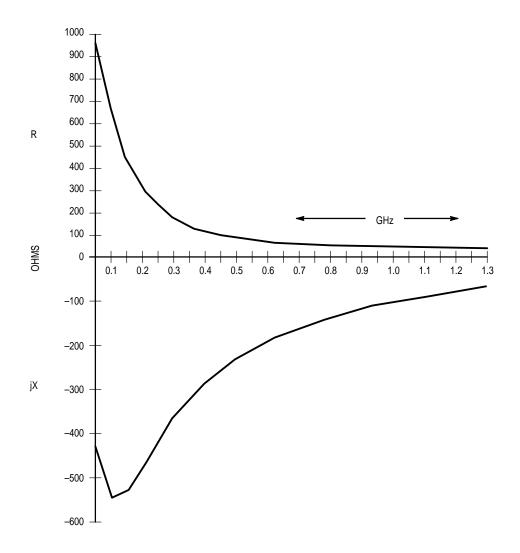
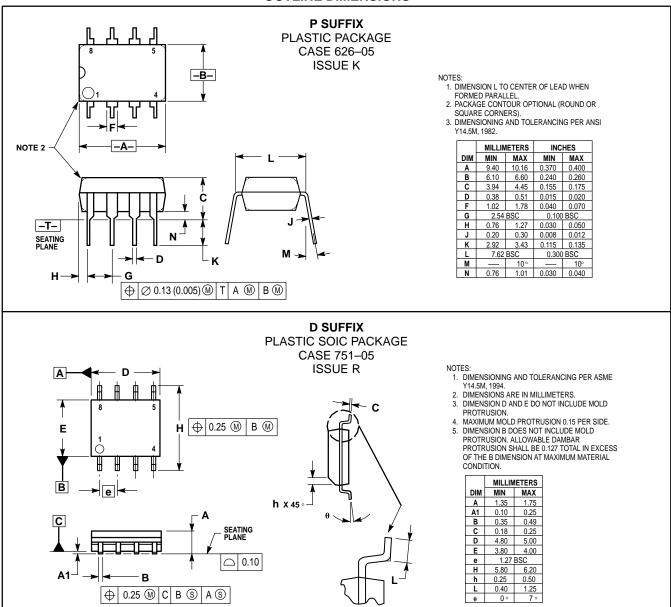


Figure 7. Typical Input Impedance versus Input Frequency

OUTLINE DIMENSIONS



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