Data Sheet | March 15, 2007 | FN7493.2

4-Channel Integrated LCD Supply

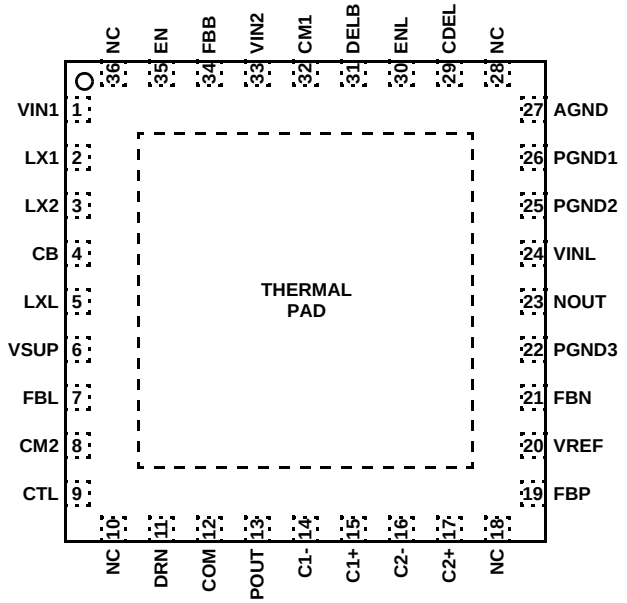
The ISL97651 represents a high power, integrated LCD supply IC targeted at large panel LCD displays. The ISL97651 integrates a high power, 4.4A boost converter for A_{VDD} generation, an integrated V_{ON} charge pump, a V_{OFF} charge pump driver, V_{ON} slicing circuitry and a buck regulator with 2A switch for logic generation.

The ISL97651 have been designed for ease of layout and low BOM cost. Supply sequencing is integrated for both A_{VDD} -> V_{OFF} -> V_{ON} and A_{VDD}/V_{OFF} -> V_{ON} sequences. The TFT power sequence uses a separate enable to the logic buck regulator for maximum flexibility.

Peak efficiencies are 90% for boost and 92% for buck while operating from a 4V to 5.5V input supply. The current mode buck offers superior line and load regulation. Available in the 36 Ld QFN package, the ISL97651 is specified for ambient operation over the -40°C to +105°C temperature range.

Pinout

ISL97651
(36 LD TQFN)
TOP VIEW



Features

- 4V to 5.5V input supply
- A_{VDD} boost up to 20V, with integrated 4.4A FET
- Integrated V_{ON} charge pump, up to 34V out
- V_{OFF} charge pump driver, down to -18V
- V_{LOGIC} buck down to 1.2V, with integrated 2A FET
- Automatic start-up sequencing
  - A_{VDD} -> V_{OFF} -> V_{ON} or A_{VDD}/V_{OFF} -> V_{ON}
  - Independent logic enable
- V_{ON} slicing
- Thermally enhanced thin QFN package (6mmx6mm)
- Pb-free plus anneal available (RoHS compliant)

Applications

- LCD monitors (15”+)
- LCD-TVs (40”+)
- Notebook displays (up to 16”)
- Industrial/medical LCD displays

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97651ARTZ-T	ISL976 51ARTZ	13” (4k pcs)	36 Ld 6x6 TQFN	L36.6x6
ISL97651ARTZ-TK	ISL976 51ARTZ	13” (1k pcs)	36 Ld 6x6 TQFN	L36.6x6

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Maximum Pin Voltages, All Pins Except Below 6.5V
LX1, LX2, V_{SUP}, NOUT, DELB, C1-, C2- 24V
C1- 14V
CB 13V
DRN, COM, POUT, C1+, C2+ 36V
CB-V_{INL} 6.5V

Recommended Operating Conditions

Input Voltage Range, V_{IN} . . . . . 4V to 5.5V
Boost Output Voltage Range, A_{VDD} . . . . . +20V
V_{ON} Output Range, V_{ON} . . . . . +15V to +32V
V_{OFF} Output Range, V_{OFF} . . . . . -15V to -5V
Logic Output Voltage Range, V_{LOGIC} . . . . . +1.5V to +3.3V
Input Capacitance, C_{IN} . . . . . 2 x 10µF
Boost Inductor, L1 . . . . . 3.3µH to 10µH
Output Capacitance, C_{OUT} . . . . . 2 x 22µF
Buck Inductor, L2 . . . . . 3.3µH to 10µH
Operating Ambient Temperature Range . . . . . -40°C to +105°C
Operating Junction Temperature . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6x6 QFN Package (Notes 1, 2)	30	2.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation
$T_A \leq +25°C$ 3.3W
T_A = +70°C 1.8W
T_A = +85°C 1.3W
T_A = +100°C 0.8W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

+150°C max junction temperature is intended for short periods of time to prevent shortening the lifetime. Operation close to +150°C junction may trigger the shutdown of the device even before +150°C, since this number is specified as typical.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = 5V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY PINS						
V_{IN}	Supply Voltage (VIN1 and VIN2)		4	5	5.5	V
V_{INL}	Logic Supply Voltage		4	5	5.5	V
V_{SUP}	Charge Pumps and V_{ON} Slice Positive Supply		4		20	V
I_{VIN}	Quiescent Current into V_{IN}	Enabled, No switching			3	mA
		Disabled			10	µA
I_{INL}	Logic Supply Current	Enabled, No switching		0.4	1.0	mA
		Disabled			10	µA
I_{SUP}	V_{SUP} Supply Current	Enabled, No switching and VP_{OUT} = V_{SUP}			0.5	mA
		Disabled			10	µA
V_{LOR}	Undervoltage lockout threshold	V_{IN} rising	2.0	2.75	2.9	V
V_{LOF}	Undervoltage lockout threshold	V_{IN} falling	1.9	2.2	2.5	V
V_{REF}	Reference Voltage	T_A = +25°C	1.19	1.205	1.235	V
			1.187	1.205	1.238	V
f_{OSC}	Oscillator Frequency		1010	1200	1400	kHz
A_{VDD} BOOST D_{Max}, Maximum Duty Cycle: Minimum 84%						
V_{BOOST}	Boost Output Range		1.25*V_{IN}		20	V
I_{BOOST}	Boost Switch Current	Current limit	4.4	4.8	6.3	A

Electrical Specifications V_{IN} = 5V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
EFF_{BOOST}	Peak Efficiency	See graphs and component recommendations		90		%
$r_{DS(ON)}$	Switch ON-Resistance			70	100	mΩ
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	PI mode, R1 = 10k and C3 = 4.7nF over a load range of 0mA to 300mA (tested), 0-I_{LIMIT_ONSET} (by design)		0.4	1.5	%/V
$\Delta V_{BOOST}/\Delta I_{OUT}$	Load Regulation			0.1	0.5	%
V_{FBB}	Boost Feedback Voltage	T_A = +25°C	1.192	1.205	1.218	V
			1.188	1.205	1.222	V
ACC_{BOOST}	A_{VDD} Output Accuracy	T_A = +25°C	-1.5		+1.5	%
t_{SS}	Soft-start Period for A_{VDD}	C_{DEL} = 220nF		9.6		ms
V_{LOGIC} BUCK D_{MAX}_buck typical maximum duty cycle = 0.85*(V_{INL}-I_{LOAD}*0.3) I_{LOAD}_min, Minimum 1mA for V_{INL}-V_{BUCK} >1.5V, 5mA otherwise						
V_{BUCK}	Buck Output Voltage	Output current = 0.5A	V_{REF}		4	V
I_{BUCK}	Buck Switch Current	Current limit	2.0	2.7		A
EFF_{BUCK}	Peak Efficiency	See graphs and component recommendations		92		%
$R_{DS-ONBK}$	Switch ON-Resistance			200	455	mΩ
$\Delta V_{BUCK}/\Delta V_{IN}$	Line Regulation	PI mode, R1 = 2k and C3 = 4.7nF over a load range of 0mA to 300mA (tested), 0-I_{LIMIT_ONSET} (by design)		0.1	1	%/V
$\Delta V_{BUCK}/\Delta I_{OUT}$	Load Regulation			0.04	0.5	%
V_{FBL}	FBL Regulation Voltage	I_{DRVL} = 1mA, T_A = +25°C	1.176	1.2	1.224	V
		I_{DRVL} = 1mA	1.174	1.2	1.226	V
ACC_{LOGIC}	V_{LOGIC} Output Accuracy	T_A = +25°C	-2		+2	%
$t_{SS(L)}$	Soft-Start Period for V(Logic)	C(VREF) = 220nF (Note - no soft-start if EN asserted HIGH before ENB)		0.5		ms
NEGATIVE (V_{OFF}) CHARGE PUMP						
V_{OFF}	V_{OFF} Output Voltage Range	2X Charge Pump	-V_{SUP}+1.4V		0	V
$I_{LOAD\_NCP\_MIN}$	External Load Driving Capability	V_{SUP} > 5V	30			mA
$r_{ON(NOUT)H}$	High-Side Driver ON-Resistance at N_{OUT}	$I_{(NOUT)}$ = +60mA			10	Ω
$r_{ON(NOUT)L}$	Low-Side Driver ON-Resistance at N_{OUT}	$I_{(NOUT)}$ = -60mA			5	Ω
$I_{PU(NOUT)LIM}$	Pull-up Current Limit in N_{OUT}	$V_{(NOUT)}$ = 0V to V(SUP)-0.5V	60	270		mA
$I_{PD(NOUT)LIM}$	Pull-down Current Limit in N_{OUT}	$V_{(NOUT)}$ = 0.36V to V(VSUP)		-200	-60	mA
$I_{(NOUT)LEAK}$	Leakage Current in N_{OUT}	$V_{(FBN)}$ < 0 or EN = LOW	-2		2	µA
V_{FBN}	FBN Regulation Voltage	I_{DRVN} = 0.2mA, T_A = +25°C	0.173	0.203	0.233	V
		I_{DRVN} = 0.2mA	0.171	0.203	0.235	V
ACCN	V_{OFF} Output Accuracy	I_{OFF} = 1mA, T_A = +25°C	-3		+3	%
D_NCP_max	Max Duty Cycle of the Negative Charge Pump			50		%
$r_{PD(FBN)OFF}$	Pull-Down Resistance, Not Active	$I_{(FBN)}$ = 500µA	2	3	4	kΩ

Electrical Specifications V_{IN} = 5V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
POSITIVE (V_{ON}) CHARGE PUMP						
V_{ON}	V_{ON} Output Voltage Range	2X or 3X Charge Pump	V_{SUP} + 2V		34	V
$I_{LOAD\_PCP\_MIN}$	External Load Driving Capability	V_{ON} = 25V (2X Charge Pump)	20			mA
		V_{ON} = 34V (3X Charge Pump)	20			mA
$r_{ON(VSUP\_SW)}$	ON-Resistance of V_{SUP} Input Switch	$I_{(SWITCH)}$ = +40mA		10	17	Ω
$r_{ON(C1/2-)H}$	High-Side Driver ON-Resistance at C1- and C2-	$I_{(C1/2-)}$ = +40mA		10	20	Ω
$r_{ON(C1/2-)L}$	Low-Side Driver ON-Resistance at C1- and C2-	$I_{(C1/2-)}$ = -40mA		4	7	Ω
$I_{PU(VSUP\_SW)}$	Pull-Up Current Limit in V_{SUP} Input Switch	$V_{(C2+)}$ = 0V to $V_{(SUP)}$ - 0.4V - $V_{(DIODE)}$	40	100		mA
$I_{PU(C1/2-)}$	Pull-Up Current Limit in C1- and C2-	$V_{(C1/2-)}$ = 0V to $V_{(VSUP)}$ - 0.4V	40	100		mA
$I_{PD(C1/2-)}$	Pull-Down Current Limit in C1- and C2-	$V_{(C1/2-)}$ = 0.2V to $V_{(VSUP)}$		-100	-40	mA
$I_{(POUT)LEAK}$	Leakage Current in P_{OUT}	EN = LOW	-5		5	µA
V_{FBP}	FBP Regulation Voltage	I_{DRVP} = 0.2mA, T_A = +25°C	1.176	1.2	1.224	V
		I_{DRVP} = 0.2mA	1.172	1.2	1.228	V
ACCP	V_{ON} Output Accuracy	I_{ON} = 1mA, T_A = +25°C	-2		+2	%
D_PCP_max	Max Duty Cycle of the Positive Charge Pump			50		%
$V_{(DIODE)}$	Internal Schottky Diode Forward Voltage	$I_{(DIODE)}$ = +40mA		600	850	mV
ENABLE INPUTS						
VHI-EN	Enable “HIGH”		2.2			V
VLO_EN	Enable “LOW”				0.8	V
IEN_pd	Enable Pin Pull-Down Current	V_{EN} > VLO_EN			25	µA
VHI-ENL	Logic Enable “HIGH”		2.2			V
VLO-ENL	Logic Enable “LOW”				0.8	V
IENL_pd	Logic Enable Pin Pull-Down Current	V_{ENL} > VLO_ENL			25	µA
V_{ON} SLICE Positive Supply = $V_{(POUT)}$						
$I_{(POUT)\_SLICE}$	V_{ON} slice Current from P_{OUT} Supply	CTL = VDD, sequence complete		100	200	µA
		CTL = AGND, sequence complete		90	120	µA
$r_{ON(POUT-COM)}$	ON-Resistance between P_{OUT} - COM	CTL = VDD, sequence complete		5	10	Ω
$r_{ON(DRN-COM)}$	ON-Resistance between DRN - COM	CTL = ACGND, sequence complete		30	60	Ω
r_{ON_COM}	ON-Resistance between COM and PGND3	During start-up sequence	200	500	1500	Ω
VLO	CTL Input LOW Voltage	V_{IN} = 4V to 5.5V			0.8	V
VHI	CTL Input HIGH Voltage	V_{IN} = 4V to 5.5V	2.2			V

Electrical Specifications V_{IN} = 5V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
FAULT DETECTION THRESHOLDS						
T_off	Thermal Shut-Down (latched and reset by power cycle or EN cycle)	Temperature rising		150		°C
Vth_A_{VDD}(FBB)	A_{VDD} Boost Short Detection	$V_{(FBB)}$ falling less than		0.9		V
Vth_V_{LOGIC}(FBL)	V_{LOGIC} Buck Short Detection	$V_{(FBL)}$ falling less than		0.9		V
Vth_P_{OUT}(FBP)	P_{OUT} Charge Pump Short Detection	$V_{(FBP)}$ falling less than		0.9		V
Vth_N_{OUT}(FBN)	N_{OUT} Charge Pump Short Detection	$V_{(FBN)}$ rising more than		0.4		V
t_{FD}	Fault Delay Time to Chip Turns Off	C_{DEL} = 220nF		52		ms
START-UP SEQUENCING						
$t_{START-UP}$	Enable to A_{VDD} Start Time	C_{DEL} = 220nF		80		ms
I_{DELB_ON}	DELB Pull-Down Current or Resistance when Enabled by the Start-Up Sequence	VDELB > 0.9V	36	50	70	µA
		VDELB < 0.9V	1000	1326	1750	Ω
I_{DELB_OFF}	DELB Pull-Down Current or Resistance when Disabled	VDELB < 20V			500	nA
t_{VOFF}	A_{VDD} to V_{OFF}	C_{DEL} = 220nF		9		ms
t_{VON}	V_{OFF} to V_{ON} Delay	C_{DEL} = 220nF		20		ms
$t_{VON-SLICE}$	V_{ON} to $V_{ON-SLICE}$ Delay	C_{DEL} = 220nF		17		ms

Typical Performance Curves

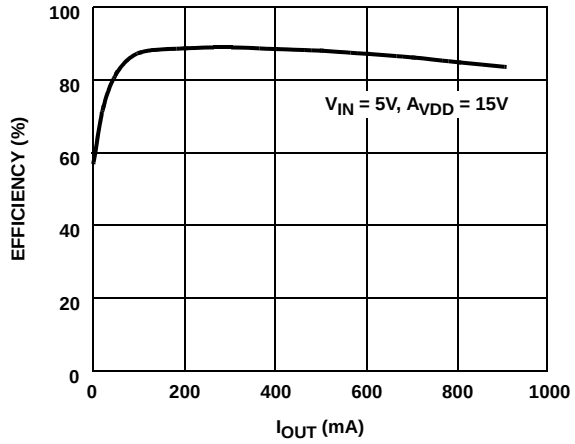


FIGURE 1. A_{VDD} EFFICIENCY vs I_{OUT}

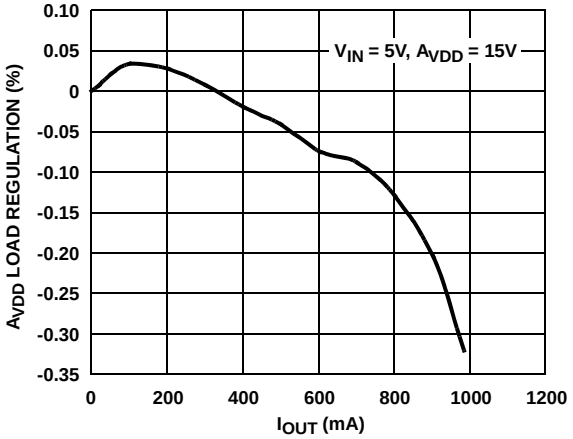


FIGURE 2. A_{VDD} LOAD REGULATION vs I_{OUT}

Typical Performance Curves (Continued)

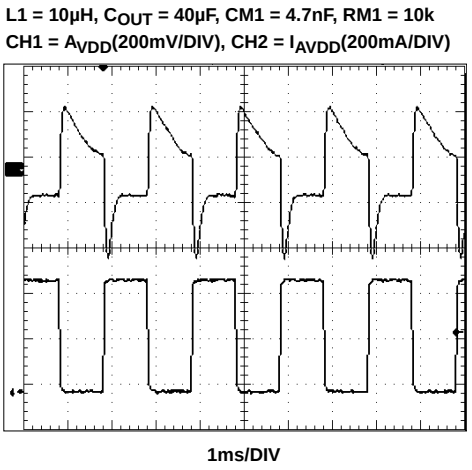


FIGURE 3. A_{VDD} TRANSIENT RESPONSE

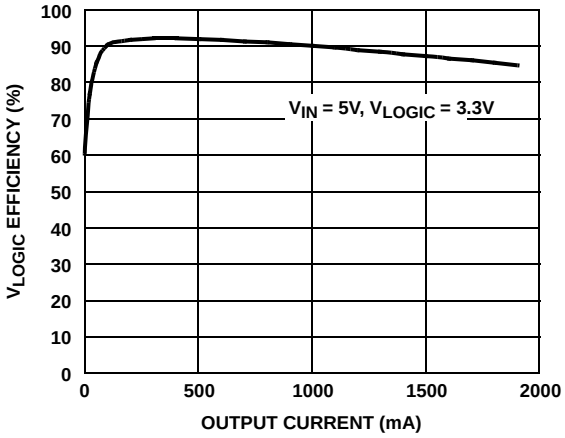


FIGURE 4. V_{LOGIC} EFFICIENCY vs OUTPUT CURRENT

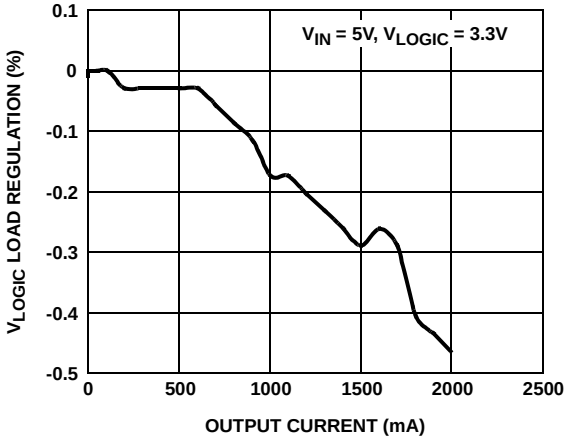


FIGURE 5. V_{LOGIC} LOAD REGULATION vs OUTPUT CURRENT

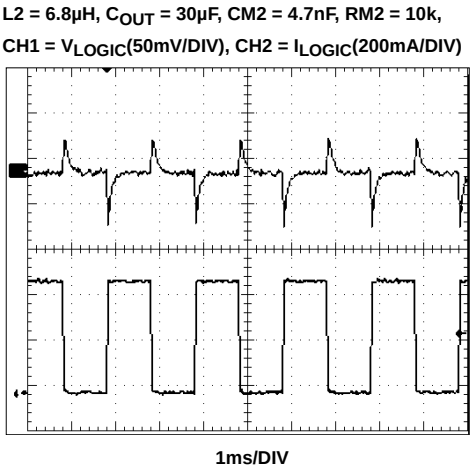


FIGURE 6. V_{LOGIC} TRANSIENT RESPONSE

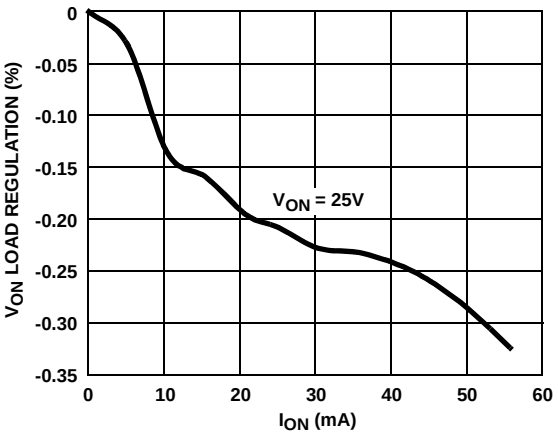


FIGURE 7. V_{ON} LOAD REGULATION vs I_{ON}

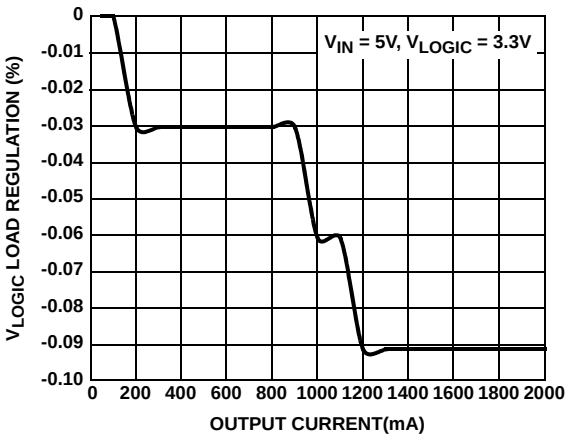
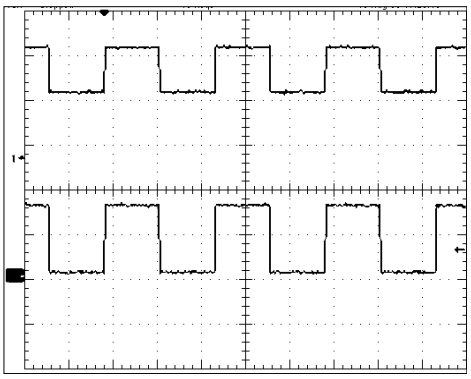


FIGURE 8. V_{LOGIC} LOAD REGULATION vs OUTPUT CURRENT

Typical Performance Curves (Continued)

CH1 = COM(10V/DIV), CH2 = CTL(2V/DIV)



4ms/DIV

FIGURE 9. V_{ON}-SLICE CIRCUIT OPERATION

CH1 = C_{DLY}, CH2 = V_{REF}, CH3 = V_{LOGIC}, CH4 = V_{ON}, R1 = A_{VDD}, R2 = A_{VDD_DELAY}, R3 = V_{OFF}

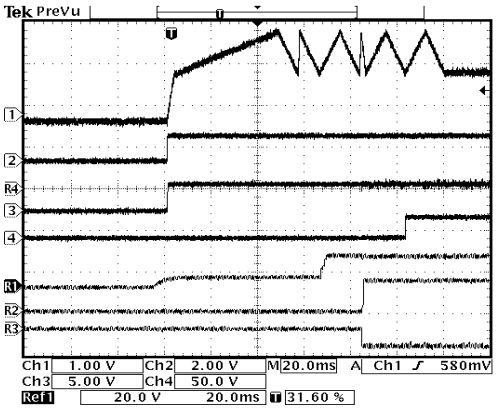


FIGURE 10. START-UP SEQUENCE

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VIN1	Input voltage, connect to pin 33 (V_{IN2})
2	LX1	Internal boost switch connection
3	LX2	Internal boost switch connection
4	CB	Logic buck, boost strap pin
5	LXL	Buck converter output
6	VSUP	Positive supply for charge pumps
7	FBL	Logic buck feedback pin
8	CM2	Buck compensation network pin
9	CTL	Input control for V_{ON} slice output
10, 18, 28, 36	NC	No connect. Connect to die pad and GND for improved thermal efficiency.
11	DRN	Lower reference voltage for V_{ON} slice output
12	COM	V_{ON} slice output: when CTL = 1, COM is connected to SRC through a 5Ω resistor; when CTL = 0, COM is connected to DRN through a 30Ω resistor.
13	POUT	Positive charge pump out
14	C1-	Charge pump capacitor 1, negative connection
15	C1+	Charge pump capacitor 1, positive connection
16	C2-	Charge pump capacitor 2, negative connection
17	C2+	Charge pump capacitor 2, positive connection
19	FBP	Positive charge pump feedback pin
20	VREF	Reference voltage
21	FBN	Negative charge pump feedback pin
22	PGND3	Power ground for V_{OFF}, V_{ON} and V_{ON} slice
23	NOUT	Negative charge pump output
24	VINL	Logic buck supply voltage
25, 26	PGND2, 1	Boost power grounds
27	AGND	Signal ground pin
29	CDEL	Delay capacitor for start up sequencing, soft-start and fault detection timers.
30	ENL	Buck enable for V_{LOGIC} output
31	DELB	Open drain NFET output to drive optional A_{VDD} delay PFET
32	CM1	Boost compensation network pin
33	VIN2	Input voltage, connect to pin 1 (V_{IN1})
34	FBB	Boost feedback pin
35	EN	Enable for Boost, charge pumps and V_{ON} slice (independent of ENL).
(Exposed Die Plate)	N/A	Connect exposed die plate on rear of package to ACGND and the PGND1, 2 pins. See “Layout Recommendation” on page 18 for PCB layout thermal considerations.

Block Diagram

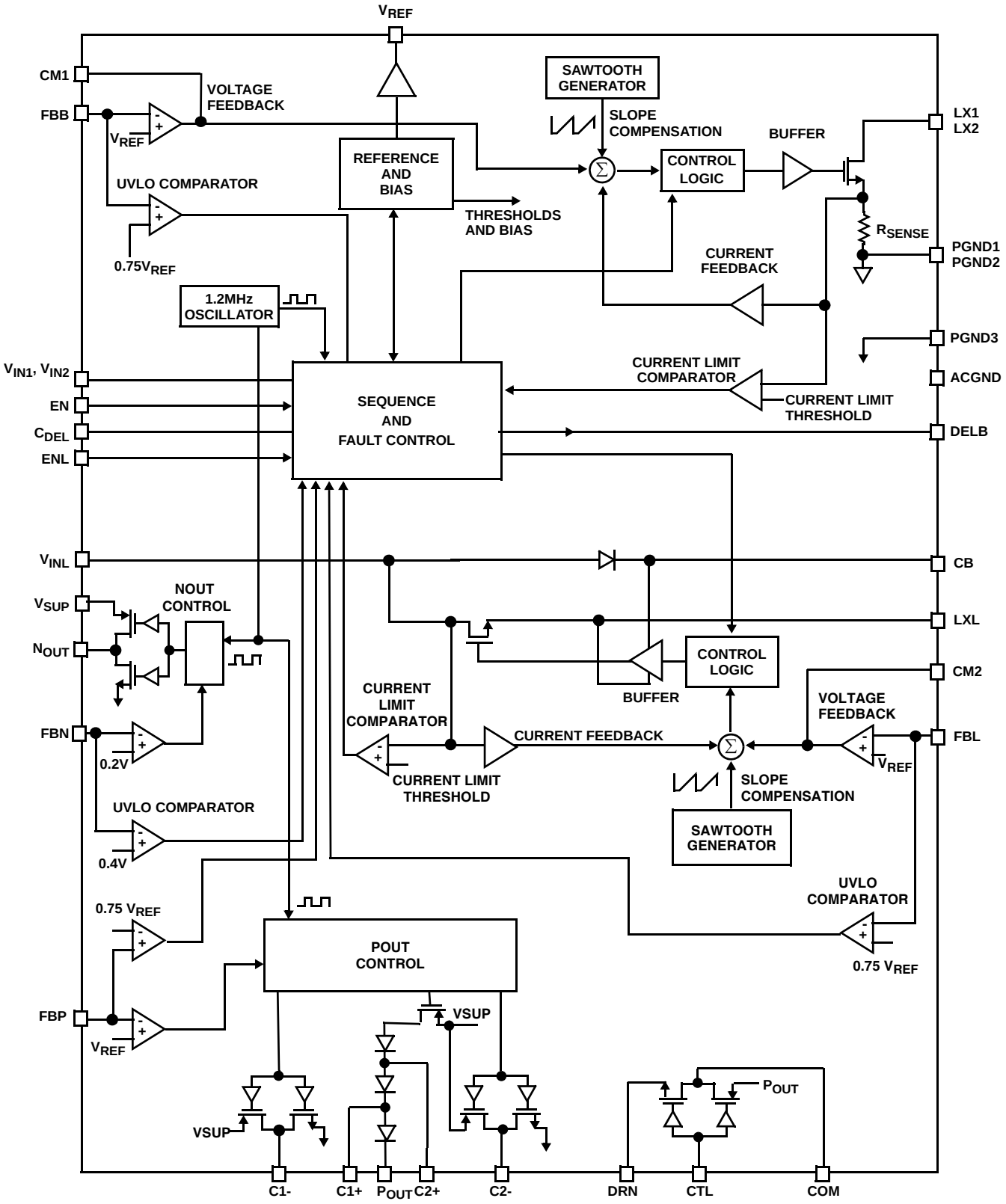
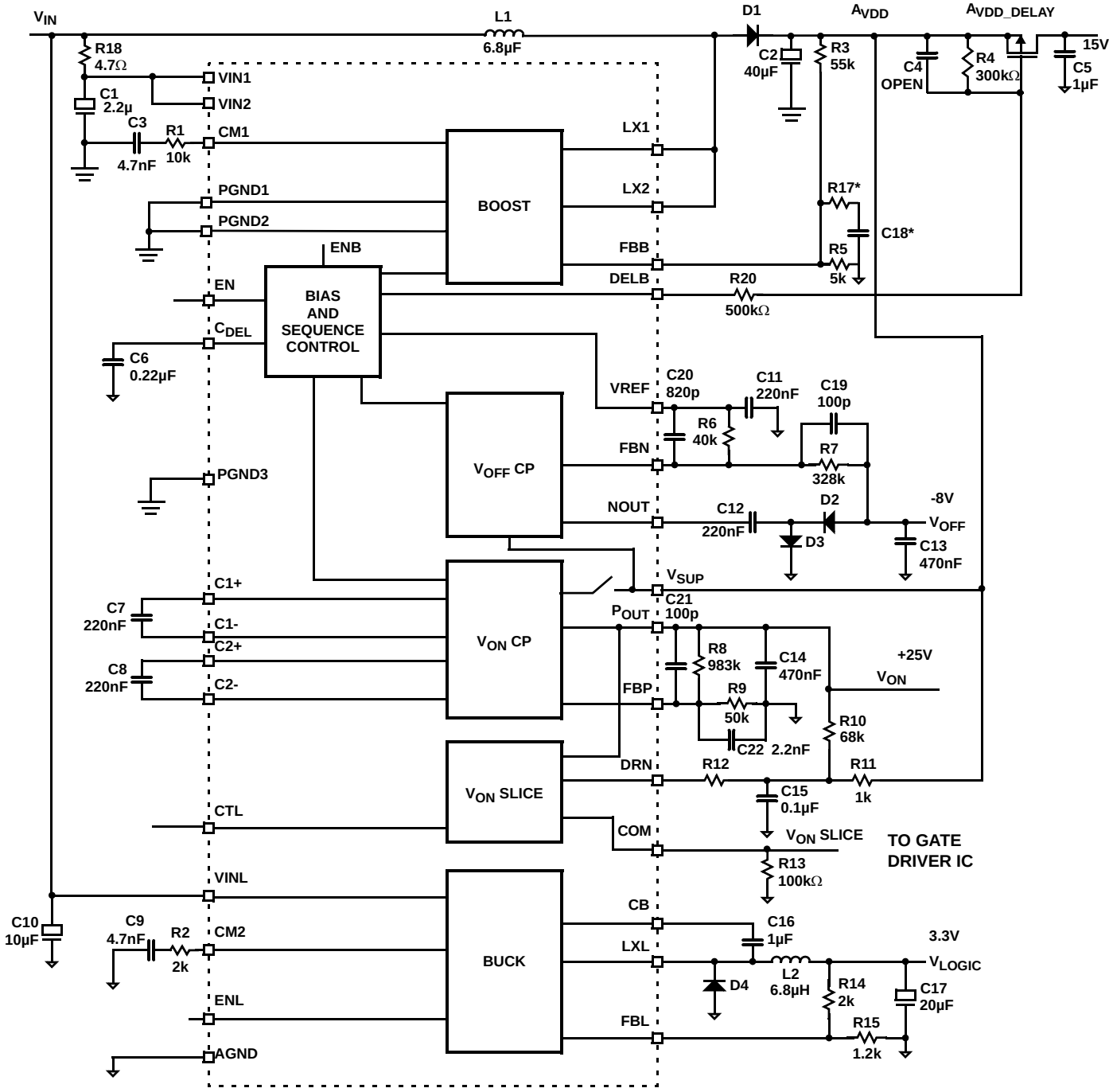


FIGURE 11. BLOCK DIAGRAM

Typical Application Diagram



*Open component positions.

Applications Information

The ISL97651 provides a complete power solution for TFT LCD applications. The system consists of one boost converter to generate the A_{VDD} voltage for column drivers, one buck converter to provide voltage to logic circuit in the LCD panel, one integrated V_{ON} charge pump and one V_{OFF} linear-regulator controller to provide the voltage to row drivers. This part also integrates V_{ON}-slice circuit which can help to optimize the picture quality. With the high output current capability, this part is ideal for big screen LCD TV and monitor panel application.

The integrated boost converter and buck converter operate at 1.2MHz which can allow the use of multilayer ceramic capacitors and low profile inductor which result in low cost, compact and reliable system. The logic output voltage is independently enabled to give flexibility to the system designers.

Boost Converter

The boost converter is a current mode PWM converter operating at a fixed frequency of 1.2MHz. It can operate in both discontinuous conduction mode (DCM) at light load and continuous mode (CCM). In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{BOOST}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

Where D is the duty cycle of the switching MOSFET

Figure 11 shows the functional block diagram of the boost regulator. It uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 2:

$$V_{BOOST} = \frac{(R_3 + R_5)}{R_5} \times V_{REF} \quad \text{(EQ. 2)}$$

The current through the MOSFET is limited to a minimum of $4.4A_{PEAK}$ (maximum values can be up to $6.3A_{PEAK}$.

This restricts the maximum output current (average) based on Equation 3:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

Where ΔI_L is peak to peak inductor ripple current, and is set by Equation 4:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 4)}$$

where f_S is the switching frequency (1.2MHz).

Table 1 gives typical values (margins are considered 10%, 3%, 20%, 10% and 15% on V_{IN}, V_O, L, f_S and I_{OMAX}:

TABLE 1. MAXIMUM OUTPUT CURRENT CALCULATION

V_{IN} (V)	V_O (V)	L (µH)	F_S (MHz)	I_{OMAX} (mA)
4	9	6.8	1.2	1661
4	12	6.8	1.2	1173
4	15	6.8	1.2	879
5	9	6.8	1.2	2077
5	12	6.8	1.2	1466
5	15	6.8	1.2	1099

Boost Converter Input Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of input capacitor should be larger than the maximum input voltage. Examples of recommended capacitors are given in Table 2 below.

TABLE 2. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/10V	1210	Murata	GRB32ER61A226K

Boost Inductor

The boost inductor is a critical component which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are to match the internal slope compensation. The inductor must be able to handle without saturating the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1-D}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 5)}$$

Some inductors are recommended in Table 3.

TABLE 3. BOOST INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
6.8µH/ 4.6A_{PEAK}	12.95x9.4x5.21	Coilcraft	DO3316P-682ML
10µH/ 5.5A_{PEAK}	10x10x5	Sumida	CDR10D48MNNP-100NC
5.2µH/ 4.55A_{PEAK}	10x10.1x3.8	Cooper Bussmann	CD1-5R2

Rectifier Diode (Boost Converter)

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements. Table 4 shows some recommendations for boost converter diode.

TABLE 4. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
SS23	30V/2A	SMB	Fairchild Semiconductor
MBRS340	40V/3A	SMC	International Rectifier
SL23	30V/2A	SMB	Vishay Semiconductor

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \quad \text{(EQ. 6)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across then increases. C_{OUT} in Equation 6 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

Table 5 shows some selections of output capacitors.

TABLE 5. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

PI Loop Compensation (Boost Converter)

The boost converter of ISL97651 can be compensated by a RC network connected from CM1 pin to ground. C3 = 4.7nF and R1 = 10k RC network is used in the demo board. A higher resistor value can be used to lower the transient overshoot - however, this may be at the expense of stability to the loop.

The stability can be examined by repeatedly changing the load between 100mA and a max level that is likely to be used in the system being used. The A_{VDD} voltage should be examined with an oscilloscope set to AC 100mV/div and the amount of ringing observed when the load current changes. Reduce excessive ringing by reducing the value of the resistor in series with the CM1 pin capacitor.

Boost Converter Feedback Resistors and Capacitor

An RC network across feedback resistor R5 may be required to optimize boost stability when A_{VDD} voltage is set to less than 12V. This network reduces the internal voltage feedback used by the IC. This RC network sets a pole in the control loop. This pole is set to approximately fp = 10kHz for C_{OUT} = 10µF and fp = 4kHz for C_{OUT} = 30µF. Alternatively, adding a small capacitor (20-100pF) in parallel with R5 (i.e. R17 = short) may help to reduce A_{VDD} noise and improve regulation, particularly if high value feedback resistors are used.

$$R17 = \left(\left(\frac{1}{0.1 \times R5}\right) - \frac{1}{R3}\right)^{-1} \quad \text{(EQ. 7)}$$

$$C18 = \frac{1}{(2 \times 3.142 \times fp \times R5)} \quad \text{(EQ. 8)}$$

Cascaded MOSFET Application

An 20V N-channel MOSFET is integrated in the boost regulator. For the applications where the output voltage is greater than 20V, an external cascaded MOSFET is needed, as shown in Figure 12. The voltage rating of the external MOSFET should be greater than A_{VDD}.

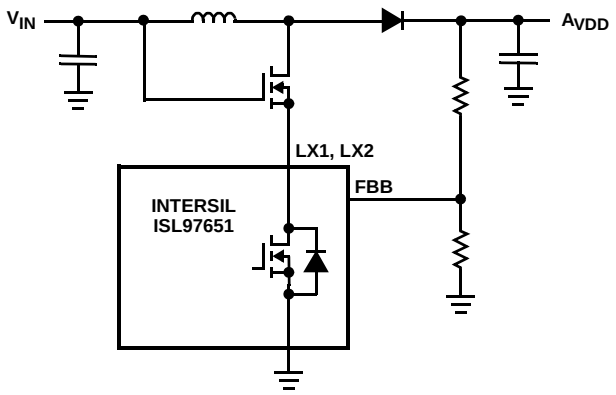


FIGURE 12. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

Buck Converter

The buck converter is the step down converter, which supplies the current to the logic circuit of the LCD system. The ISL97651 integrates an 20V N-Channel MOSFET to save cost and reduce external component count. In the continuous current mode, the relationship between input voltage and output voltage is shown in Equation 9:

$$\frac{V_{LOGIC}}{V_{IN}} = D \quad \text{(EQ. 9)}$$

Where D is the duty cycle of the switching MOSFET. Because D is always less than 1, the output voltage of buck converter is lower than input voltage.

The peak current limit of buck converter is set to 2A, which restricts the maximum output current (average) based on the Equation 10:

$$I_{OMAX} = 2A - \Delta I_{pp} \quad \text{(EQ. 10)}$$

Where ΔI_{PP} is the ripple current in the buck inductor as the Equation 11:

$$\Delta I_{pp} = \frac{V_{LOGIC}}{L \cdot f_s} \cdot (1 - D) \quad \text{(EQ. 11)}$$

Where L is the buck inductor, f_S is the switching frequency (1.2MHz).

Feedback Resistors

The buck converter output voltage is determined by the Equation 12:

$$V_{LOGIC} = \frac{R_{14} + R_{15}}{R_{15}} \times V_{REF} \quad \text{(EQ. 12)}$$

Where R14 and R15 are the feedback resistors of buck converter to set the output voltage current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 1kΩ is recommended.

Buck Converter Input Capacitor

The capacitor should support the maximum AC RMS current which happens when D = 0.5 and maximum output current.

$$I_{ACRMS}(C_{IN}) = \sqrt{D \cdot (1 - D)} \cdot I_O \quad \text{(EQ. 13)}$$

Where I_O is the output current of the buck converter. Table 6 shows some recommendations for input capacitor.

TABLE 6. INPUT CAPACITOR (BUCK) RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/16V	1210	Murata	C3225X7R1C226M

Buck Inductor

An inductor value in the range 3.3µH to 10µH is recommended for the buck converter. Besides the inductance, the DC resistance and the saturation current should also be considered when choosing buck inductor. Low DC resistance can help maintain high efficiency, and the saturation current rating should be at least 2A. Table 7 shows some recommendations for buck inductor.

TABLE 7. BUCK INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
4.7µH/2.7A_{PEAK}	5.7x5.0x4.7	Murata	LQH55DN4R7M01K
6.8µH/3A_{PEAK}	7.3x6.8x3.2	TDK	RLF7030T-6R8M2R8
10µH/2.4A_{PEAK}	12.95x9.4x3.0	Coilcraft	DO3308P-103

Rectifier Diode (Buck Converter)

A Schottky diode is recommended due to fast recovery and low forward voltage. The reverse voltage rating should be higher than the maximum input voltage. The peak current rating is 2A, and the average current should be as the Equation 14:

$$I_{AVG} = (1 - D)^* I_o \quad \text{(EQ. 14)}$$

Where I_O is the output current of buck converter. Table 8 shows some diode recommended.

TABLE 8. BUCK RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
PMEG2020EJ	20V/2A	SOD323F	Philips Semiconductors
SS22	20V/2A	SMB	Fairchild Semiconductor

Output Capacitor (Buck Converter)

Four 10µF or two 22µF ceramic capacitors are recommended for this part. The overshoot and undershoot will be reduced with more capacitance, but the recovery time will be longer.

TABLE 9. BUCK OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/6.3V	0805	TDK	C2012X5R0J106M
10µF/6.3V	0805	Murata	GRM21BR60J106K
22µF/6.3V	1210	TDK	C3216X5R0J226M
100µF/6.3V	1206	Murata	GRM31CR60J107M

PI Loop Compensation (Buck Converter)

The buck converter of ISL97651 can be compensated by a RC network connected from CM2 pin to ground. C9 = 4.7nF and R2 = 2k RC network is used in the demo board. The larger value resistor can lower the transient overshoot, however, at the expense of stability of the loop.

The stability can be optimized in a similar manner to that described in “PI Loop Compensation (Boost Converter)” on page 12.

Bootstrap Capacitor (C16)

This capacitor is used to provide the supply to the high driver circuitry for the buck MOSFET. The bootstrap supply is formed by an internal diode and capacitor combination. A 1µF is recommended for ISL97651. A low value capacitor can lead to overcharging and in turn damage the part.

If the load is too light, the on-time of the low side diode may be insufficient to replenish the bootstrap capacitor voltage. In this case, if V_{IN} - V_{BUCK} < 1.5V, the internal MOSFET pull-up device may be unable to turn-on until V_{LOGIC} falls. Hence, there is a minimum load requirement in this case. The minimum load can be adjusted by the feedback resistors to FBL.

The bootstrap capacitor can only be charged when the higher side MOSFET is off. If the load is too light which can not make the on time of the low side diode be sufficient to replenish the boot strap capacitor, the MOSFET can’t turn on. Hence there is minimum load requirement to charge the bootstrap capacitor properly.

Linear-Regulator Controllers (V_{ON} and V_{OFF})

The ISL97651 include 2 independent charge pumps (see Figure 13). The negative charge pump inverters the V_{SUP} voltage and provides a regulated negative output voltage. The positive charge pump doubles or triples the V_{SUP} voltage and provides a regulated positive output voltage. The regulation of both the negative and positive charge pumps is generated by internal comparator that senses the output voltage and compares it with the internal reference.

The pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps can provide 30mA for V_{OFF} and 20mA for V_{ON}.

The positive charge pump can generate double or triple V_{SUP} voltage depending on the configuration of C2+ and C2- pins. If the C2+ pin connects to C1+, it is the voltage doubler, and if C2+ connects C2- via a capacitor, it configured a voltage tripler.

Positive Charge Pump Design Consideration

The positive charge pump integrates all the diodes (D1, D2 and D3 shown in the block diagram in Figure 13) required for x2 (V_{SUP} doubler) and x3 (V_{SUP} tripler) modes of operation. During the chip start-up sequence the mode of operation is automatically detected when the charge pump is enabled. With both C7 and C8 present, the x3 mode of operation is detected. With C7 present, C8 open and with C1+ shorted to C2+, the x2 mode of operation will be detected.

Due to the internal switches to V_{SUP} (M1, M2 and M3), P_{OUT} is independent of the voltage on V_{SUP} until the charge pump is enabled. This is important for TFT applications where the negative charge pump output voltage (V_{OFF}) and A_{VDD} supplies need to be established before P_{OUT}.

The maximum P_{OUT} charge pump current can be estimated from Equation 15 assuming a 50% switching duty:

$$I_{MAX}(2x) \sim \text{min of } 50\text{mA or } \frac{2 \bullet V_{SUP} - 2 \bullet V_{DIODE}(2 \bullet I_{MAX}) - V(V_{ON})}{(2 \bullet (2 \bullet R_{ONH} + R_{ONL}))} \bullet 0.95\text{A} \quad \text{(EQ. 15)}$$

$$I_{MAX}(3x) \sim \text{min of } 50\text{mA or } \frac{3 \bullet V_{SUP} - 3 \bullet V_{DIODE}(2 \bullet I_{MAX}) - V(V_{ON})}{(2 \bullet (3 \bullet R_{ONH} + 2 \bullet R_{ONL}))} \bullet 0.95\text{V}$$

Note: V_{DIODE} (2 • I_{MAX}) is the on-chip diode voltage as a function of I_{MAX} and V_{DIODE} (40mA) < 0.7V.

In voltage doubler configuration, the maximum V_{ON} is as given by Equation 16:

$$V_{ON\_MAX(2x)} = 2 \bullet (V_{SUP} - V_{DIODE}) - 2 \bullet I_{OUT} \bullet (2 \bullet r_{ONH} + r_{ONL}) \quad \text{(EQ. 16)}$$

For Voltage Tripler:

$$V_{ON\_MAX(3x)} = 3 \bullet (V_{SUP} - V_{DIODE}) - 2 \bullet I_{OUT} \bullet (3 \bullet r_{ONH} + 2 \bullet r_{ONL}) \quad \text{(EQ. 17)}$$

V_{ON} output voltage is determined by Equation 18:

$$V_{ON} = V_{FBP} \bullet \left(1 + \frac{R_8}{R_9}\right) \quad \text{(EQ. 18)}$$

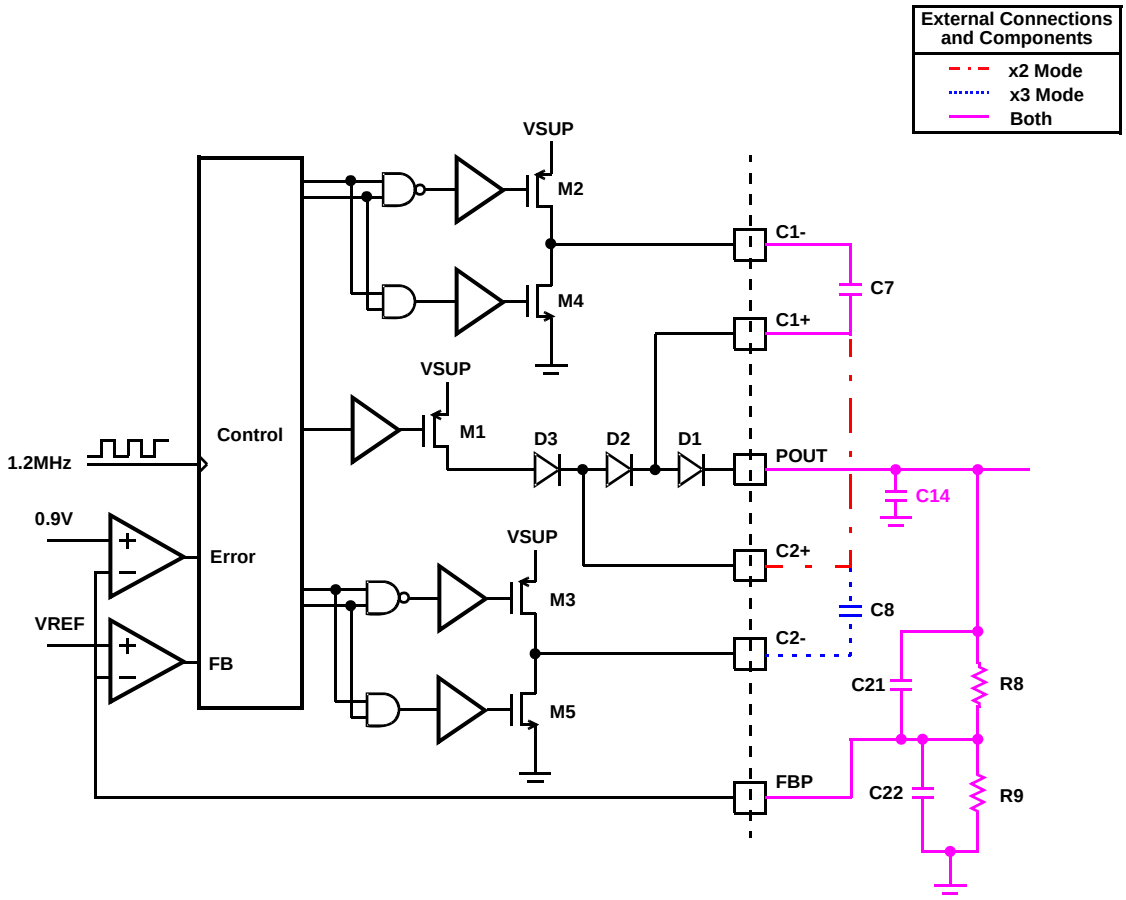


FIGURE 13. V_{ON} FUNCTION DIAGRAM

Negative Charge Pump Design Consideration

The negative charge pump consists of an internal switcher M1, M2 which drives external steering diodes D2 and D3 via a pump capacitor (C12) to generate the negative V_{OFF} supply. An internal comparator (A1) senses the feedback voltage on FBN and turns on M1 for a period up to half a CLK period to maintain $V_{(FBN)}$ in regulated operation at 0.2V. External feedback resistor R6 is referenced to V_{REF}.

Faults on V_{OFF} which cause V_{FBN} to rise to more than 0.4V, are detected by comparator (A2) and cause the fault detection system to start a fault ramp on C_{DLY} pin which will cause the chip to power down if present for more than the time TFD (see "Electrical Specification" on page 2 and also Figure 15).

The maximum V_{OFF} output voltage of a single stage charge pump is:

$$V_{OFF\_MAX}(2x) = -V_{SUP} + V_{DIODE} + 2 \bullet I_{OUT} \bullet (r_{ON}(NOUT)H + r_{ON}(NOUT)L \quad \text{(EQ. 19)}$$

R6 and R7 in the “Typical Application Diagram” on page 10 determine V_{OFF} output voltage.

$$V_{OFF} = V_{FBN} \bullet \left(1 + \frac{R7}{R6}\right) - V_{REF} \bullet \left(\frac{R7}{R6}\right) \quad \text{(EQ. 20)}$$

Improving Charge Pump Noise Immunity

Depending on PCB layout and environment, noise pick-up at the FBP and FBN inputs, which may degrade load regulation performance, can be reduced by the inclusion of capacitors across the feedback resistors (e.g. in the “Typical Application Diagram” on page 10, C21 and C22 for the positive charge pump). Set R6 • C20 = R7 • C19 with C19 ~ 100pF.

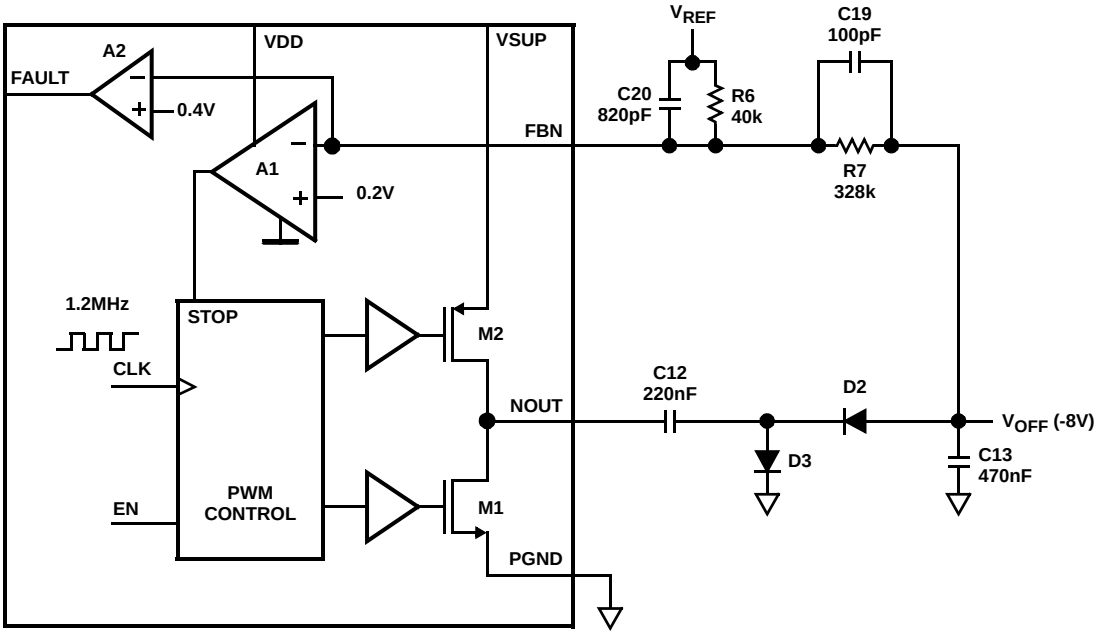


FIGURE 14. NEGATIVE CHARGE PUMP BLOCK DIAGRAM

V_{ON} Slice Circuit

The V_{ON} Slice Circuit functions as a three way multiplexer, switching the voltage on COM between ground, DRN and SRC, under control of the start-up sequence and the CTL pin.

During the start-up sequence, COM is held at ground via an NDMOS FET, with ~1k impedance. Once the start-up sequence has completed, CTL is enabled and acts as a multiplexer control such that if CTL is low, COM connects to DRN through a 30Ω internal MOSFET, and if CTL is high, COM connects to P_{OUT} internally via a 5Ω MOSFET.

The slew rate of start-up of the switch control circuit is mainly restricted by the load capacitance at COM pin as Equation 21:

$$\frac{\Delta V}{\Delta t} = \frac{V_g}{(R_i \| R_L) \times C_L} \quad \text{(EQ. 21)}$$

RWhere V_g is the supply voltage applied to DRN or voltage at P_{OUT}, which range is from 0V to 36V. R_i is the resistance between COM and DRN or P_{OUT} including the internal MOSFET $r_{DS(On)}$, the trace resistance and the resistor inserted, R_L is the load resistance of switch control circuit, and C_L is the load capacitance of switch control circuit.

In the “Typical Application Diagram” on page 10, R10, R11 and C15 give the bias to DRN based on Equation 22:

$$V_{DRN} = \frac{V_{ON} \cdot R_{11} + AVDD \cdot R_{10}}{R_{10} + R_{11}} \quad \text{(EQ. 22)}$$

And R12 can be adjusted to adjust the slew rate.

Start-Up Sequence

Figure 15 shows a detailed start up sequence waveform. For a successful power up, there should be 6 peaks at V_{CDLY}. When a fault is detected, the device will latch off until either EN is toggled or the input supply is recycled.

When the input is higher than 2.75V; if either EN or ENL is H, V_{REF} turns on. If ENL is H, V_{LOGIC} turns on. If EN is H, an internal current source starts to charge C_{CDLY} to an upper threshold using a fast ramp followed by a slow ramp. Several more ramps follow, during which time the device checks for fault conditions. If a fault is found, the sequence is halted.

Initially the boost is not enabled so A_{VDD} rises to V_{IN} - V_{DIODE} through the output diode. Hence, there is a step at A_{VDD} during this part of the start up sequence. If this step is not desirable, an external PMOS FET can be used to delay the output until the boost is enabled internally. The delayed output appears at A_{VDD}.

A_{VDD} soft-starts at the beginning of the third ramp. The soft-start ramp depends on the value of the C_{DLY} capacitor. The range of C_{DLY} capacitor value is from 10nF to 220nF. For C_{DLY} of 220nF, the soft-start time is ~8ms.

V_{OFF} turns on at the start of the fourth peak, at the same time DELB gate goes low to turn on the external PMOS to generate a delayed A_{VDD} output.

V_{ON} is enabled at the beginning of the sixth ramp.

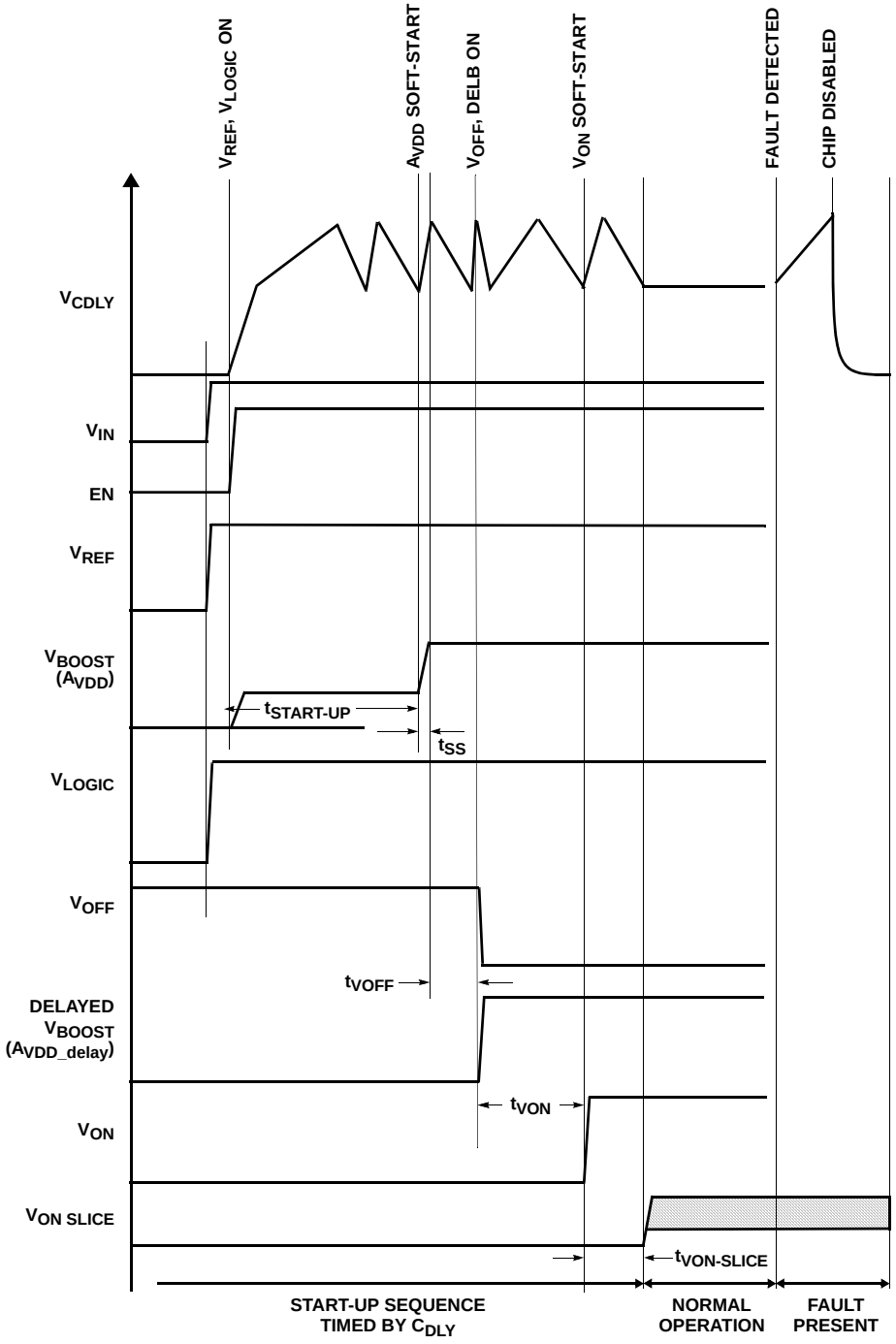
Once the start-up sequence is complete, the voltage on the C_{DLY} capacitor remains at 1.15V until either a fault is detected or the EN pin is disabled. If a fault is detected, the voltage on C_{DLY} rises to 2.4V at which point the chip is disabled until the power is cycled or enable is toggled.

A_{VDD_delay} Generation Using DELB

DELB pin is an open drain internal N-FET output used to drive an external optional P-FET to provide a delayed A_{VDD} supply which also has no initial pedistal voltage (see Figure 15 and compare the A_{VDD} and $A_{VDD\_delayed}$ curves). When the part is enabled, the N-FET is held off until C_{DLY} reaches the 4th peak in the start-up sequence. During this period, the voltage potential of the source and gate of the external P-FET (M0 in application diagram) should be almost the same due to the presence of the resistor (R4) across the source and gate, hence M0 will be off. Please note that the maximum leakage of DELB in this period is 500nA. To avoid any mis-trigger, the maximum value of R4 should be less than:

$$R_{4\_max} < \frac{V_{GS(th)\_min(M0)}}{500nA} \quad \text{(EQ. 23)}$$

Where $V_{GS(th)\_min(M0)}$ is the minimum value of gate threshold voltage of M0.



NOTE: Not to scale

FIGURE 15. START-UP SEQUENCE

After C_{DLY} reaches the 4th peak, the internal N-FET is turned-on and produces an initial current output of IDELB_ON1 (~50µA). This current allows the user to control the turn-on inrush current into the A_{VDD_delay} supply capacitors by a suitable choice of C4. This capacitor can provide extra delay and also filter out any noise coupled into the gate of M0, avoiding spurious turn-on, however, C4 must not be so large that it prevents DELB reaching 0.6V by the end of the start-up sequence on C_{DLY}, else a fault time-out ramp on C_{DLY} will start. A value of 22nF is typically required for C4. The 0.6V threshold is used by the chip's fault detection system and if V(DELB) is still above 0.6V at the end of the power sequencing then a fault time-out ramp will be initiated on C_{DLY}.

When the voltage at DELB falls below ~0.6V it's current is increased to IDELB_ON2 (~1.4mA) to firmly pull the DELB voltage to ground.

If the maximum V_{GS} voltage of M0 is less than the A_{VDD} voltage being used, then a resistor may be inserted between the DELB pin and the gate of M0 such that it's potential divider action with R4 ensures the gate/source stays below VGS(M0)max. This additional resistor allows much larger values of C4 to be used, and hence longer A_{VDD} delay, without affecting the fault protection on DELB.

Component Selection for Start-up Sequencing and Fault Protection

The C_{REF} capacitor is typically set at 220nF and is required to stabilize the V_{REF} output. The range of C_{REF} is from 22nF to 1µF and should not be more than five times the capacitor on C_{DEL} to ensure correct start-up operation.

The C_{DEL} capacitor is typically 220nF and has a usable range from 47nF minimum to several microfarads – only limited by the leakage in the capacitor reaching µA levels.

C_{DEL} should be at least 1/5 of the value of C_{REF} (see above). Note with 220nF on C_{DEL} the fault time-out will be typically 50ms and the use of a larger/smaller value will vary this time proportionally (e.g., 1µF will give a fault time-out period of typically 230ms).

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that the die temperature exceeds the thermal trip point of +150°C, the device will shut down. Operation with die temperatures between +125°C and +150°C can be tolerated for short periods of time, however, in order to maximize the operating life of the IC, it is recommended that the effective continuous operating junction temperature of the die should not exceed +125°C.

Layout Recommendation

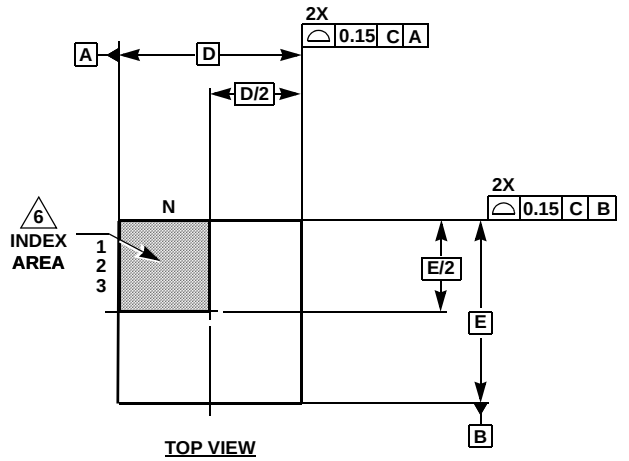
The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

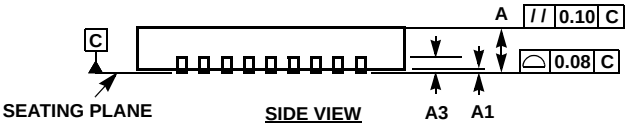
There are some general guidelines for layout:

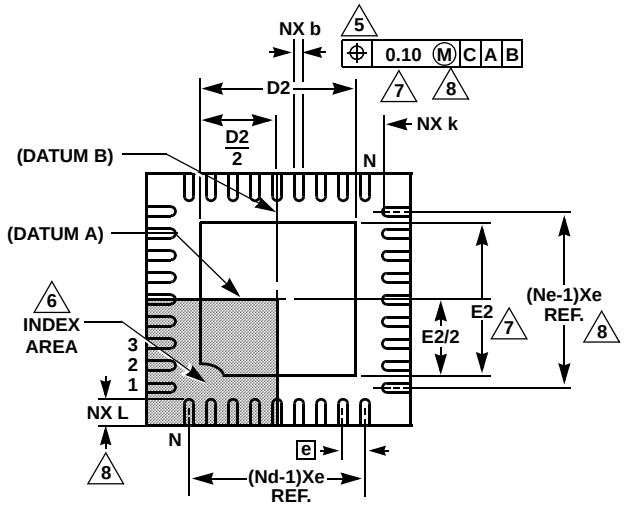
1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{REF} and V_{DC} bypass capacitors close to the pins.
3. Reduce the loop with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point.
6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC."
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. Minimize feedback input track lengths to avoid switching noise pick-up.

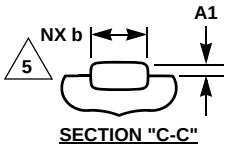
A demo board is available to illustrate the proper layout implementation.

Thin Quad Flat No-Lead Plastic Package (TQFN)









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36 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220WJJD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		
b	0.18	0.25	0.30	5, 8
D		6.00 BSC		-
D2	3.80	3.95	4.05	7, 8
E		6.00 BSC		-
E2	3.80	3.95	4.05	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.45	0.55	0.65	8
N		36		2
Nd		9		3
Ne		9		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.