Data Sheet | April 17, 2006 | FN8243.1

128-Tap DCP, 16kbit EEPROM, and I²C Serial Interface

This device integrates a 128-tap digitally controlled potentiometer, 16kbit of EEPROM, and a 2-wire I²C serial interface. The device is powered by a single 3.3V supply. The potentiometer is available with total resistance of either 10kΩ or 50kΩ.

The memory is organized in 128 pages of 16 bytes each, to reduce total programming time. All programming signals are generated on-chip.

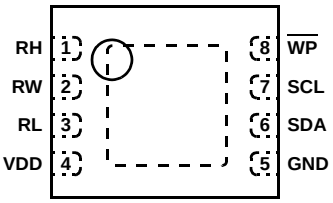
The potentiometer is implemented with a combination of CMOS switches and resistor elements. The position of the wiper can be stored in non-volatile memory and then be recalled upon a subsequent power-up. The three terminals of the potentiometer are available for use as either a variable resistor or a resistor divider.

Features

- Integrated Digitally Controlled Potentiometer
  - 128-Tap Positions
  - 10kΩ, 50kΩ Total Resistance
  - Monotonic Over Temperature
  - Non-Volatile Wiper Position Storage
  - 0 to VDD Terminal Voltage
- I²C Serial Interface
- 16kbit EEPROM
  - 50 Years Retention @ ≤ 55°C
  - 1,000,000 Cycles Endurance
- Single 3.3 ±0.3V Supply
- 3mm x 3mm Thin DFN Package – 0.8mm Max Thickness, 0.65mm Pitch
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

ISL96017
(8 LD TDFN)
TOP VIEW



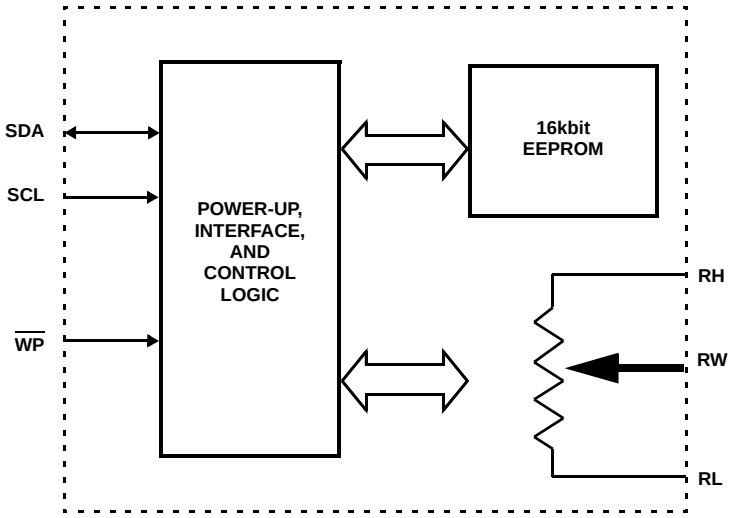
Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL96017WIRT8Z* (Note)	96017WIZ	10	-40 to 85	8 Ld 3x3 TDFN (Pb-free)	L8.3x3A
ISL96017UIRT8Z* (Note)	96017UIZ	50	-40 to 85	8 Ld 3x3 TDFN (Pb-free)	L8.3x3A

*Add "-TK" suffix for 1000 units tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	RH	“High” terminal of the DCP
2	RW	“Wiper” terminal of the DCP
3	RL	“Low” terminal of the DCP
4	VDD	Power supply
5	GND	Ground
6	SDA	Open drain serial interface data input/output
7	SCL	Open drain serial interface clock input
8	$\overline{WP}$	Hardware write protection pin. Active low. Prevents any “Write” operation to the device.

Absolute Maximum Ratings

Storage Temperature: . . . . . -65°C to 150°C
Note: All Voltages with Respect to GND
Voltage at SCL, SDA, $\overline{WP}$: . . . . . -0.3V to 4V
Voltage at RH, RW, RL: . . . . . GND to VDD
VDD . . . . . -0.3V to 4V
Lead Temperature (Soldering, 10s): . . . . . 300°C
Wiper Current. . . . . ±6mA
ESD (MIL-STD-883B, Method 3014) . . . . . >2000V
ESD (Machine Model) . . . . . >150V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA}
8 Ld TDFN Package. . . . . 90(°C/W)
Moisture Sensitivity (see Technical Brief TB363). . . . . .Level 2
Maximum Junction Temperature (Plastic Package). . . . . .150°C

Recommended Operating Conditions

Ambient Temperature . . . . . -40°C to 85°C
VDD Voltage for DCP Operation . . . . . 3.0V to 3.6V
Wiper Current . . . . . -3mA to 3mA
Power Rating 5mW

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device, at these or any other conditions above those listed in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.

Electrical Specifications

Over recommended operating conditions unless otherwise stated. All voltages with respect to GND.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
IccdSby	Standby Current at VDD	Serial interface in standby			10	µA
IccdRd	Read Current at VDD	Reading with 400kHz at SCL			1	mA
IccdWr	Write Current at VDD	Writing to EEPROM			5	mA
I_{LkgDig}	Leakage Current at Pins SDA, SCL, and $\overline{WP}$	Pin voltage from GND to VDD	-10		10	µA
I_{LkgDCP}	Leakage Current at RH, RW, RL	Pin voltage from GND to VDD	-1		1	µA
VDDRamp	VDD Power-Up Ramp Rate		0.2			V/ms
t_{DCP} (Note 13)	DCP Wiper Response Time	SCL falling edge of last bit of DCP Data Byte to wiper change		1.5		µs
t_D	Power-Up Delay	VDD above 2.6V, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
CH/CW/CL (Note 13)	RH, RW, RL Pin Capacitance			10		pF
R_{Total}	Total Resistance	W and U versions, respectively. T_A = 25°C. Measured between R_H and R_L pins.		10, 50		kΩ
	R_{Total} Tolerance	T_A = 25°C. Measured between R_H and R_L pins.	-20		20	%
R_{Wiper}	Wiper Resistance	V_{DD} = 3.3V @ 25°C. Wiper current = V_{DD}/R_{Total}		100	300	Ω
	DCP Resolution		7			Bits
DCP IN VOLTAGE DIVIDER MODE (0V at RL, VCC at RH; measured at RW unloaded)						
FSerror (Note 2, 3)	Full-Scale Error	U option	-2	-1	0	LSB
		W option	-5	-1	0	LSB
ZSerror (Note 2, 4)	Zero-Scale Error	U option	0	1	2	LSB
		W option	0	1	5	LSB
TC_V (Note 7, 13)	Ratiometric Temperature Coefficient	DCP Register between 10 hex and 6F hex		±4		ppm/°C
DNL (Note 2, 5)	Differential Non-Linearity	Monotonic over all tap positions	-0.75		0.75	LSB
INL (Note 2, 6)	Integral Non-Linearity		-1		1	LSB

Electrical Specifications Over recommended operating conditions unless otherwise stated. All voltages with respect to GND. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
DCP IN RESISTOR MODE (Measurements between RH and RW with RL not connected)						
R_{127} (Note 8)	Resistance Offset.	U version - DCP Register set to 7F hex. Measured between R_H and R_W pins.	0	0.5	2	MI
		W version - DCP Register set to 7F hex. Measured between R_H and R_W pins.		1	5	MI
TC_R (Note 11,13)	Resistance Temperature Coefficient			±100		ppm/°C
RDNL (Note 8,9)	Resistance Differential Non-Linearity		-0.75		0.75	MI (Note 1)
RINL (Note 8,10)	Resistance Integral Non-Linearity		-1		1	MI (Note 1)
EEPROM SPECS						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	At 55°C	50			Years
t_{WC} (Note 12)	Non-Volatile Write Cycle Time			6	12	ms
SERIAL INTERFACE SPECS						
V_{IL}	$\overline{WP}$, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3* VDD	V
V_{IH}	$\overline{WP}$, SDA and SCL Input Buffer HIGH Voltage		0.7* VDD		VDD +0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05* VDD			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin	$\overline{WP}$, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs.	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of VDD, until SDA exits the 30% to 70% of VDD window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of VCC during a STOP condition, to SDA crossing 70% of VDD during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of VDD crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of VDD crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of VDD	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of VDD to SCL falling edge crossing 70% of VDD	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of VDD window, to SCL rising edge crossing 30% of VDD	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of VDD to SDA entering the 30% to 70% of VDD window	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of VCC, to SDA rising edge crossing 30% of VDD	600			ns

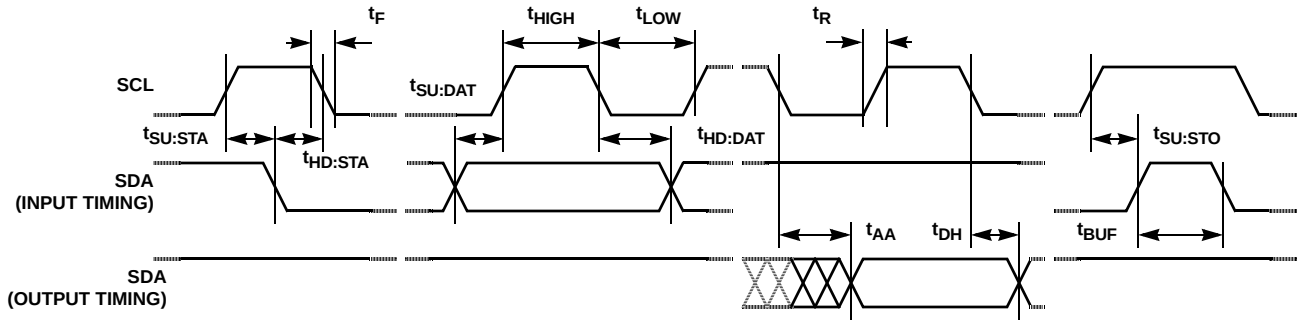
Electrical Specifications Over recommended operating conditions unless otherwise stated. All voltages with respect to GND. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of VDD	600			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of VDD, until SDA enters the 30% to 70% of VDD window	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of VDD	20+ 0.1*Cb		250	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of VDD	20+ 0.1*Cb		250	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ
$t_{SU:WP}$	$\overline{WP}$ Setup Time	Before START condition			600	ns
$t_{HD:WP}$	$\overline{WP}$ Hold Time	After STOP condition			600	ns

NOTES:

2. Typical values are for T_A = 25°C and V_{DD} = 3.3V.
3. LSB = $(V(RW)_{127} – V(RW)_0)/127$. $V(RW)_{127}$ and $V(RW)_0$ are the voltage at pin RW for the DCP Register set to 7F hex and 00 hex respectively.
4. FSerror = $(V(RW)_{127} – VDD)/LSB$
5. ZSerror = $V(RW)_0/LSB$
6. DNL = $[(V(RW)_i – V(RW)_{i-1})/LSB] – 1$, for i from 1 to 127. i is the DCP Register setting.
7. INL = $[V(RW)_i – i * LSB – V(RW)_0]/LSB$, for I = 1 to 127.
8. $TC_V = \frac{[Max(V(RW)i) – Min(V(RW)i)]}{(Max(V(RW)i) + Min(V(RW)i))/2} \times \frac{10^6}{125°C}$ for i = 16 to 111, and T = -40°C to 85°C
9. MI = $(R_0 – R_{127})/127$. MI is minimum increment. R_0 and R_{127} are the resistances between RH and RW with the DCP Register set to 00 hex and 7F hex, respectively.
10. RDNL = $(R_i – R_{i-1})/MI – 1$, for i from 1 to 111. i is the DCP Register setting.
11. RINL = $[R_i – (MI * i) – R_{127}]/MI$, for i from 1 to 111.
12. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{1 \times 10^6}{125°C}$; for i = 1 to 111, and T = -40°C to 85°C
13. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
14. Parameter is not 100% tested.

I^2C Timing Diagram



Typical Performance Curves

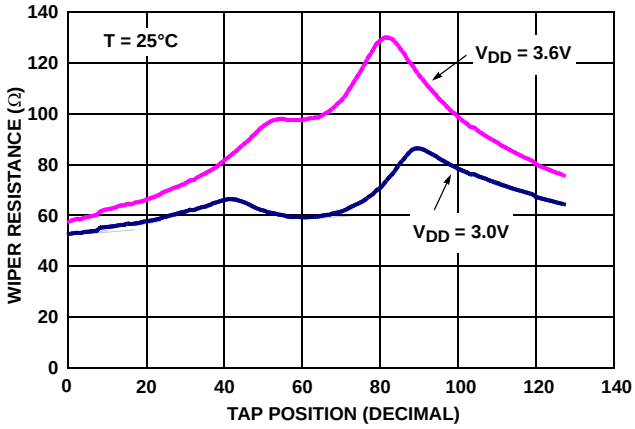


FIGURE 1. WIPER RESISTANCE vs TAP POSITION FOR 10kΩ (W)

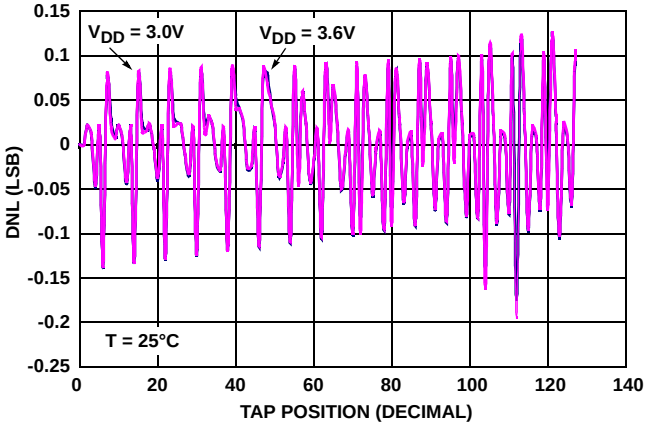


FIGURE 2. DNL vs TAP POSITION FOR 10kΩ (W)

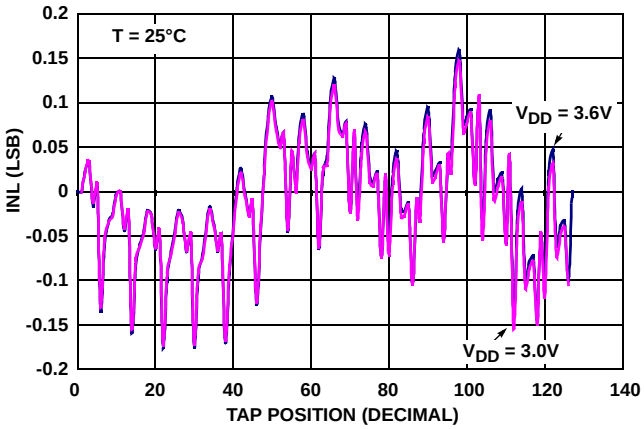


FIGURE 3. INL vs TAP POSITION FOR 10kΩ (W)

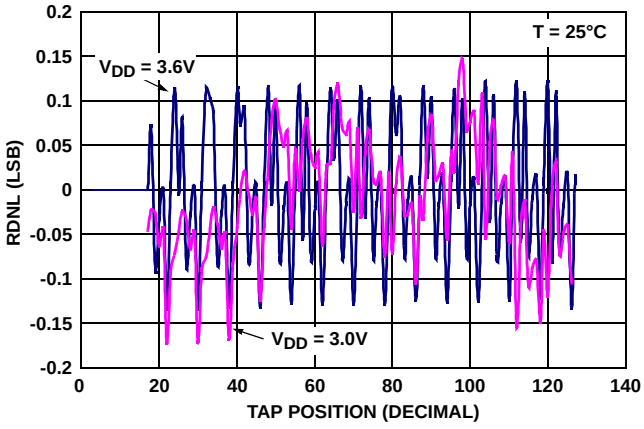


FIGURE 4. RDNL vs TAP POSITION FOR 10kΩ (W)

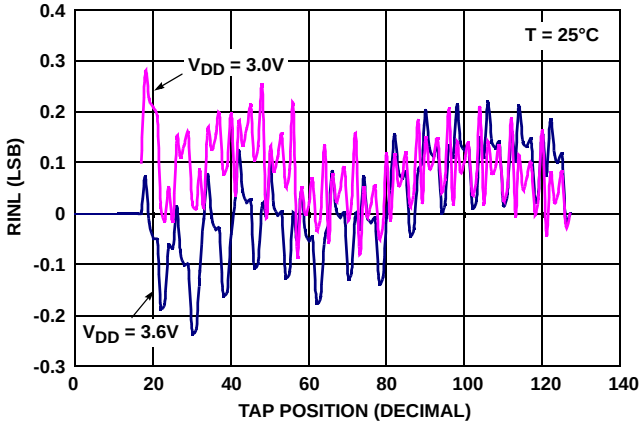


FIGURE 5. RINL vs TAP POSITION FOR 10kΩ (W)

Principles of Operation

This device combines a DCP, 16kbit non-volatile memory, and an I^2C serial interface providing direct communication between a host and the DCP and memory.

DCP Description

The DCP has 10kΩ or 50kΩ nominal total resistance and 128 taps. It is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP, the RH and RL pins, are equivalent to the fixed terminals of a mechanical potentiometer. The RW pin is connected to intermediate nodes, and it is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by a 7-bit volatile DCP Register. When the DCP Register contains all zeroes (00 hex, or "R_0"), its wiper terminal, RW, is closest to its RL terminal. When the DCP Register contains all ones (7F hex, or "R_{127}"), its wiper terminal is closest to its RH terminal. As the value of the DCP Register increases from all zeroes to all ones, the wiper moves monotonically from the position closest to RL to the closest to RH. Therefore, the resistance between RH and RW decreases monotonically from R_0 to R_{127}, while the resistance between RW and RL increases monotonically from R_{127} to R_0.

While the device is being powered up, the DCP Register is reset to 40 hex (64 decimal). Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading, the device reads the value stored on the non-volatile Initial Value Register (IVR) and loads it into the DCP Register.

Memory Description

This device contains 2048 non-volatile bytes organized in 128 pages of 16 bytes each. This allows writing 16 bytes on a single I^2C interface operation, followed by a single internal non-volatile write cycle. The memory is accessed by I^2C interface operations with addresses 000 hex through 7FF hex.

Bytes at addresses 000 hex through 7FB hex are available to the user as general purpose memory. The byte at address 7FF hex, IVR, contains the initial value loaded at power-up into the volatile DCP Register. The byte at address 7FE hex controls the access to the DCP byte (See "Access to DCP Register and IVR"). Bytes at addresses 7FC hex and 7FD hex, are reserved, which means that they should not be written, and their value should be ignored if they are read. (See Table 1).

Access to DCP Register and IVR

The volatile DCP Register and the non-volatile (IVR) can be read or written directly using the I^2C serial interface, with Address Byte 07FF hex.

The MSB of the byte at address 7FE hex is called "OnlyVolatile" and controls the access to the DCP Register and IVR. This bit is volatile and it's reset to "0" at power up.

The Data Byte read from memory address 7FF hex, is from the DCP register when the "OnlyVolatile" bit is "1", and from the IVR when this bit is "0".

The Data Byte of a Write operation to memory address 7FF hex is written only to the DCP Register when the "OnlyVolatile" bit is "1", and it's written to both the DCP Register and the IVR when this bit is "0".

When writing to the "OnlyVolatile" bit at address 7FE hex, the seven LSBs of the Data Byte must be all zeros.

Writing to address 7FE hex and 7FF hex can be done in two Write operations, or one Write operation with two Data Bytes.

See next sections for interface protocol description.

TABLE 1. ISL96017 MEMORY MAP

Address	Data Bits								Function
7FFh	0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	IVR, DCP
7FEh	OV	0	0	0	0	0	0	0	Access Control
7FDh	Reserved								
7FCh	Reserved								
7FBh	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	General Purpose Memory
↓									↓
000h									

Note: OV = "Only Volatile". All other bits in register 7FEh must be 0.

I²C Serial Interface

This device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, this device operates as a slave device in all applications. All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 6). On power up, the SDA pin is in the input mode. All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 6). A START condition is ignored during the power up sequence and during internal non-volatile write cycles. All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 6). A STOP condition at the end of a Read operation, or at the end of a Write operation to volatile bytes only places the device in its standby mode. A STOP condition during a Write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 7). This device responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of the Address Byte. This device also responds with an ACK after receiving each Data Byte of a Write operation. The master must respond with an ACK after receiving each Data Byte of a read operation except the last one. A valid Identification Byte contains 1010 as the four MSBs. The following three bits are the MSBs of the memory address to be accessed. The LSB of the Identification Byte is the Read/Write bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 2). The complete memory address location to be accessed is a 11-bit word, since the memory has 2048 bytes. The eight LSBs are in the Address Byte.

TABLE 2. IDENTIFICATION BYTE FORMAT

1	0	1	0	A10	A9	A8	R/Wb
MSB							LSB

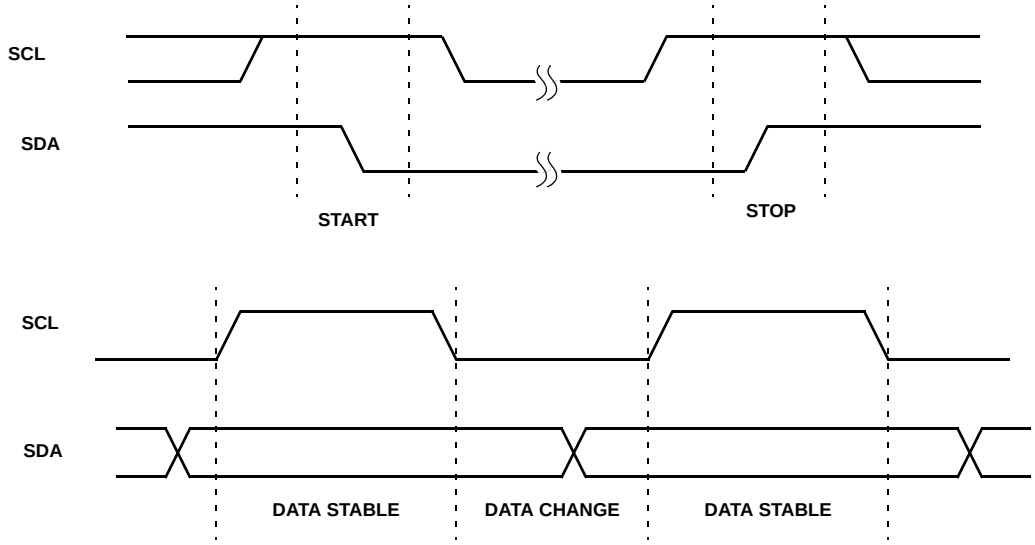


FIGURE 6. VALID DATA CHANGES, START AND STOP CONDITIONS

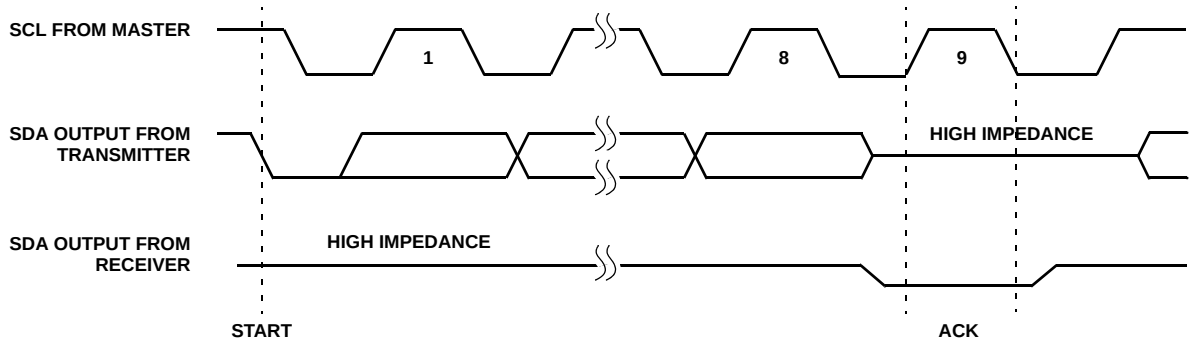


FIGURE 7. ACKNOWLEDGE RESPONSE FROM RECEIVER

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, one or more Data Bytes, and a STOP condition (See Figure 8). After each of the bytes, this device responds with an ACK. At this time, if the operation is only writing to volatile registers, then the device enters its standby state. If one or more Data Bytes are to be written to non-volatile memory, the device begins its internal write cycle to non-volatile memory. During this cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the device enters its standby state.

The memory is organized as 128 pages of 16 bytes each. This allows writing 16 bytes on a single I^2C interface operation, followed by a single internal non-volatile write cycle. The addresses of bytes within a page share the same eight MSBs, and differ on the four LSBs. For example, the first page is located at addresses 0 hex through F hex, the second page is located at addresses 10 hex through 1F hex, etc.

A Write operation with more than one Data Byte sends the first Data Byte to the memory address indicated by the three address bits of the Identification Byte plus the eight bits of the Address Byte, the second Data Byte to the following address, etc.

A single Write operation has to stay within a page. If the Address Byte corresponds to the lowest address of a page, then the Write operation can have anywhere from 1 to 16 Data Bytes. If the Address Byte corresponds to the highest address of a page, then only one byte can be written with that Write operation.

See “Access to DCP Register and IVR” for additional information.

Data Protection

The $\overline{WP}$ pin has to be at logic HIGH to perform any Write operation to the device. When $\overline{WP}$ is active (LOW) the device ignores Data Bytes of a Write operation, does not respond to them with ACK, and instead, goes to its standby state waiting for a new START condition.

A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers.

During a Write sequence, Data Bytes are loaded into an internal shift register as they are received. If the address bits in the Identification Byte plus the bits in the Address Byte are all ones, the Data Byte is transferred to the DCP Register at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte.

The STOP condition acts as a protection of non-volatile memory. Non-volatile internal write cycles are started by STOP conditions.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 9). The master initiates the operation issuing the following sequence: a START, the Identification Byte with the R/W bit set to “0”, an Address Byte which contains the LSBs of the memory address, a second START, and a second Identification Byte with the same address bits but with the R/W bit set to “1”. After each of the three bytes, this device responds with an ACK. Then this device transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the Read operation (issuing a STOP condition) following the last bit of the last Data Byte. The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the address bits in the Identification Byte plus the bits in the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte.

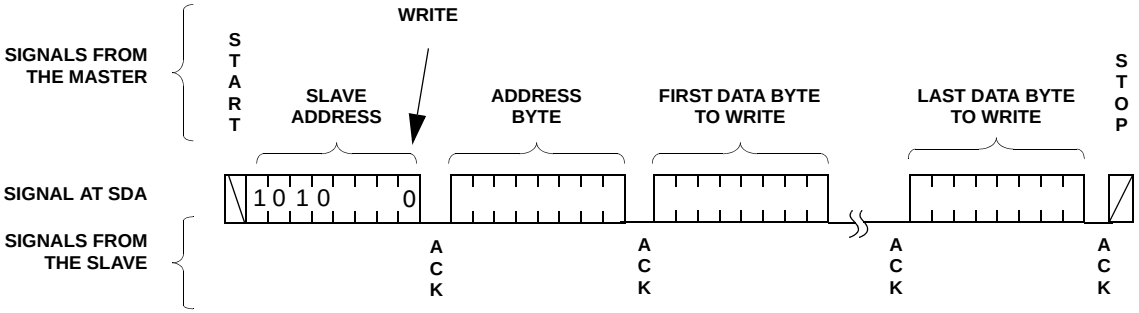


FIGURE 8. WRITE SEQUENCE

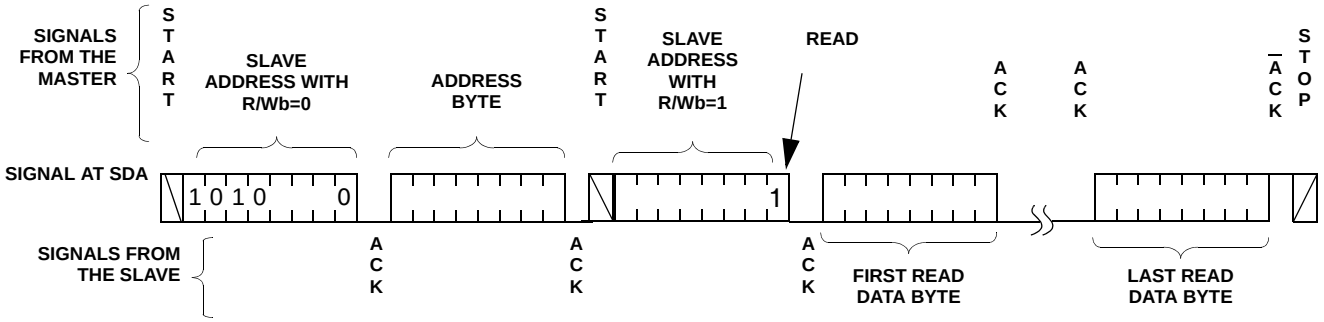


FIGURE 9. READ SEQUENCE

Applications Information

The typical application diagram is shown on Figure 10. For proper operation adding 0.1µF decoupling ceramic capacitor to Vdd is recommended. The capacitor value may vary based on expected noise frequency of the design.

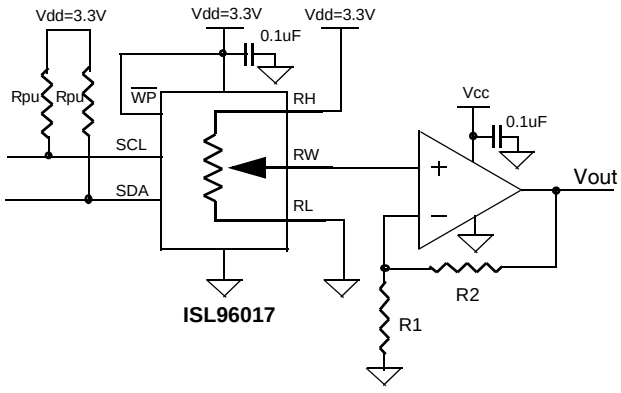
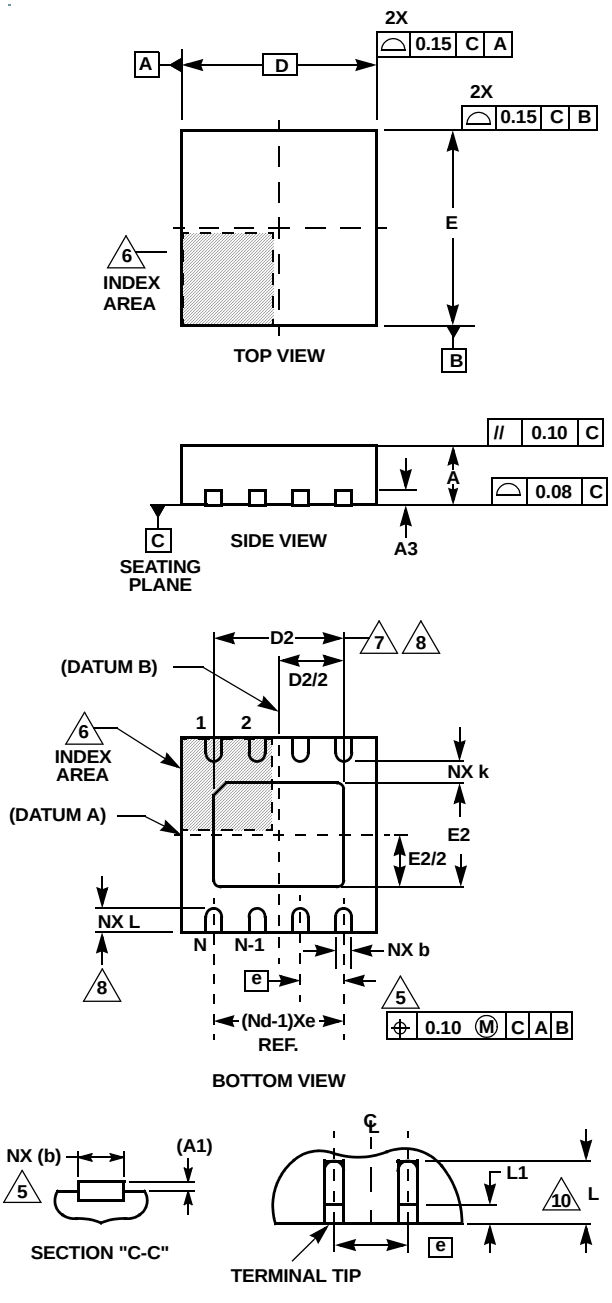


FIGURE 10. TYPICAL APPLICATION DIAGRAM FOR IMPLEMENTING ADJUSTABLE VOLTAGE REFERANCE

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3		0.20 REF		-
b	0.25	0.30	0.35	5, 8
D		3.00 BSC		-
D2	2.20	2.30	2.40	7, 8, 9
E		3.00 BSC		-
E2	1.40	1.50	1.60	7, 8, 9
e		0.65 BSC		-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N		8		2
Nd		4		3

Rev. 3 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the “L” min dimension.