Data Sheet | December 23, 2008 | FN6829.0

500mA 4.3MHz Low I_Q High Efficiency Synchronous Buck Converter

The ISL9104, ISL9104A is a 500mA, 4.3MHz step-down regulator, which is ideal for powering low-voltage microprocessors in compact devices such as PDAs and cellular phones. It is optimized for generating low output voltages down to 0.8V. The supply voltage range is from 2.7V to 6V allowing the use of a single Li+ cell, three NiMH cells or a regulated 5V input. It has guaranteed minimum output current of 500mA. A high switching frequency of 4.3MHz pulse-width modulation (PWM) allows using small external components. Under light load condition, the device operates at low I_Q skip mode with typical 20µA quiescent current for highest light load efficiency to maximize battery life, and it automatically switches to fixed frequency PWM mode under heavy load condition.

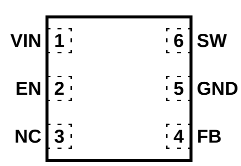
The ISL9104, ISL9104A includes a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize system efficiency and minimize the external component count. 100% duty-cycle operation allows less than 300mV dropout voltage at 500mA.

The ISL9104, ISL9104A offers internal digital soft-start, enable for power sequence, overcurrent protection and thermal shutdown functions. In addition, the ISL9104, ISL9104A offers a quick bleeding function that discharges the output capacitor when the IC is disabled.

The ISL9104, ISL9104A is offered in a 1.6x1.6mm µTDFN package. The complete converter occupies less than $0.5CM^2$.

Pinout

ISL9104, ISL9104A
(6 LD 1.6x1.6 µTDFN)
TOP VIEW



Features

- High Efficiency Integrated Synchronous Buck Regulator with up to 93% Efficiency
- 2.7V to 6.0V Supply Voltage
- 4.3MHz PWM Switching Frequency
- 500mA Guaranteed Output Current
- 3% Output Accuracy Over-Temperature and Line for Fixed Output Options
- 20µA Quiescent Supply Current in Skip Mode
- Less than 1µA Logic Controlled Shutdown Current
- 100% Maximum Duty Cycle for Lowest Dropout
- Ultrasonic Switching Frequency at Skip Mode to Prevent Audible Frequency Noise (For ISL9104A Only)
- Discharge Output Capacitor when Disabled
- Internal Digital Soft-Start
- Peak Current Limiting, Short Circuit Protection
- Over-Temperature Protection
- Chip Enable
- Small 6 Pin 1.6mmx1.6mm µTDFN Package
- Pb-Free (RoHS Compliant)

Applications

- Single Li-ion Battery-Powered Equipment
- Mobile Phones and MP3 Players
- PDAs and Palmtops
- WCDMA Handsets
- Portable Instruments

Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	OUTPUT VOLTAGE (V) (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #	ULTRASONIC FUNCTION
ISL9104IRUNZ-T	K6	3.3	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
Coming Soon ISL9104IRUJZ-T	K7	2.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
ISL9104IRUFZ-T	K8	2.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
Coming Soon ISL9104IRUDZ-T	K9	2.0	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
Coming Soon ISL9104IRUCZ-T	L0	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
ISL9104IRUBZ-T	L1	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
Coming Soon ISL9104IRUWZ-T	L2	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
ISL9104IRUAZ-T	L3	ADJ	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	NO
ISL9104AIRUNZ-T	L4	3.3	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
Coming Soon ISL9104AIRUJZ-T	L5	2.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
ISL9104AIRUFZ-T	L6	2.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
Coming Soon ISL9104AIRUDZ-T	L7	2.0	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
Coming Soon ISL9104AIRUCZ-T	L8	1.8	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
ISL9104AIRUBZ-T	L9	1.5	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
Coming Soon ISL9104AIRUWZ-T	M0	1.2	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES
ISL9104AIRUAZ-T	M1	ADJ	-40 to +85	6 Ld µTDFN	L6.1.6x1.6	YES

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

VIN, EN to GND . . . . -0.3V to 6.5V
SW to GND . . . . -1.5V to 6.5V
FB to GND (for adjustable version) . . . . -0.3V to 2.7V
FB to GND (for fixed output version) . . . . -0.3V to 3.6V

Recommended Operating Conditions

VIN Supply Voltage Range . . . . 2.7V to 6.0V
Load Current . . . . up to 500mA
Ambient Temperature Range. . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
1.6x1.6 µTDFN Package 160
Junction Temperature Range. . . . . -40°C to +125°C
Storage Temperature Range . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, V_{IN} = V_{EN} = 3.6V, L = 1.0µH, C_1 = 4.7µF, C_2 = 4.7µF, I_{OUT} = 0A (see “Typical Applications” on page 8). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Undervoltage Lockout Threshold (UVLO)	V_{UVLO}	T_A = +25°C, Rising	-	2.5	2.7	V
UVLO Hysteresis			50	150	-	mV
Quiescent Supply Current (for ISL9104 adjustable output voltage only)	I_{VIN1}	In skip mode, no load at the output, no switch, V_{IN} = 6.0V	-	20	34	µA
Quiescent Supply Current (for ISL9104A adjustable output only)	I_{VIN2}	In skip mode, no load at the output, no switch, V_{IN} = 6.0V	-	32	45	µA
Quiescent Supply Current (for ISL9104A 1.5V fixed output)		In skip mode, no load at the output, V_{IN} = 6.0V		84		µA
Shut Down Supply Current	I_{SD}	V_{IN} = 6.0V, EN = LOW	-	0.05	1	µA
OUTPUT REGULATION						
FB Voltage Accuracy (for adjustable output only)		T_A = 0°C to +85°C	-2	-	+2	%
			-2.5	-	+2.5	%
FB Voltage	V_{FB}			0.8		V
FB Bias Current (for adjustable output only)	I_{FB}	VFB = 0.75V	-	5	100	nA
Output Voltage Accuracy (for fixed output voltage only)		PWM Mode	-3		3	%
Line Regulation		V_{IN} = V_O + 0.5V to 6V (minimal 2.7V)	-	0.2	-	%/V
Load Regulation		V_{IN} =3.6V, I_O = 150mA to 500mA		0.0009		%/mA
SW						
P-Channel MOSFET ON-Resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.45	0.6	Ω
		V_{IN} = 2.7V, I_O = 200mA	-	0.55	0.72	Ω
N-Channel MOSFET ON-Resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.4	0.52	Ω
		V_{IN} = 2.7V, I_O = 200mA	-	0.5	0.65	Ω
N-Channel Bleeding MOSFET ON-Resistance				100		Ω
P-Channel MOSFET Peak Current Limit	I_{PK}	V_{IN} = 3.6V	0.75	1.00	1.25	A
Maximum Duty Cycle			-	100	-	%

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, V_{IN} = V_{EN} = 3.6V, L = 1.0µH, C_1 = 4.7µF, C_2 = 4.7µF, I_{OUT} = 0A (see “Typical Applications” on page 8). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SW Leakage Current				0.01	2	µA
PWM Switching Frequency	f_S	V_{IN} = 3.6V, T_A = -20°C to +85°C	3.6	4.3	4.9	MHz
SW Minimum On-Time			-	65	-	ns
Soft-Start-Up Time			-	1.0	-	ms
EN						
Logic Input Low			-	-	0.4	V
Logic Input High			1.4	-	-	V
Logic Input Leakage Current			-	0.1	1	µA
Thermal Shutdown			-	130	-	°C
Thermal Shutdown Hysteresis			-	30	-	°C

Typical Operating Performance

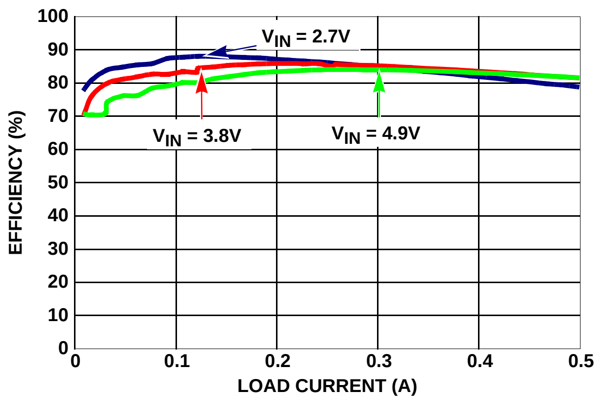


FIGURE 1. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 1.5V)

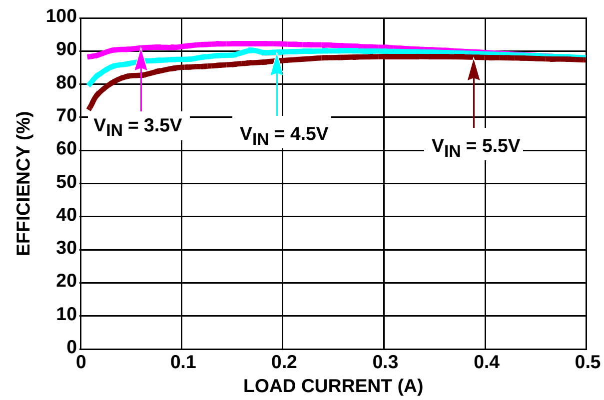


FIGURE 2. EFFICIENCY vs LOAD CURRENT (V_{OUT} = 2.5V)

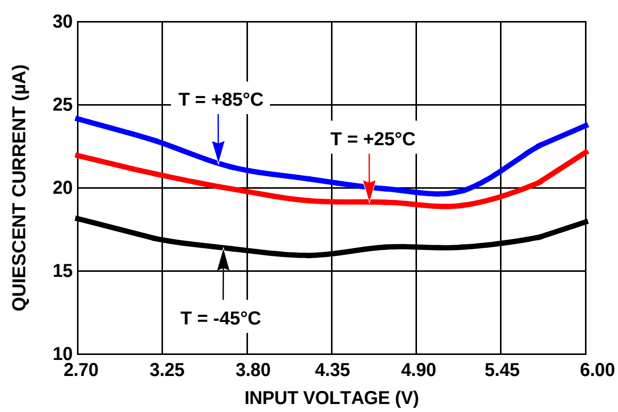


FIGURE 3. INPUT QUIESCENT CURRENT vs V_{IN} (V_{OUT} = 2.5V)

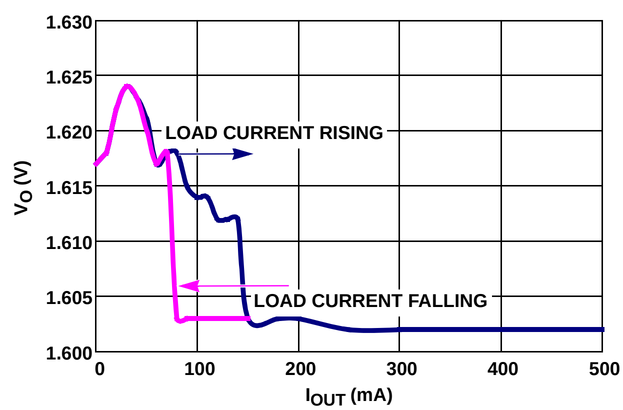


FIGURE 4. OUTPUT VOLTAGE vs LOAD CURRENT (V_{IN} = 3.6V, V_{OUT} = 1.6V)

Typical Operating Performance (Continued)

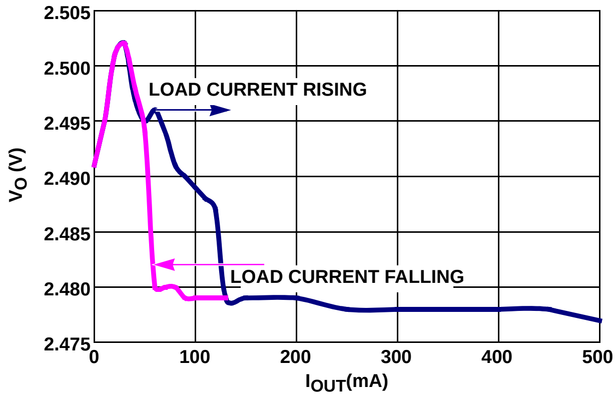


FIGURE 5. OUTPUT VOLTAGE vs LOAD CURRENT (V_{IN} = 4.0V, V_{OUT} = 2.5V)

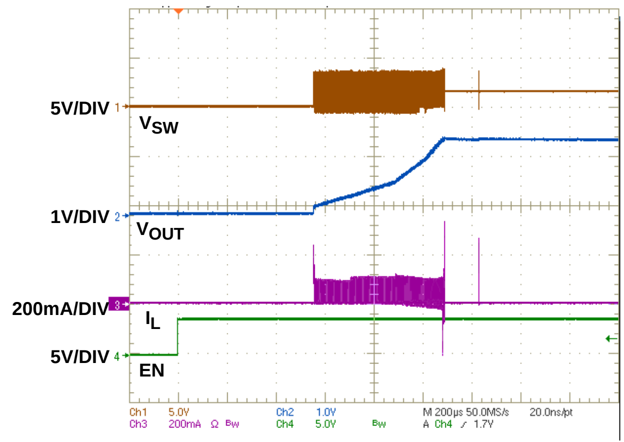


FIGURE 6. SOFT-START TO PFM MODE (V_{IN} = 3.6V, V_{OUT} = 1.5V, I_{OUT} = 0.001mA)

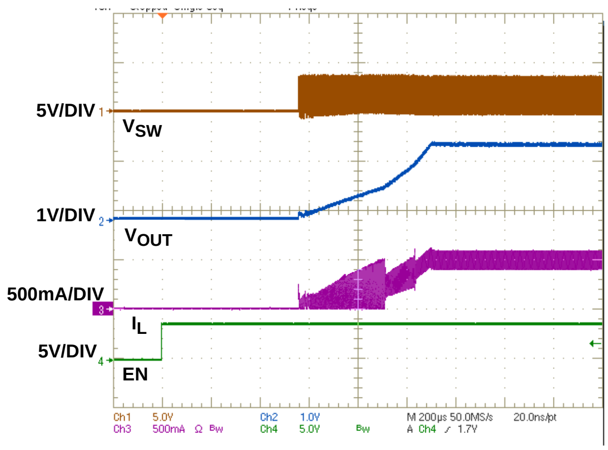


FIGURE 7. SOFT-START TO PWM MODE (V_{IN} = 3.6V, V_{OUT} = 1.5V, I_{OUT} = 500mA)

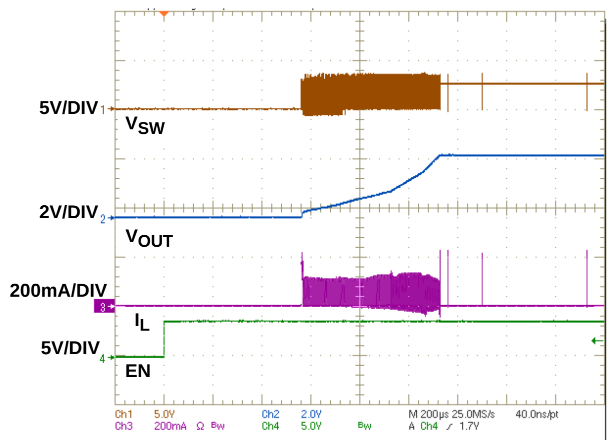


FIGURE 8. SOFT-START TO PFM MODE (V_{IN} = 3.6V, V_{OUT} = 2.5V, I_{OUT} = 0.001mA)

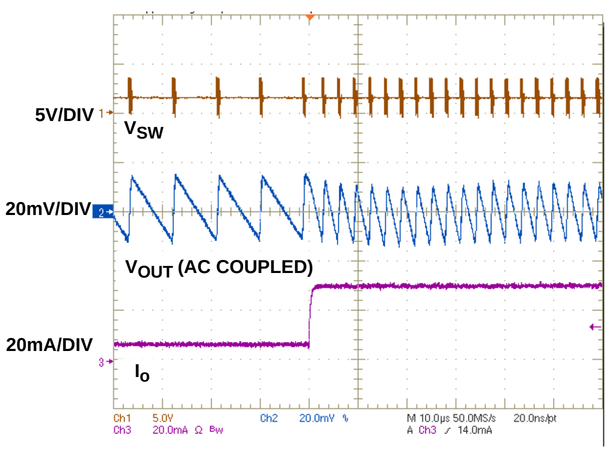


FIGURE 9. LOAD TRANSIENT IN PFM MODE (V_{IN} = 3.6V, V_{OUT} = 1.5V, 5mA TO 30mA)

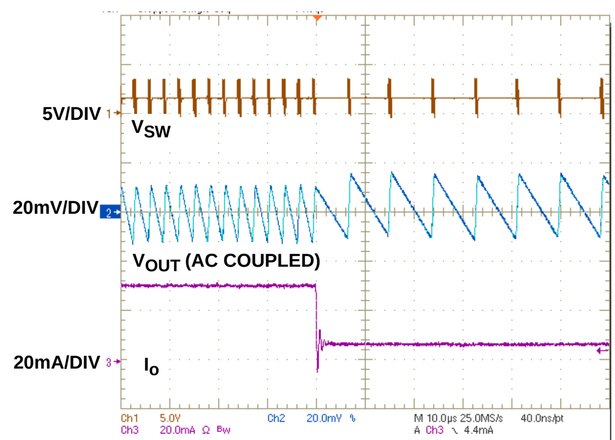


FIGURE 10. LOAD TRANSIENT IN PFM MODE (V_{IN} = 3.6V, V_{OUT} = 1.5V, 30mA TO 5mA)

Typical Operating Performance (Continued)

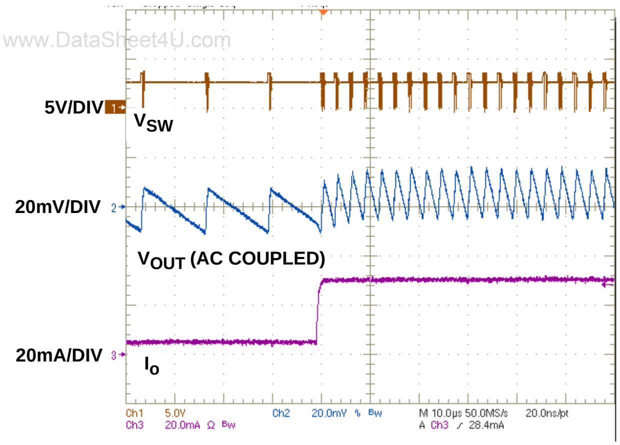


FIGURE 11. LOAD TRANSIENT IN PFM MODE (V_{IN} = 3.6V, V_{OUT} = 2.5V, 5mA TO 30mA)

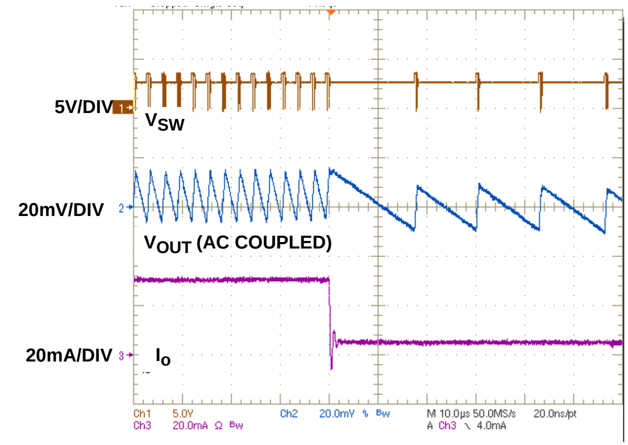


FIGURE 12. LOAD TRANSIENT IN PFM MODE (V_{IN} = 3.6V, V_{OUT} = 2.5V, 30mA TO 5mA)

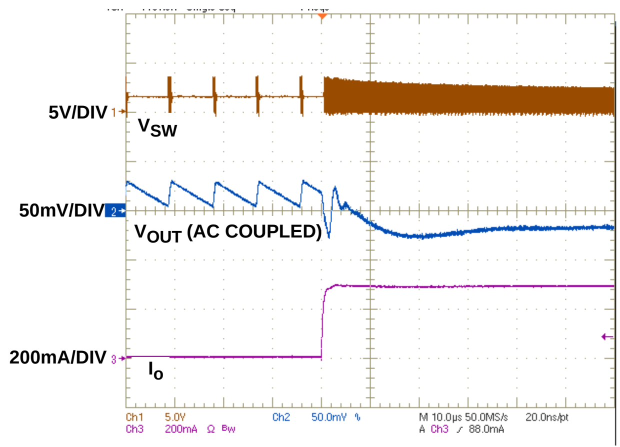


FIGURE 13. LOAD TRANSIENT FROM PFM TO PWM MODE (V_{IN} = 3.6V, V_{OUT} = 1.5V, 5mA TO 300mA)

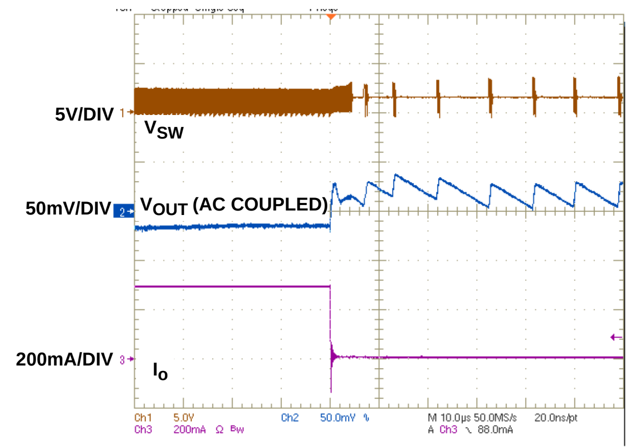


FIGURE 14. LOAD TRANSIENT FROM PWM TO PFM MODE (V_{IN} = 3.6V, V_{OUT} = 1.5V, 300mA TO 5mA)

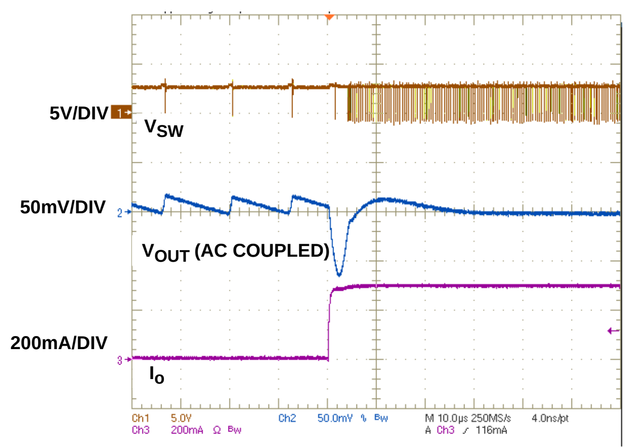


FIGURE 15. LOAD TRANSIENT FROM PFM TO PWM MODE (V_{IN} = 3.6V, V_{OUT} = 2.5V, 5mA TO 300mA)

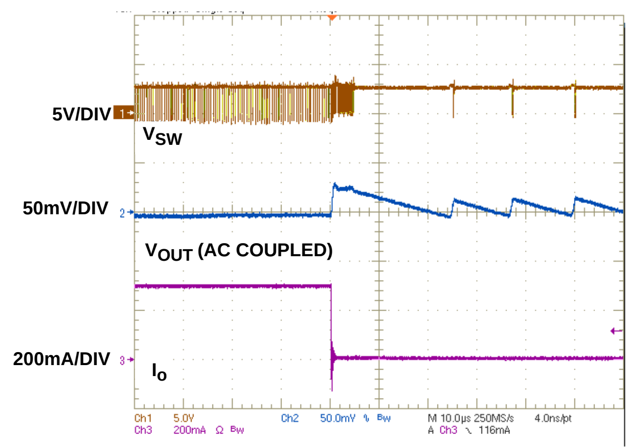


FIGURE 16. LOAD TRANSIENT FROM PWM TO PFM MODE (V_{IN} = 3.6V, V_{OUT} = 2.5V, 300mA TO 5mA)

Typical Operating Performance (Continued)

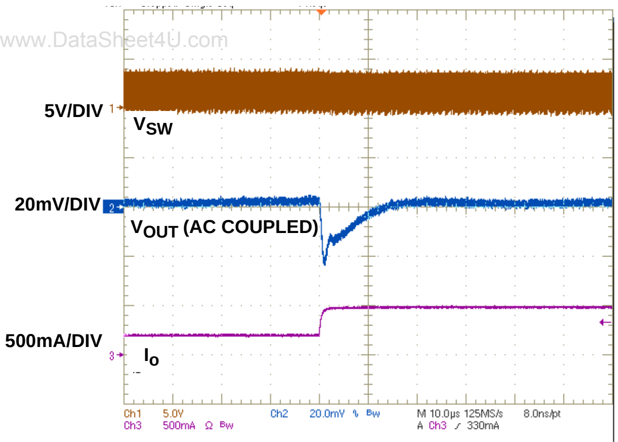


FIGURE 17. LOAD TRANSIENT IN PWM MODE (V_{IN} = 3.6V, V_O = 1.5V, 200mA TO 500mA)

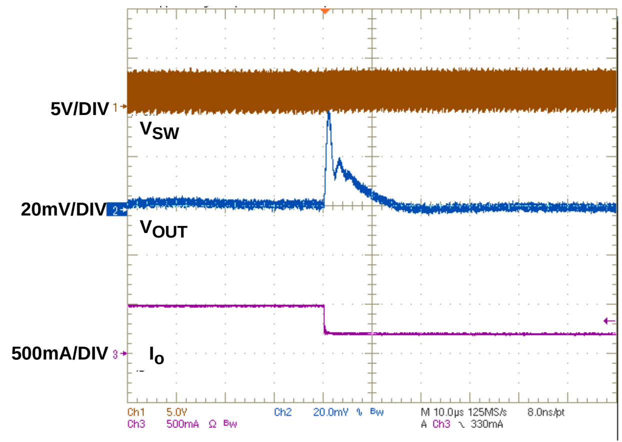


FIGURE 18. LOAD TRANSIENT IN PWM MODE (V_{IN} = 3.6V, V_O = 1.5V, 500mA TO 200mA)

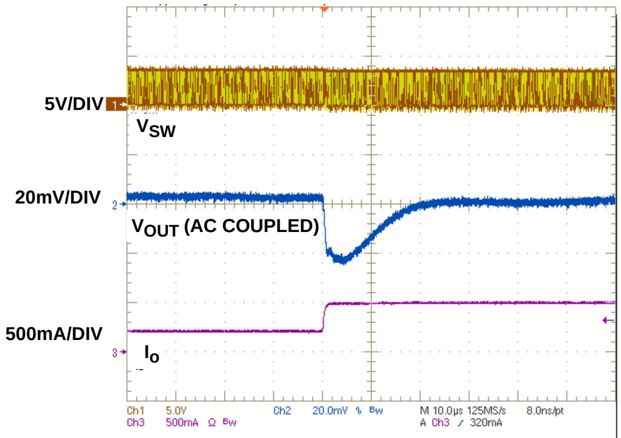


FIGURE 19. LOAD TRANSIENT IN PWM MODE (V_{IN} = 3.6V, V_O = 2.5V, 200mA TO 500mA)

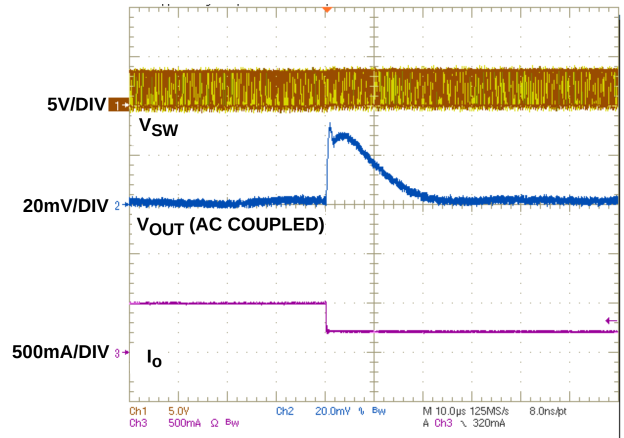


FIGURE 20. LOAD TRANSIENT IN PWM MODE (V_{IN} = 3.6V, V_O = 2.5V, 500mA TO 200mA)

Pin Descriptions

VIN

Input supply voltage. Typically connect a 4.7µF ceramic capacitor to ground.

NC

No connect, leave it floating.

EN

Regulator enable pin. Enable the device when driven to high. Shut down the chip and discharge output capacitor when driven to low. Do not leave this pin floating.

SW

Switching node connection. Connect to one terminal of inductor.

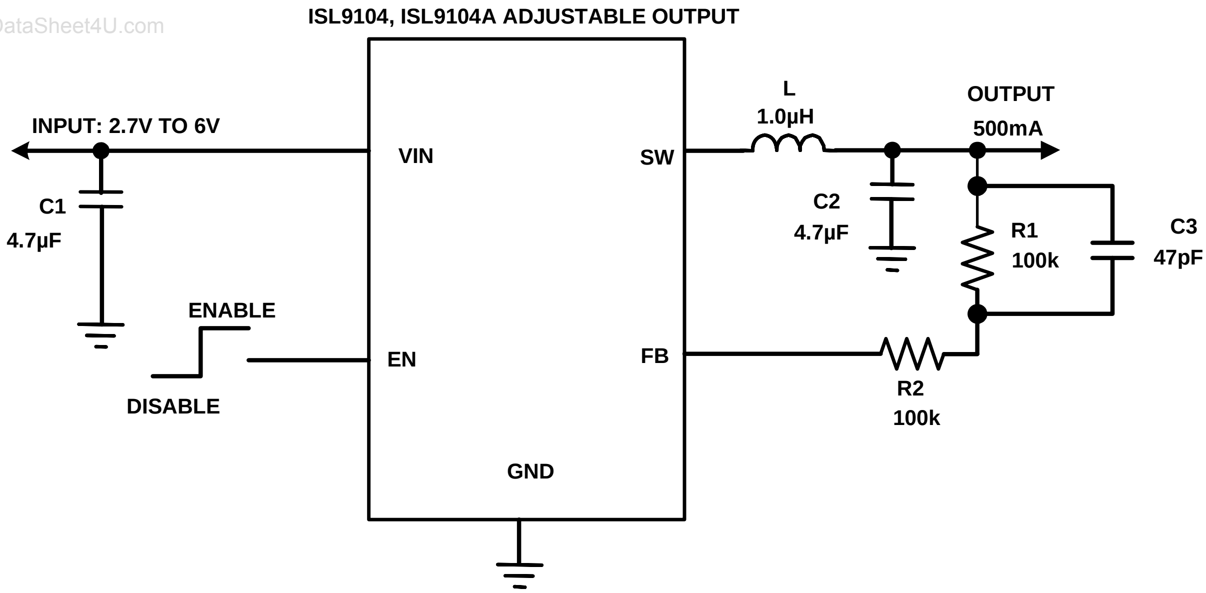
GND

Ground connection.

FB

Buck converter output feedback pin. For adjustable output version, its typical value is 0.8V and connect it to the output through a resistor divider for desired output voltage; for fixed output version, directly connect this pin to the converter output.

Typical Applications



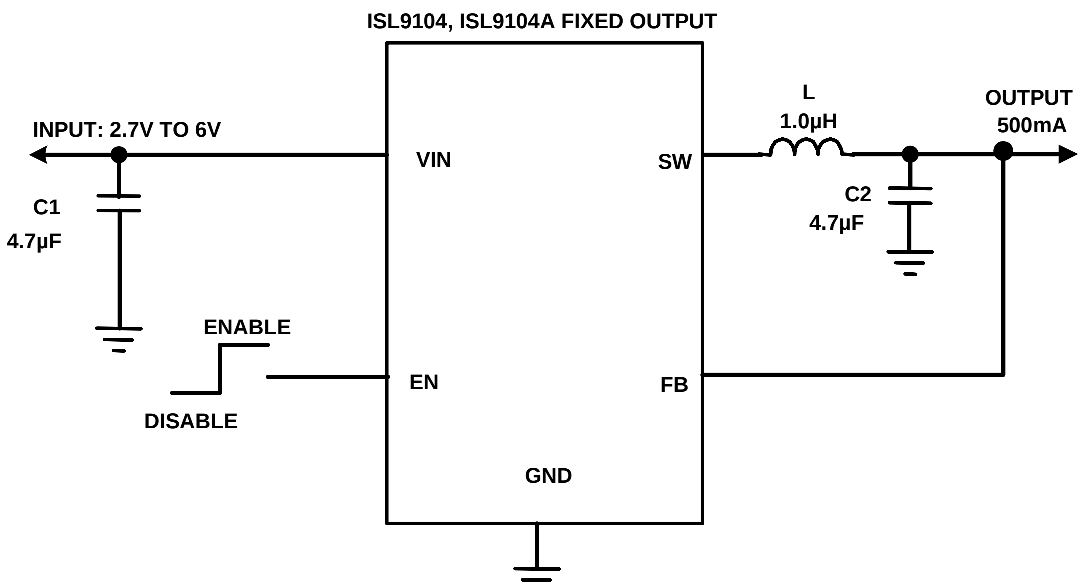
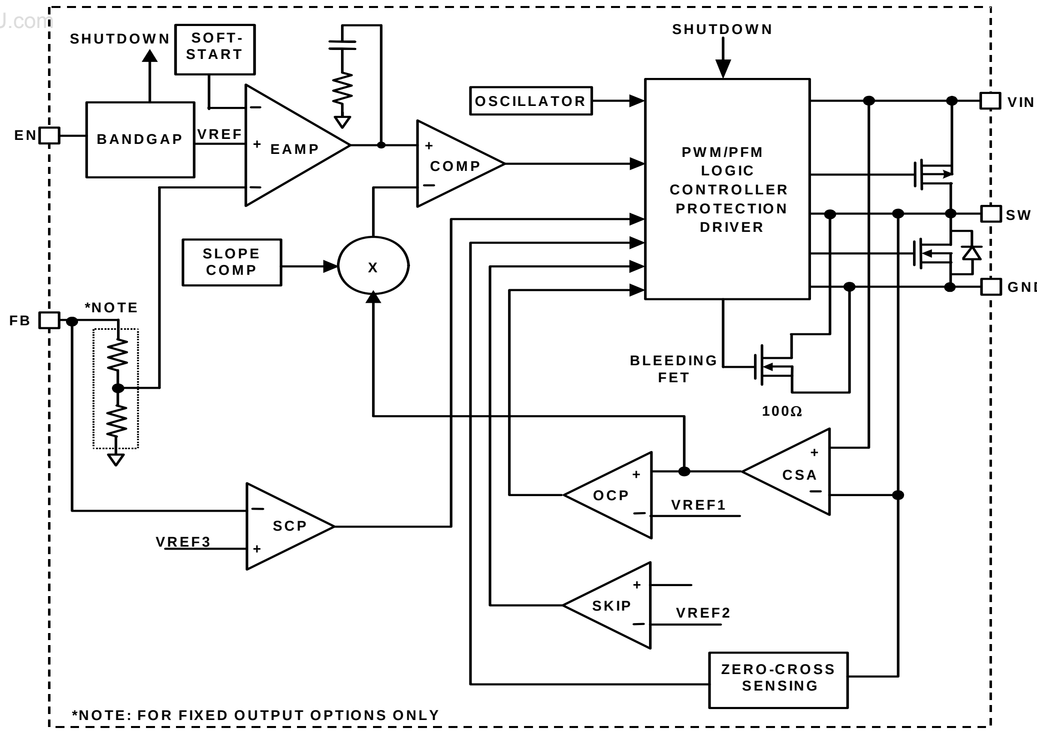


FIGURE 21. TYPICAL APPLICATIONS DIAGRAM

Note: For adjustable output version, the internal feedback resistor divider is disabled and the FB pin is directly connected to the error amplifier.

PARTS	DESCRIPTION	MANUFACTURERS	PART NUMBER	SPECIFICATIONS	SIZE
L	Inductor	KEMET	LB3218-T1R0MK	1.0µH/1.0A/60mΩ	3.2mmx1.8mmx1.8mm
C1, C2	Input and output capacitor	Murata	GRM188R60J475KE19D	4.7µF/6.3V, X5R	0603
C3	Capacitor	KEMET	C0402C470J5GACTU	47pF/50V	0402
R1, R2	Resistor	Various	-	100kΩ, SMD, 1%	0402

Block Diagram



NOTE: For Adjustable output version, the internal feedback resistor divider is disabled and the FB pin is directly connected to the error amplifier.

FIGURE 22. FUNCTIONAL BLOCK DIAGRAM

Theory of Operation

The ISL9104, ISL9104A is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at typical 4.3MHz fixed switching frequency under heavy load condition to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator can automatically enter the skip mode (PFM mode) to reduce the switching frequency to minimize the switching loss and to maximize the battery life. The quiescent current under skip mode under no load and no switch condition is typically only 20µA. The supply current is typically only 0.05µA when the regulator is disabled.

PWM Control Scheme

The ISL9104, ISL9104A uses the peak-current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 22 shows the circuit functional block diagram. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-Channel MOSFET when it is turned on and the Current Sense Amplifier (CSA). The control reference for the current loops comes from the Error Amplifier (EAMP) of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the P-Channel MOSFET starts ramping up. When the sum of the CSA output and the compensation slope reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-Channel MOSFET and to turn on the N-Channel MOSFET. The N-MOSFET remains on till the end of the PWM cycle. Figure 23 shows the typical operating waveforms during the normal PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the CSA output.

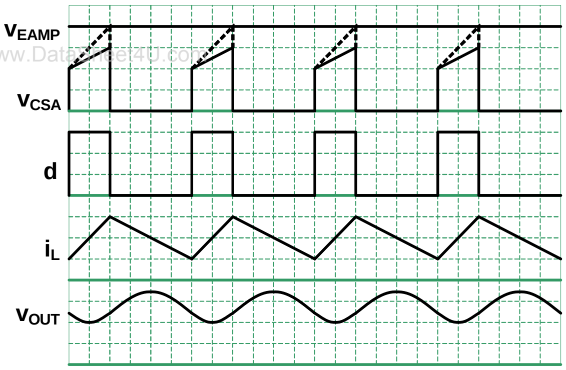


FIGURE 23. PWM OPERATION WAVEFORMS

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the FB pin. The soft-start block only affects the operation during the start-up and will be discussed separately in “Soft-Start” on page 11. The EAMP is a transconductance amplifier, which converts the voltage error signal to a current output. The voltage loop is internally compensated by a RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage.

Skip Mode (PFM Mode)

Under light load condition, ISL9104, ISL9104A automatically enters a pulse-skipping mode to minimize the switching loss by reducing the switching frequency. Figure 24 illustrates the skip mode operation. A zero-cross sensing circuit (as shown in Figure 22) monitors the current flowing through SW node for zero crossing. When it is detected to cross zero for 16-consecutive cycles, the regulator enters the skip mode.

During the 16-consecutive cycles, the inductor current could be negative. The counter is reset to zero when the sensed current flowing through SW node does not cross zero during any cycle within the 16-consecutive cycles. Once ISL9104, ISL9104A enters the skip mode, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 22. Each pulse cycle is still synchronized by the PWM clock. The P-Channel MOSFET is turned on at the rising edge of clock and turned off when its current reaches ~20% of the peak current limit. As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle over cycle. When the output voltage is sensed to reach 1.5% above its nominal voltage, the P-Channel MOSFET is turned off immediately and the inductor current is fully discharged to zero and stays at zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-Channel MOSFET will be turned on again, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage is sensed to drop below 1.5% of its nominal voltage value.

Enable

The enable (EN) pin allows user to enable or disable the converter for purposes such as power-up sequencing. With EN pin pulled to high, the converter is enabled and the internal reference circuit wakes up first and then the soft start-up begins. When EN pin is pulled to logic low, the converter is disabled, both P-Channel MOSFET and N-Channel MOSFETS are turned off, and the output capacitor is discharged through internal discharge path.

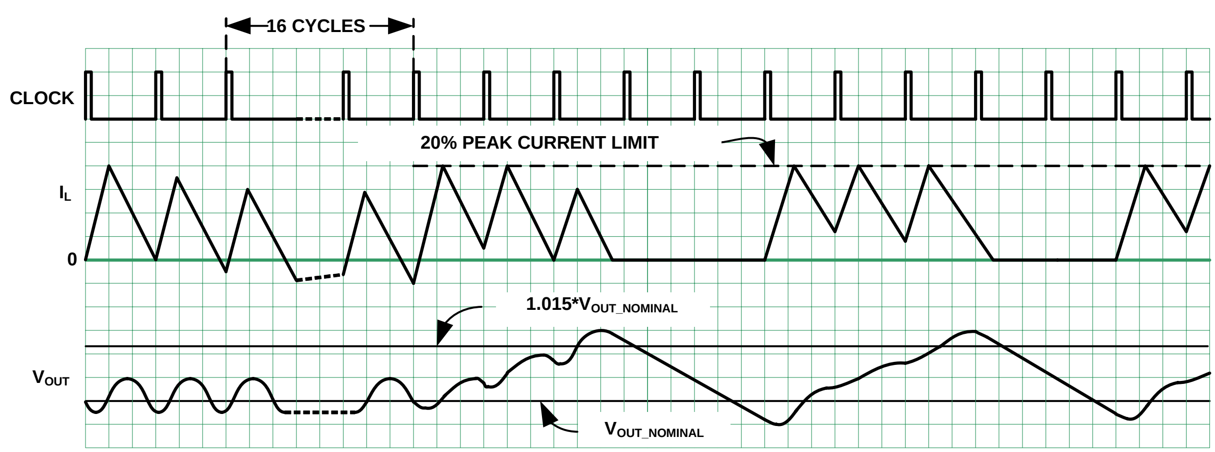


FIGURE 24. SKIP MODE OPERATION WAVEFORMS

Overcurrent Protection

The overcurrent protection is provided on ISL9104, ISL9104A when overload condition happens. It is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 22. When the current at P-Channel MOSFET is sensed to reach the current limit, the OCP comparator is trigged to turn off the P-Channel MOSFET immediately.

Short-Circuit Protection

ISL9104, ISL9104A has a Short-Circuit Protection (SCP) comparator, which monitors the FB pin voltage for output short-circuit protection. When the output voltage is sensed to be lower than a certain threshold, the SCP comparator reduces the PWM oscillator frequency to a much lower frequency to protect the IC from being damaged.

Undervoltage Lockout (UVLO)

When the input voltage is below the Undervoltage Lock Out (UVLO) threshold, ISL9104, ISL9104A is disabled.

Soft-Start

The soft-start feature eliminates the inrush current during the circuit start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion.

Low Dropout Operation

The ISL9104, ISL9104A features low dropout operation to maximize the battery life. When the input voltage drops to a level that ISL9104, ISL9104A can no longer operate under switching regulation to maintain the output voltage, the P-Channel MOSFET is completely turned on (100% duty cycle). The dropout voltage under such condition is the product of the load current and the ON-resistance of the P-Channel MOSFET. Minimum required input voltage V_{IN} under this condition is the sum of output voltage plus the voltage drop cross the inductor and the P-Channel MOSFET switch.

Thermal Shut Down

The ISL9104, ISL9104A provides built-in thermal protection function. The thermal shutdown threshold temperature is +130°C (typ) with a 30°C (typ) hysteresis. When the internal temperature is sensed to reach +130°C, the regulator is completely shut down and as the temperature drops to +100°C (typ), the ISL9104, ISL9104A resumes operation starting from the soft-start.

Applications Information

Inductor and Output Capacitor Selection

To achieve better steady state and transient response, ISL9104, ISL9104A typically uses a 1.0µH inductor. The peak-to-peak inductor current ripple can be expressed in Equation 1:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \qquad \text{(EQ. 1)}$$

In Equation 1, usually the typical values can be used but to have a more conservative estimation, the inductance should consider the value with worst case tolerance; and for switching frequency f_S, the minimum f_S from the "Electrical Specifications" table on page 3 can be used.

To select the inductor, its saturation current rating should be at least higher than the sum of the maximum output current and half of the delta calculated from Equation 1. Another more conservative approach is to select the inductor with the current rating higher than the P-Channel MOSFET peak current limit.

Another consideration is the inductor DC resistance since it directly affects the efficiency of the converter. Ideally, the inductor with the lower DC resistance should be considered to achieve higher efficiency.

Inductor specifications could be different from different manufacturers so please check with each manufacturer if additional information is needed.

For the output capacitor, a ceramic capacitor can be used because of the low ESR values, which helps to minimize the output voltage ripple. A typical value of 4.7µF/6.3V ceramic capacitor should be enough for most of the applications and the capacitor should be X5R or X7R.

Input Capacitor Selection

The main function for the input capacitor is to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current from flowing back to the battery rail. A 4.7µF/6.3V ceramic capacitor (X5R or X7R) is a good starting point for the input capacitor selection.

Output Voltage Setting Resistor Selection

For ISL9104, ISL9104A adjustable output option, the voltage resistors, R_1 and R_2, as shown in Figure 21, set the desired output voltage values. The output voltage can be calculated using Equation 2:

$$V_O = V_{FB} \bullet \left(1 + \frac{R_1}{R_2}\right) \qquad \text{(EQ. 2)}$$

where V_{FB} is the feedback voltage (typically it is 0.8V). The current flowing through the voltage divider resistors can be calculated as $V_O/(R_1 + R_2)$, so larger resistance is desirable to minimize this current. On the other hand, the FB pin has leakage current that will cause error in the output voltage setting. The leakage current has a typical value of 0.1µA. To minimize the accuracy impact on the output voltage, select the R_2 no larger than 200kΩ.

For adjustable output versions, C3 (shown in Figure 21) is highly recommended for improving stability and achieving better transient response.

Table 1 provides the recommended component values for some output voltage options.

TABLE 1. RECOMMENDED IISL9104, ISL9104A ADJUSTABLE OUTPUT VERSION CIRCUIT CONFIGURATION vs V_{OUT}

VOUT (V)	L (µH)	C2 (µF)	R1 (kΩ)	C3 (pF)	R2 (kΩ)
0.8	1.0	4.7	0	N/A	N/A
1.0	1.0	4.7	44.2	100	178
1.2	1.0	4.7	80.6	47	162
1.5	1.0	4.7	84.5	47	97.6
1.8	1.0	4.7	100	47	80.6
2.5	1.0	4.7	100	47	47.5
2.8	1.0	4.7	100	47	40.2
3.3	1.0	4.7	102	47	32.4

Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well, especially under the high current high switching frequency condition.

For ISL9104, ISL9104A, the power loop is composed of the output inductor L, the output capacitor C_{OUT}, the SW pin and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide; the same type of traces should be used to connect the VIN pin, the input capacitor C_{IN} and its ground.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the voltage feedback trace and other noise sensitive traces away from these noisy traces.

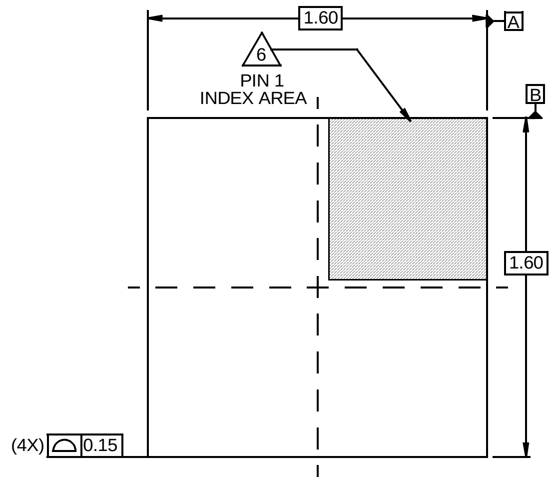
The input capacitor should be placed as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible as well. In addition, a solid ground plane is helpful for EMI performance.

Package Outline Drawing

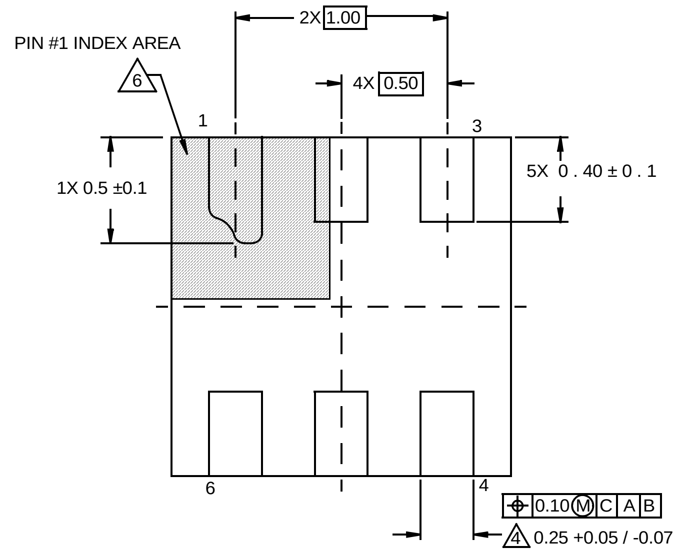
L6.1.6x1.6

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD COL PLASTIC PACKAGE (UTDFN COL)

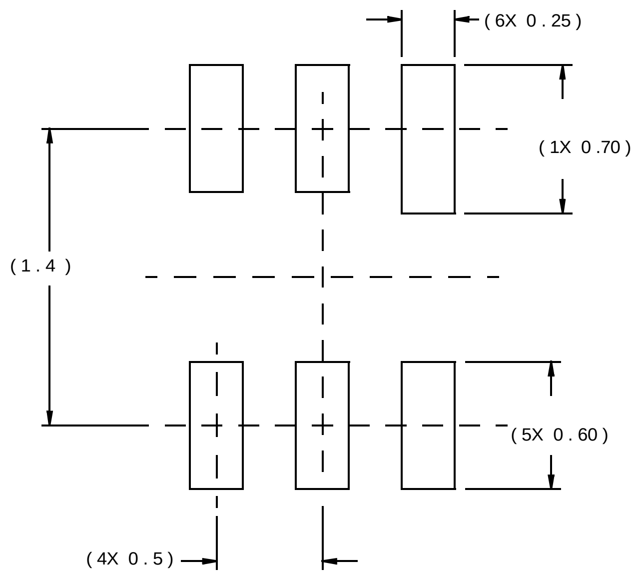
Rev 1, 11/07



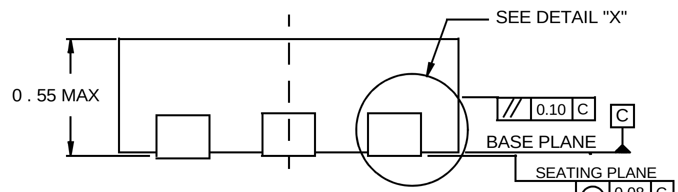
TOP VIEW



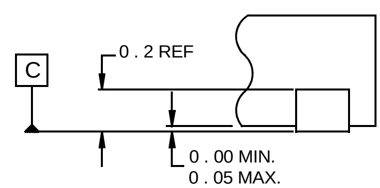
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.