2.5A Buck Controller with Integrated High-Side MOSFET

ISL78205

The ISL78205 is a synchronous buck controller with a 90mΩ high side MOSFET and low side driver integrated. The ISL78205 supports a wide input voltage range from 3V to 40V. Regarding the output current capability, the ISL78205 can typically support a continuous load of 2.5A under conditions of 5V V_{OUT}, V_{IN} range of 8V to 30V, 500kHz, +85°C ambient temperature with still air. For any specific application, the actual maximum output current depends upon the die temperature not exceeding +125°C with the power dissipated in the IC, which is related to input voltage, output voltage, duty cycle, switching frequency, ambient temperature and board layout, etc. Refer to "Output Current" on page 12 for more details.

The ISL78205 offers the most robust current protections. It uses peak current mode control with cycle-by-cycle current limiting. It is implemented with frequency foldback under current limit conditions. In addition, the hiccup overcurrent mode is also implemented to guarantee reliable operations under harsh short conditions.

The ISL78205 has comprehensive protections against various faults, including overvoltage and over-temperature protections, etc.

Features

- Ultra Wide Input Voltage Range 3V to 40V
- Less than 3µA Standby Input Current (IC Disabled)
- Temperature Range -40°C to +105°C
- Integrated 90mΩ High-Side MOSFET
- Operational Topologies
  - Synchronous Buck
  - Non-Synchronous Buck
- Programmable Frequency from 200kHz to 2.2MHz and Frequency Synchronization Capability
- ±1% Tight Voltage Regulation Accuracy
- Reliable Cycle-by-Cycle Overcurrent Protection
  - Temperature Compensated Current Sense
  - Frequency Foldback
  - Programmable OC Limit
  - Hiccup Mode Protection in Worst Case Short Condition
- 20 Ld HTSSOP Package
- Pb-Free (RoHS Compliant)

Applications

- Automotive Applications
- General Purpose Power Regulator
- 24V Bus Power
- Battery Power
- Embedded Processor and I/O Supplies

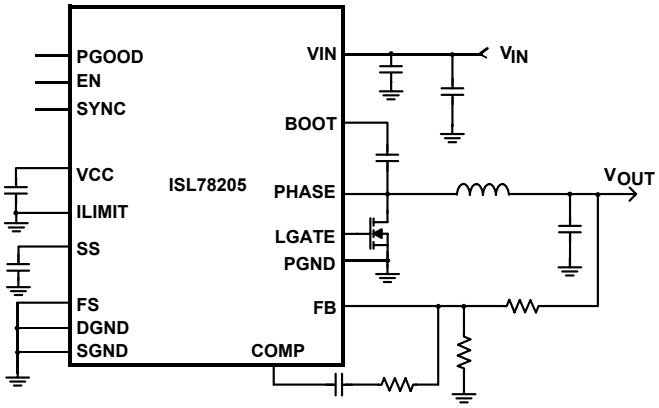


FIGURE 1. TYPICAL APPLICATION SCHEMATIC I - SYNCHRONOUS BUCK

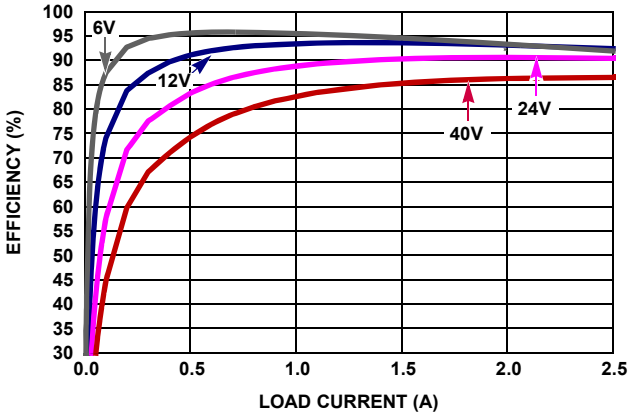
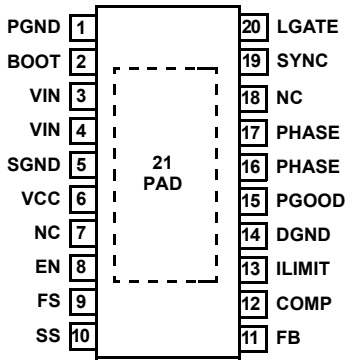


FIGURE 2. EFFICIENCY, SYNCHRONOUS BUCK, 500kHZ, V_{OUT} 5V, T_A = +25°C

Pin Configuration

ISL78205
(20 LD HTSSOP)
TOP VIEW



Functional Pin Description

PIN NAME	PIN #	DESCRIPTION
PGND	1	This pin is used as the ground connection of the power flow, including the driver.
BOOT	2	This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot charge circuitries are integrated inside of the IC. No external boot diode is needed. A 1µF ceramic capacitor is recommended to be used between the BOOT and PHASE pin.
VIN	3, 4	Connect the input rail to these pins that are connected to the drain of the integrated high-side MOSFET, as well as the source for the internal linear regulator that provides the bias of the IC. With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding Absolute Maximum Ratings.
SGND	5	This pin provides the return path for the control and monitor portions of the IC.
VCC	6	This pin is the output of the internal linear regulator that supplies the bias for the IC, including the driver. A minimum 4.7µF decoupling ceramic capacitor is recommended between VCC to ground.
EN	8	The controller is enabled when this pin is pulled HIGH. The IC is disabled when this pin is pulled LOW. Range: 0V to 5.5V.
FS	9	Tying this pin to VCC, or GND, or leaving it open will force the IC to have 500kHz switching frequency. The oscillator switching frequency can also be programmed by adjusting the resistor from this pin to GND.
SS	10	Connect a capacitor from this pin to ground. This capacitor, along with an internal 5µA current source, sets the soft-start interval of the converter. Also, this pin can be used to track a ramp on this pin.
FB	11	This pin is the inverting input of the voltage feedback error amplifier. With a properly selected resistor divider connected from V_{OUT} to FB, the output voltage can be set to any voltage between the input rail (reduced by maximum duty cycle and voltage drop) and the 0.8V reference. Loop compensation is achieved by connecting an RC network across COMP and FB. The FB pin is also monitored for overvoltage events.
COMP	12	Output of the voltage feedback error amplifier.
ILIMIT	13	Programmable current limit pin. With this pin connected to VCC pin, or to GND, or left open, the current limit threshold is set to a default of 3.6A; the current limit threshold can be programmed with a resistor from this pin to GND.
DGND	14	Digital ground pin. Connect to SGND at quiet ground copper plane.
PGOOD	15	PGOOD is an open drain output that will be pulled low immediately in the event that the output is out of regulation (OV or UV) or the EN pin is pulled low. PGOOD is equipped with a fixed delay of 1000 cycles upon output power-up (V_O > 90%).
PHASE	16, 17	These pins are the PHASE nodes that should be connected to the output inductor. These pins are connected to the source of the high side N-channel MOSFET.
SYNC	19	This pin can be used to synchronize two or more ISL78205 controllers. Multiple ISL78205s can be synchronized with their SYNC pins connected together. 180 degree phase shift is automatically generated between the master and slave ICs. The internal oscillator can also lock to an external frequency source applied to this pin with square pulse waveform (with frequency 10% higher than the IC's local frequency, and pulse width higher than 150ns). This pin should be left floating if not used.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
LGATE	20	In synchronous buck mode, this pin is used to drive the lower side MOSFET to improve efficiency. In non-synchronous buck when a diode is used as the bottom side power device, this pin should be connected to VCC before VCC start-up to disable the low side driver (LGATE).
NC	7, 18	No connection pin. Connect these pins to SGND at quiet ground copper plane.
PAD	21	Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout, it must be connected to PCB ground copper plane with area as large as possible to effectively reduce the thermal impedance.

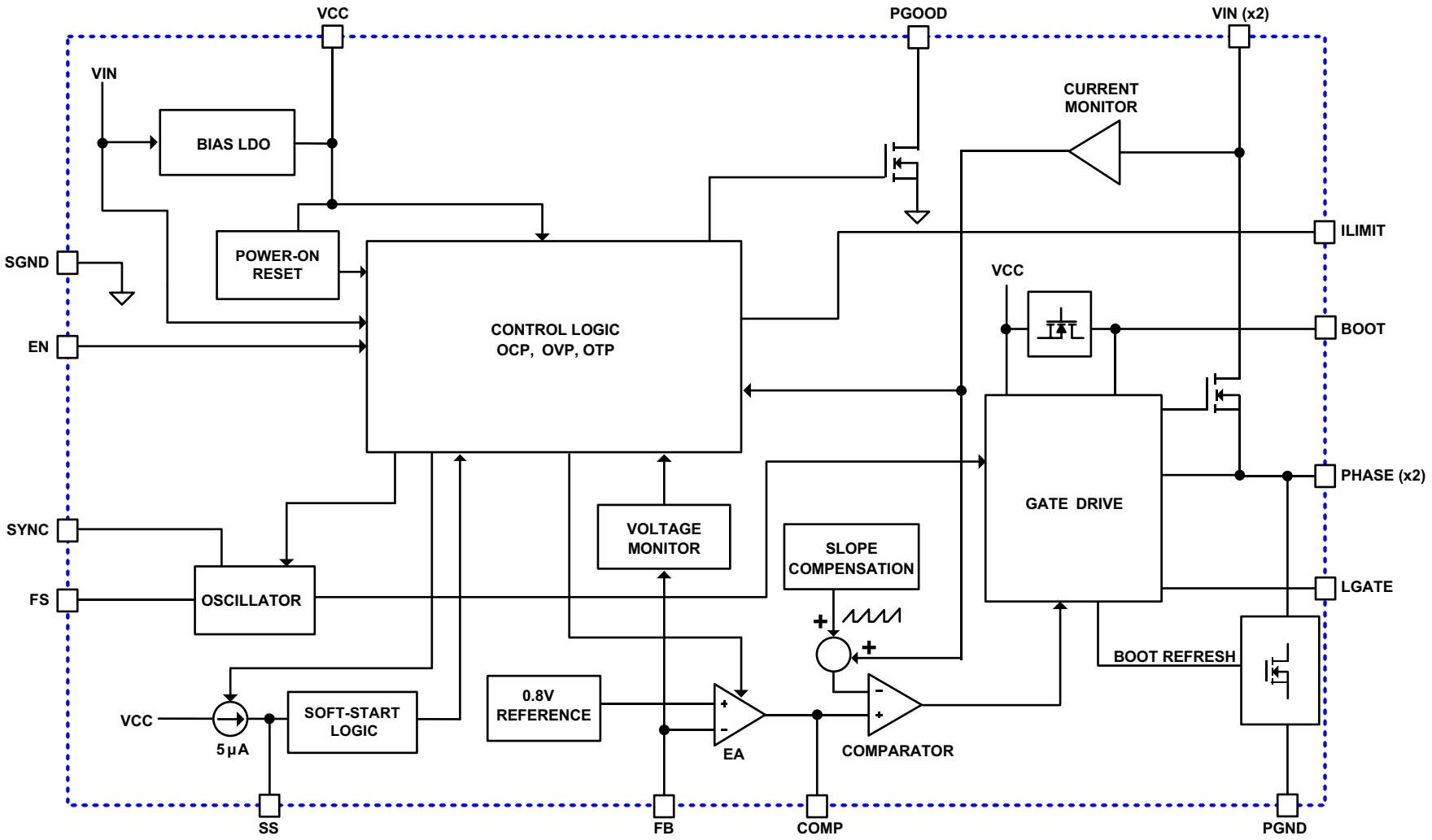
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL78205AVEZ	78205 AVEZ	-40 to +105	20 Ld HTSSOP	MDP0048

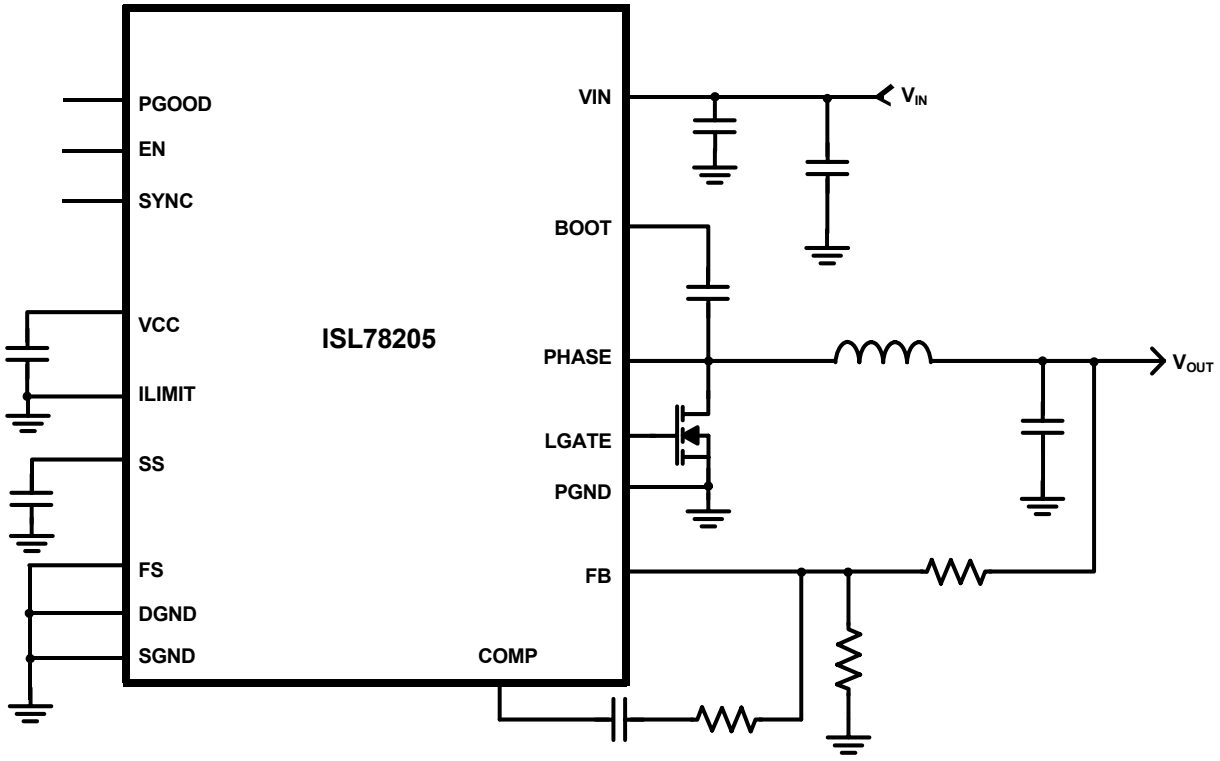
NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78205. For more information on MSL please see techbrief TB363.

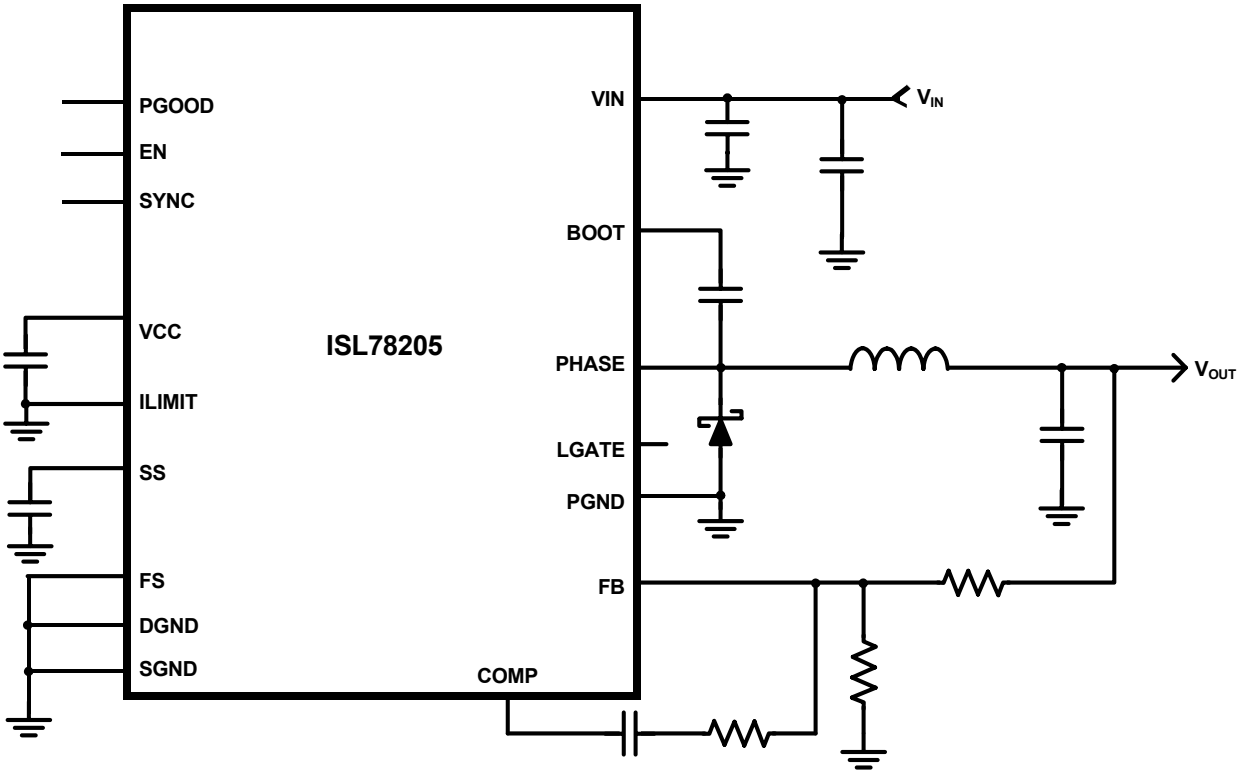
Block Diagram



Typical Application Schematic I - Synchronous Buck



Typical Application Schematic II - Non-Synchronous Buck



Absolute Maximum Ratings

VIN, PHASE . . . . . GND - 0.3V to +44V
VCC . . . . . GND - 0.3V to +6.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +50.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . +6.0V
All Other Pins . . . . . GND - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model 2000V
Machine Model 250V
Charged Device Model 1000V
Latch Up Rating (Tested per JESD78B; Class II, Level A) 100mA

Recommended Operating Conditions

Supply Voltage on VIN . . . . . 3V to 40V
Ambient Temperature Range (Automotive) . . . . . -40°C to +105°C
Junction Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld HTSSOP Package (Notes 4, 5)	32	3.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Refer to "Block Diagram" on page 4 and Typical Application Schematics on page 5. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{IN} SUPPLY						
V_{IN} Voltage Range		V_{IN}	**3.05**		**40**	V
		V_{IN} connected to VCC	**3.05**		**5.5**	V
Operating Supply Current	I_Q	No switching		1.2		mA
Standby Supply Current	I_{Q_SBY}	EN connected to GND, V_{IN} = 12V		1.8	**3**	µA
INTERNAL MAIN LINEAR REGULATOR						
MAIN LDO V_{CC} Voltage	V_{CC}	V_{IN} > 5V	**4.2**	4.5	**4.8**	V
MAIN LDO Dropout Voltage	$V_{DROPOUT\_MAIN}$	V_{IN} = 4.2V, I_{VCC} = 35mA		0.3	**0.5**	V
		V_{IN} = 3V, I_{VCC} = 25mA		0.25	**0.3**	V
V_{CC} Current Limit of MAIN LDO				60		mA
POWER-ON RESET						
Rising V_{CC} POR Threshold	V_{PORH_RISE}		**2.82**	2.9	**3.05**	V
Falling V_{CC} POR Threshold	V_{PORL_FALL}			2.6	**2.8**	V
V_{CC} POR Hysteresis	V_{PORL_HYS}			0.3		V
ENABLE						
Required Enable On Voltage	V_{ENH}		**2**			V
Required Enable Off voltage	V_{ENL}				**0.8**	V

Electrical Specifications Refer to "Block Diagram" on page 4 and Typical Application Schematics on page 5. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
OSCILLATOR						
PWM Frequency	f_{OSC}	R_T = 665kΩ	**160**	200	**240**	kHz
		R_T = 51.1kΩ	**1950**	2200	**2450**	kHz
		FS Pin connected to VCC or Floating or GND	**450**	500	**550**	kHz
MIN ON Time	t_{MIN_ON}			130	**225**	ns
MIN OFF Time	t_{MIN_OFF}			210	**325**	ns
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}			0.8		V
System Accuracy			**-1.0**		**1.0**	%
FB Pin Source Current				5		nA
SOFT-START						
Soft-Start Current	I_{SS}		**3**	5	**7**	µA
ERROR AMPLIFIER						
Unity Gain-Bandwidth		C_{LOAD} = 50pF		10		MHz
DC Gain		C_{LOAD} = 50pF		88		dB
Maximum Output Voltage				3.6		V
Minimum Output Voltage				0.5		V
Slew Rate	SR	C_{LOAD} = 50pF		5		V/µs
INTERNAL HIGH-SIDE MOSFET						
Upper MOSFET $r_{DS(ON)}$	$r_{DS(ON)\_UP}$	Note 6		90	**150**	mΩ
LOW-SIDE MOSFET GATE DRIVER						
LGate Source Resistance		100mA Source Current		3.5		Ω
LGATE Sink Resistance		100mA Sink Current		3.3		Ω
POWER GOOD MONITOR						
Overvoltage Rising Trip Point	V_{FB}/V_{REF}	Percentage of Reference Point	**104**	110	**116**	%
Overvoltage Rising Hysteresis	V_{FB}/V_{OVTRIP}	Percentage Below OV Trip Point		3		%
Undervoltage Falling Trip Point	V_{FB}/V_{REF}	Percentage of Reference Point	**84**	90	**96**	%
Undervoltage Falling Hysteresis	V_{FB}/V_{UVTRIP}	Percentage Above UV Trip Point		3		%
PGOOD Rising Delay	t_{PGOOD_DELAY}	f_{OSC} = 500kHz		2		ms
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 4.5V		10		nA
PGOOD Low Voltage	V_{PGOOD}	PGOOD LOW, I_{PGOOD} = 0.2mA		0.10		V
OVERCURRENT PROTECTION						
Default Cycle by Cycle Current Limit Threshold	I_{OC_1}	ILIMIT = GND or VCC or Floating	**3**	3.6	**4.2**	A
Hiccup Current Limit Threshold	I_{OC_2}	Hiccup, I_{OC_2}/I_{OC_1}		115		%
OVERVOLTAGE PROTECTION						
OV Latching-off Trip Point		Percentage of Reference Point LG = UG = LATCH LOW		120		%

Electrical Specifications Refer to "Block Diagram" on page 4 and Typical Application Schematics on page 5. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
OV Non-Latching-off Trip Point		Percentage of Reference Point LG = UG = LOW		110		%
OV Non-Latching-off Release Point		Percentage of Reference Point		102.5		%
OVER TEMPERATURE PROTECTION						
Over-Temperature Trip Point				155		°C
Over-Temperature Recovery Threshold				140		°C

NOTE:

6. Wire bonds not included. The wire bond resistance between VIN and PHASE pin is 32mΩ typical.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

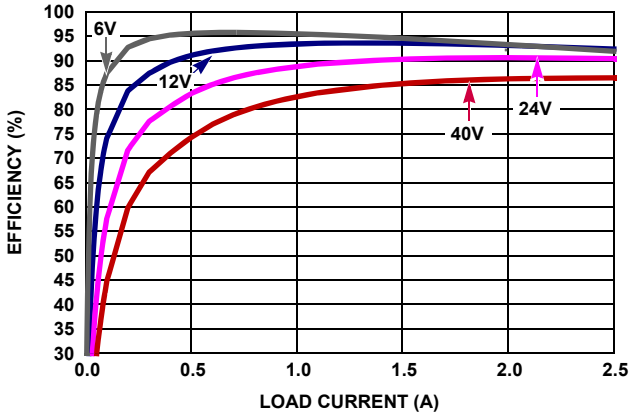


FIGURE 3. EFFICIENCY, SYNCHRONOUS BUCK, 500kHz, V_{OUT} 5V, T_A = +25°C

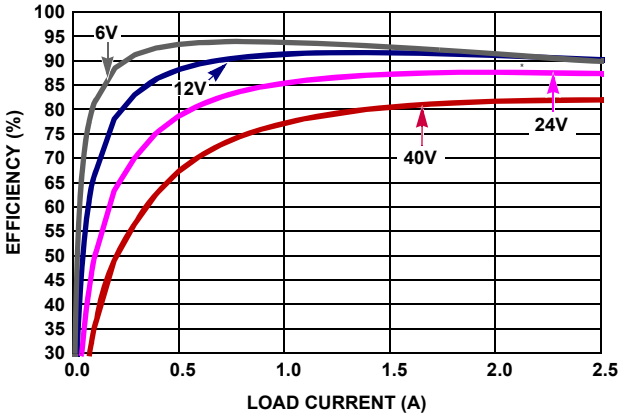


FIGURE 4. EFFICIENCY, SYNCHRONOUS BUCK, 500kHz, V_{OUT} 3.3V, T_A = +25°C

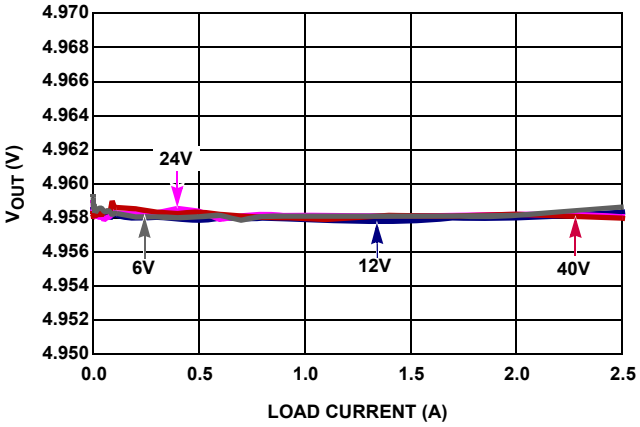


FIGURE 5. LOAD REGULATION, V_{OUT} 5V, T_A = +25°C

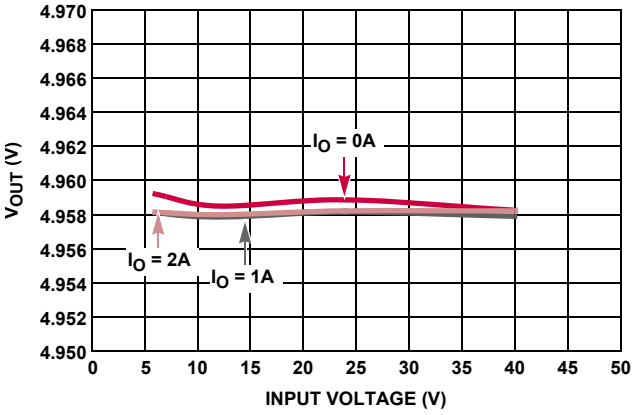


FIGURE 6. LINE REGULATION, V_{OUT} 5V, T_A = +25°C

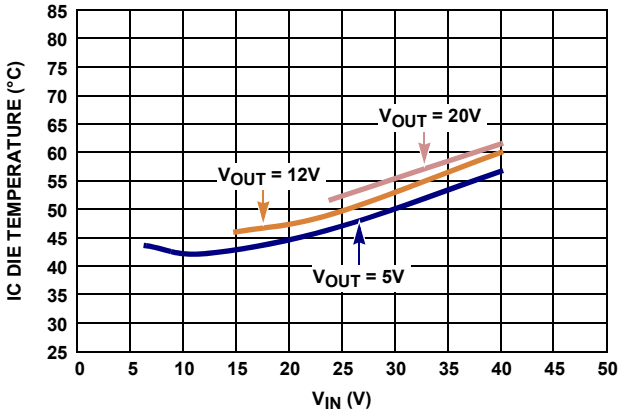


FIGURE 7. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500kHz, I_O = 2A

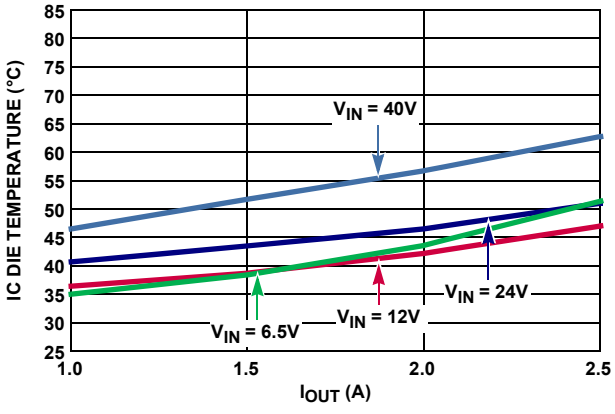


FIGURE 8. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500kHz, V_{OUT} = 5V

Typical Performance Curves (Continued)

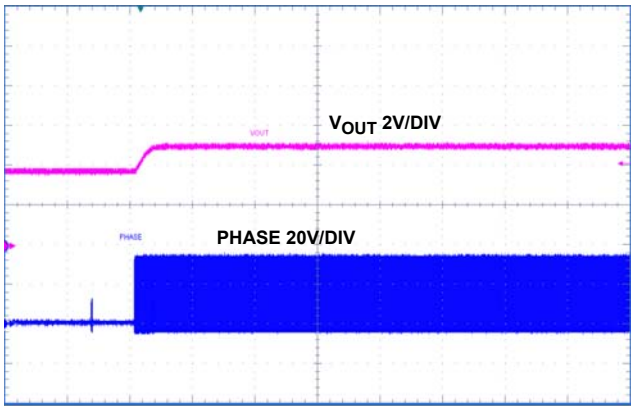


FIGURE 9. V_{IN} 36V, PRE-BIASED START-UP

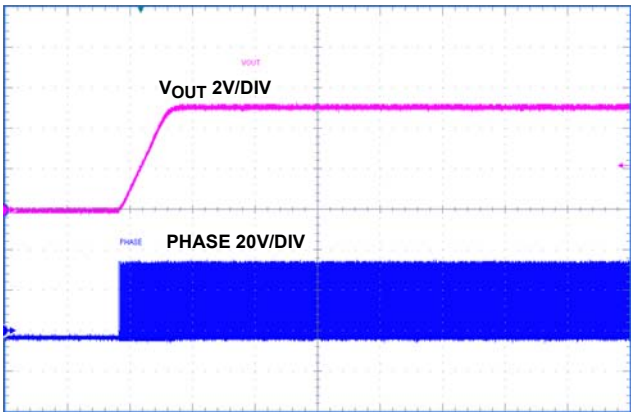


FIGURE 10. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE ON

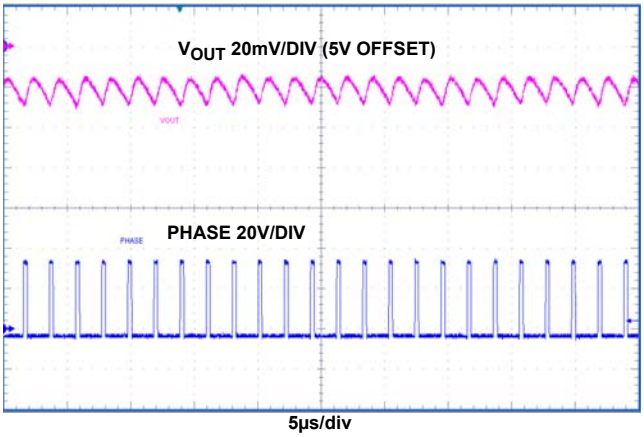


FIGURE 11. SYNCHRONOUS BUCK, V_{IN} 36V, I_O 2A

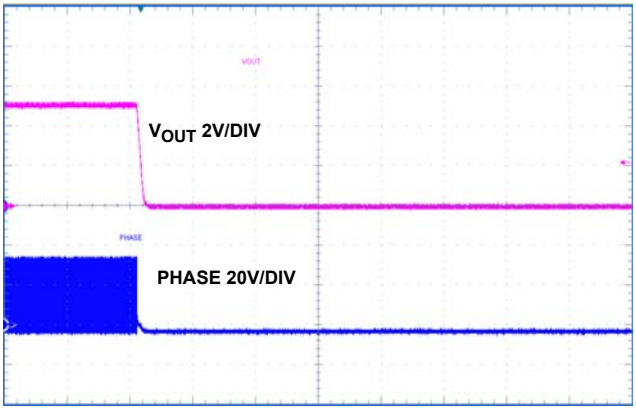


FIGURE 12. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE OFF

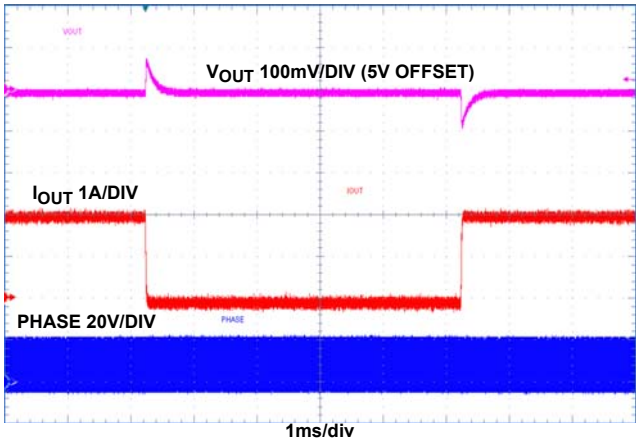


FIGURE 13. V_{IN} 24V, 0A TO 2A STEP LOAD

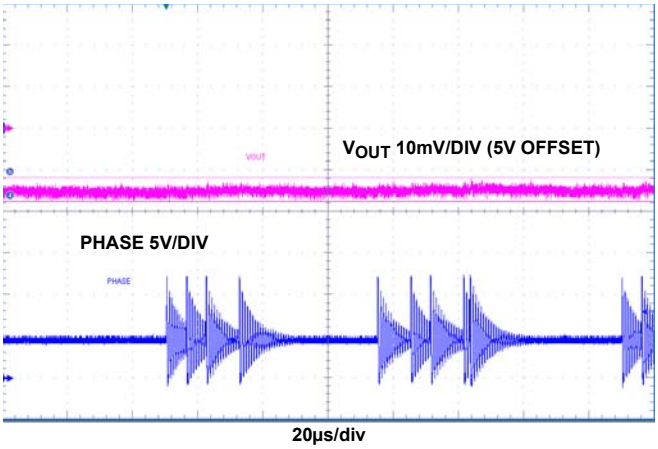


FIGURE 14. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, NO LOAD

Typical Performance Curves (Continued)

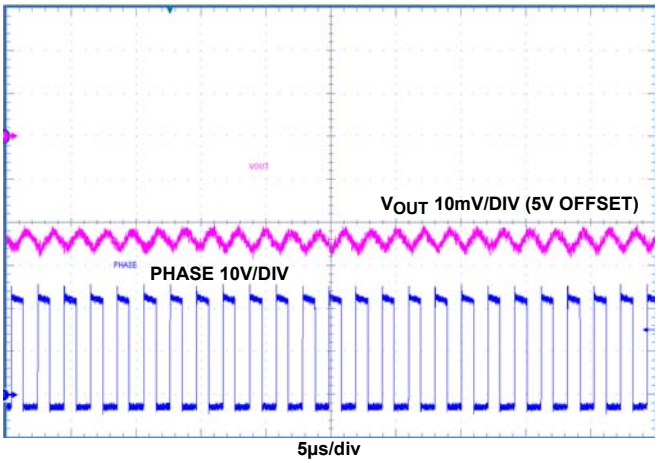


FIGURE 15. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, 2A

Functional Description

Initialization

Initially, the ISL78205 continually monitors the voltage at the EN pin. When the voltage on the EN pin exceeds its rising threshold, the internal LDO will start-up to build up VCC. After Power-On Reset (POR) circuits detect that the VCC voltage has exceeded the POR threshold, the soft-start will be initiated.

Soft-Start

The soft-start (SS) ramp is built up in the external capacitor on the SS pin that is charged by an internal 5µA current source.

$$C_{SS}[\mu F] = 6.5 \cdot t_{SS}[S] \quad \text{(EQ. 1)}$$

The SS ramp starts from 0 to voltage above 0.8V. Once SS reaches 0.8V, the bandgap reference takes over and IC gets into steady state operation.

The SS plays a vital role in the hiccup mode of operation. The IC works as cycle-by-cycle peak current limiting at over load condition. When a harsh condition occurs and the current in the upper side MOSFET reaches the second overcurrent threshold, the SS pin is pulled to ground and a dummy soft-start cycle is initiated. At dummy SS cycle, the current to charge the soft-start cap is cut down to 1/5 of its normal value. Therefore, a dummy SS cycle takes 5 times that of the regular SS cycle. During the dummy SS period, the control loop is disabled and there is no PWM output. At the end of this cycle, it will start the normal SS. The hiccup mode persists until the second overcurrent threshold is no longer reached.

The ISL78205 is capable of starting up with pre-biased output.

PWM Control

The ISL78205 employs the peak current mode PWM control for fast transient response and cycle-by-cycle current limiting. See the “Block Diagram” on page 4.

The PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on by the clock at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current sense signal and the slope compensation signal reaches the error amplifier output voltage level, the PWM comparator is triggered to shut down the PWM logic to turn off the high side MOSFET. The high side MOSFET stays off until the next clock signal starts.

The output voltage is sensed by a resistor divider from V_{OUT} to FB pin. The difference between the FB voltage and 0.8V reference is amplified and compensated to generate the error voltage signal at the COMP pin. Then the COMP pin signal is compared with the current ramp signal to shut down the PWM.

Synchronous and Non-Synchronous Buck

The ISL78205 supports both synchronous and non-synchronous buck operations. For a non-synchronous buck operation when a power diode is used as the low side power device, the LGATE driver can be disabled with LGATE connected to VCC (before IC start-up).

Input Voltage

With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding Absolute Maximum Ratings.

Output Voltage

The ISL78205 output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB. The maximum achievable voltage is (V_{IN}*D_{MAX} - V_{DROP}), where V_{DROP} is the voltage drop in the power path, including mainly the MOSFET $r_{DS(ON)}$ and inductor DCR. The maximum duty cycle D_{MAX} is decided by ($1/Fs - t_{MIN\_OFF}$).

Output Current

With the high side MOSFET integrated, the maximum current that the ISL78205 can support is decided by the package and many operating conditions, including input voltage, output voltage, duty cycle, switching frequency and temperature, etc.

First, the maximum DC output current is 5A limited by the package.

Second, from the thermal perspective, the die temperature shouldn’t be above +125°C with the power loss dissipated inside of the IC. Figures 7 and 8 show the thermal performance of this part operating at different conditions. Figure 7 shows 2A applications under +25°C still air conditions. Different V_{OUT} (5V, 12V, 20V) applications thermal data are shown over V_{IN} range at +25°C and still air. The temperature rise data in this Figure can be used to estimate the die temperature at different ambient temperatures under various operating conditions. Note that more temperature rise is expected at higher ambient temperature due to more conduction loss caused by $r_{DS(ON)}$ increase. Figure 8 shows 5V output applications' thermal performance under various output current and input voltage. It shows the temperature rise trend with load and V_{IN} changes. The part can output 2.5A under typical application conditions (V_{IN} 8~30V, V_{OUT} 5V, 500kHz, still air and +85°C ambient conditions). The output current should be derated under any conditions, causing the die temperature to exceed +125°C.

Basically, the die temperature is equal to the sum of the ambient temperature and the temperature rise resulting from the power dissipated from the IC package with a certain junction to ambient thermal impedance θ_{JA}. The power dissipated in the IC is related to the MOSFET switching loss, conduction loss and the internal LDO loss. Besides the load, these losses are also related to input voltage, output voltage, duty cycle, switching frequency and temperature. With the exposed pad at the bottom, the heat of the IC mainly goes through the bottom pad and θ_{JA} is greatly reduced. The θ_{JA} is highly related to layout and air flow conditions. In layout, multiple vias (≥15) are strongly recommended in the IC bottom pad. In addition, the bottom pad with its vias should be placed in the ground copper plane with an area as large as possible connected through multiple layers. The θ_{JA} can be reduced further with air flow. With 100CFM air flow, the θ_{JA} can be reduced by 25%.

Oscillator and Synchronization

The oscillator has a default frequency of 500kHz with the FS pin connected to VCC, or ground, or floating. The frequency can be programmed to any frequency between 200kHz and 2.2MHz with a resistor from the FS pin to GND.

$$R_{FS}[k\Omega] = \frac{145000 - 16 \cdot FS[kHz]}{FS[kHz]} \quad \text{(EQ. 2)}$$

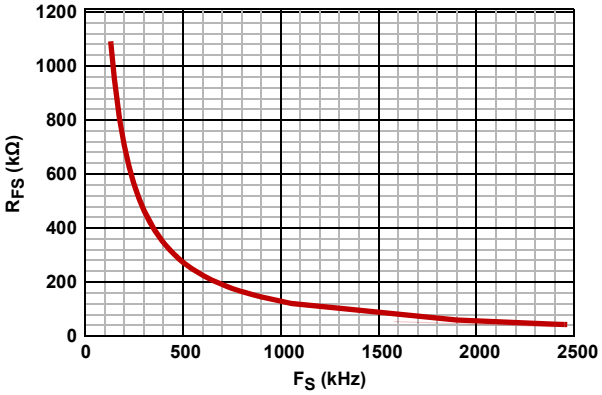


FIGURE 16. R_{FS} vs FREQUENCY

With the SYNC pins simply connected together, multiple ISL78205s can be synchronized. The slave ICs automatically have 180 degree phase shift with respect to the master IC.

With an external square pulse waveform (with frequency 10% higher than the local frequency, 10% to 90% duty cycle and pulse width higher than 150ns) on the SYNC pin, the ISL78205 will synchronize its switching frequency to the fundamental frequency of the input waveform. The internal oscillator synchronizes with the leading edge of the input signal. The rising edge of UGATE PWM is delayed by 180 degrees from the leading edge of the external clock signal.

Fault Protection

Overcurrent Protection

The overcurrent function protects against any overload conditions and output shorts at worst case, by monitoring the current flowing through the upper MOSFET.

There are 2 current limiting thresholds. The first one, I_{OC1}, is to limit the high-side MOSFET peak current cycle-by-cycle. The current limit threshold is set to a default of 3.6A with the ILIMIT pin connected to GND or VCC, or left open. The current limit threshold can also be programmed by a resistor R_{LIM} at ILIMIT pin to ground. Use Equation 3 to calculate the resistor.

$$R_{LIM} = \frac{300000}{I_{OC}[A] + 0.018} \quad \text{(EQ. 3)}$$

Note that with the lower R_{LIM}, IOC1 is higher. IOC1 reaches its maximum 5.4A with R_{LIM} at 54.9k (TYP). With R_{LIM} lower than 54.9k (TYP), the OC limit goes to its default value of 3.6A (TYP).

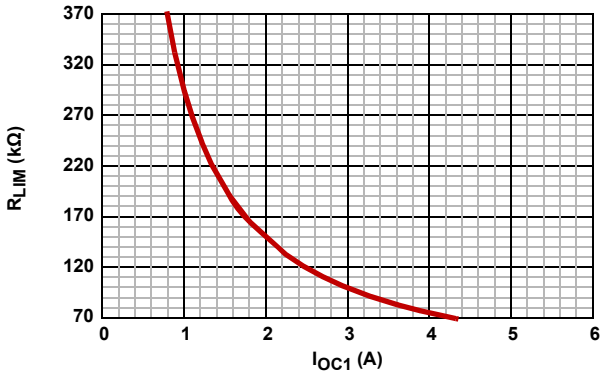


FIGURE 17. R_{LIM} vs IOC1

The second current protection threshold, I_{OC2}, is 15% higher than I_{OC1} mentioned above. Upon the instant that the high-side MOSFET current reaches I_{OC2}, the PWM shuts off after 2 cycle delay and the IC enters hiccup mode. In hiccup mode, the PWM is disabled for dummy soft-start duration equaling 5 regular soft-start periods. After this dummy soft-start cycle, the true soft-start cycle is attempted again. The I_{OC2} offers a robust and reliable protection against worst case conditions.

The frequency fold back is implemented for the ISL78205. When overcurrent limiting, the switching frequency is reduced to be proportional to the output voltage in order to keep the inductor current under limit threshold during overload conditions. The low limit of frequency under frequency foldback is 40kHz.

Overvoltage Protection

If the voltage detected on the FB pin is over 110% of reference, the high-side and low-side driver shuts down immediately and will not be allowed to turn on until the FB voltage falls down to 0.8V. When the FB voltage drops to 0.8V, the drivers are released on. If the 120% overvoltage threshold is reached, the high-side and low-side driver shut down immediately and the IC is latched off. The IC has to be reset for restart.

Thermal Protection

The ISL78205 PWM will be disabled if the junction temperature reaches +155°C. A +15°C hysteresis insures that the device will not restart until the junction temperature drops below +140°C.

Component Selection

Output Capacitors

Output capacitors are required to filter the inductor current and supply the load transient current.

All ceramic output capacitors are achievable with this IC. Also, in applications the aluminum electrolytic type capacitor provides better load transient and longer holdup time for the load. When low cost, high ESR aluminum capacitors are used at the output. Ceramic capacitors (2.2µF to 10µF) are recommended to handle the ripple current and reduce the total equivalent ESR effectively.

Input Capacitors

Depending upon the system input power rail conditions, the aluminum electrolytic type capacitor is normally needed to provide the stable input voltage and restrict the switching frequency pulse current in small areas over the input traces for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at the VIN pin of the IC and multiple capacitors, including 1µF and 0.1µF, are recommended. Place these capacitors as closely as possible to the IC.

Output Inductor

Generally the inductor should filter the current ripple to be 30~40% of the regulator's maximum average output current. The low DCR inductor should be selected for the highest efficiency. In addition, the inductor saturation current rating should be higher than the highest transient expected.

Low Side Power MOSFET

In synchronous buck applications, a power N MOSFET is needed as the synchronous low side MOSFET and it must have low $r_{DS(ON)}$, lowest Rg (Rg_typ < 1.5Ω recommended), Vgth (Vgth_min ≥ 1.2V) and Qgd. A good example is BSZ100N06LS3G.

Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB, according to Equation 4.

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_{UP}}{R_{LOW}}\right) \quad \text{(EQ. 4)}$$

In applications requiring the least input quiescent current, large resistors should be used for the divider to keep its leakage current low. 232k is a recommended for the upper resistor.

Compensation Network

With peak current mode control, type II compensation is normally used for most applications. However, in applications seeking achieve higher bandwidth, type III compensation is good to use.

Layout Suggestions

1. Place the input ceramic capacitors as close as possible to the IC VIN pin and power ground connecting to the power MOSFET or diode. Keep this loop (input ceramic capacitor, IC VIN pin and MOSFET/Diode) as tiny as possible to achieve the least voltage spikes induced by the trace parasitic inductance.

2. Place the input aluminum capacitors close to the IC VIN pin.

3. Keep the phase node copper area small, but large enough to handle the load current.

4. Place the output ceramic and aluminum capacitors also close to the power stage components.

5. Put vias (≥15) in the bottom pad of the IC. The bottom pad should be placed in the ground copper plane with area as large as possible in multiple layers to effectively reduce the thermal impedance.

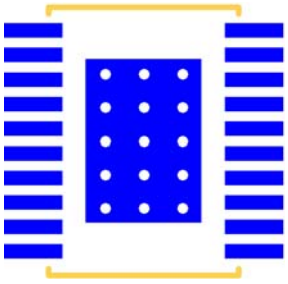


FIGURE 18. PCB VIA PATTERN

6. Place the 4.7µF ceramic decoupling capacitor at the VCC pin and as close as possible to the IC. Put multiple vias (≥3) close to the ground pad of this capacitor.

7. Keep the bootstrap capacitor close to the IC.

8. Keep the LGATE drive trace as short as possible and try to avoid using via in LGATE drive path to achieve the lowest impedance.

9. Place the positive voltage sense trace close to the load for tighter regulation.

10. Put all the peripheral control components close to the IC.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 22, 2011	FN7926.0	Initial Release

Products

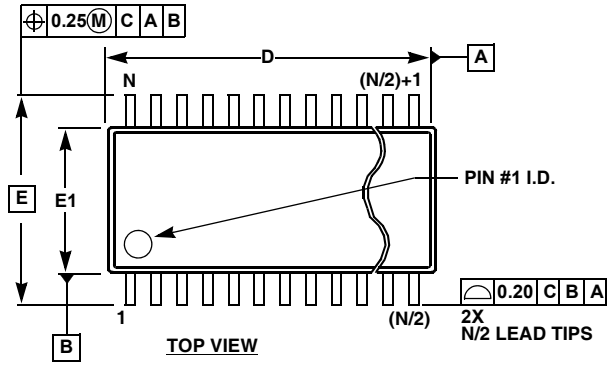
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

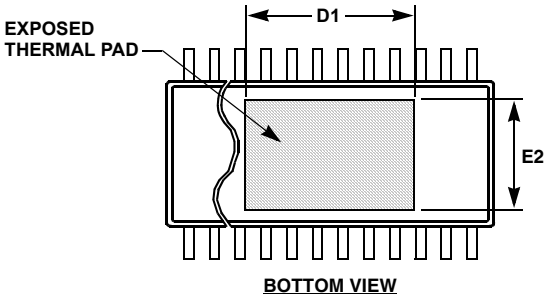
For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL78205

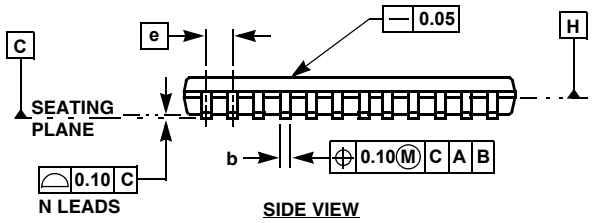
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

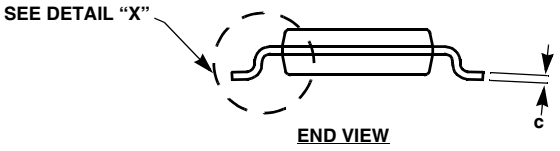
FITs are available from our website at: http://rel.intersil.com/reports/sear

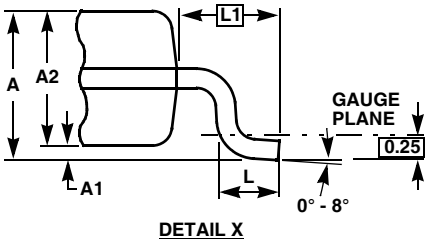
HTSSOP (Heat-Sink TSSOP) Family











MDP0048

HTSSOP (HEAT-SINK TSSOP) FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.