Radiation Hardened Ultra High Frequency NPN/PNP Transistor Arrays

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The ISL73096RH, ISL73127RH and ISL73128RH are radiation hardened bipolar transistor arrays. The ISL73096RH consists of three NPN transistors and two PNP transistors on a common substrate. The ISL73127RH consists of five NPN transistors on a common substrate. The ISL73128RH consists of five PNP transistors on a common substrate. One of our bonded wafer, dielectrically isolated fabrication processes provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment.

The high gain-bandwidth product and low noise figure of these transistors make them ideal for use in high frequency amplifier and mixer applications. Monolithic construction of the NPN and PNP transistors provides the closest electrical and thermal matching possible. Access is provided to each terminal of the transistors for maximum application flexibility.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-07218. A "hot-link" is provided on our website for downloading.

Features

- Electrically Screened to SMD # 5962-07218
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
  - Gamma Dose (γ) . . . . 3×10^5 RAD(Si)
  - SEL Immune. . . . . . . Bonded Wafer Dielectric Isolation
- NPN Gain Bandwidth Product (F_T) . . . . .8GHz (Typ)
- NPN Current Gain (h_{FE}). . . . . 130 (Typ)
- NPN Early Voltage (V_A) . . . . 50V (Typ)
- PNP Gain Bandwidth Product (F_T). . . . . 5.5GHz (Typ)
- PNP Current Gain (h_{FE}). 60 (Typ)
- PNP Early Voltage (V_A) . . . . 20V (Typ)
- Noise Figure (50Ω) at 1GHz . . . . .3.5dB (Typ)
- Collector-to-Collector Leakage. . . . . <1pA (Typ)
- Complete Isolation Between Transistors

Applications

- High Frequency Amplifiers and Mixers
  - Refer to Application Note AN9315
- High Frequency Converters
- Synchronous Detector

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F0721801V9A	ISL73096RHVX	-55 to +125
5962F0721801VXC	ISL73096RHVF	-55 to +125
5962F0721802V9A	ISL73127RHVX	-55 to +125
5962F0721802VXC	ISL73127RHVF	-55 to +125
5962F0721803V9A	ISL73128RHVX	-55 to +125
5962F0721803VXC	ISL73128RHVF	-55 to +125
ISL73096RHF/PROTO	ISL73096RHF/PROTO	-55 to +125
ISL73096RHX/SAMPLE	ISL73096RHX/SAMPLE	-55 to +125
ISL73127RHF/PROTO	ISL73127RHF/PROTO	-55 to +125
ISL73127RHX/SAMPLE	ISL73127RHX/SAMPLE	-55 to +125
ISL73128RHF/PROTO	ISL73128RHF/PROTO	-55 to +125
ISL73128RHX/SAMPLE	ISL73128RHX/SAMPLE	-55 to +125

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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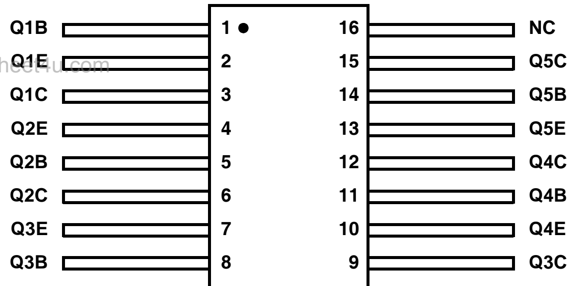
Pinouts

ISL73096RH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



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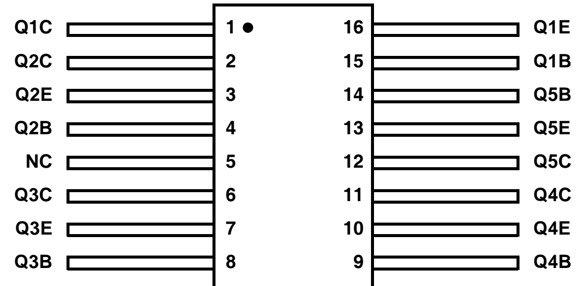
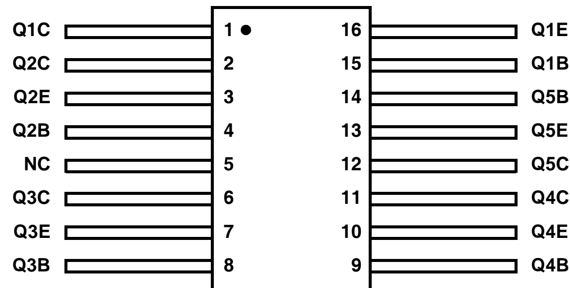
ISL73127RH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



ISL73128RH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



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Die Characteristics

DIE DIMENSIONS:

52.8 mils x 52.0 mils x 14 mils ±1 mil
1340µm x 1320µm x 355.6µm ±25.4µm

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

Top Metallization:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.5kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

Substrate:

UHF-1X Bonded Wafer, DI

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Floating

ADDITIONAL INFORMATION:

Worst Case Current Density:

$3.04 \times 10^5 A/cm^2$

Transistor Count:

5

Metallization Mask Layout

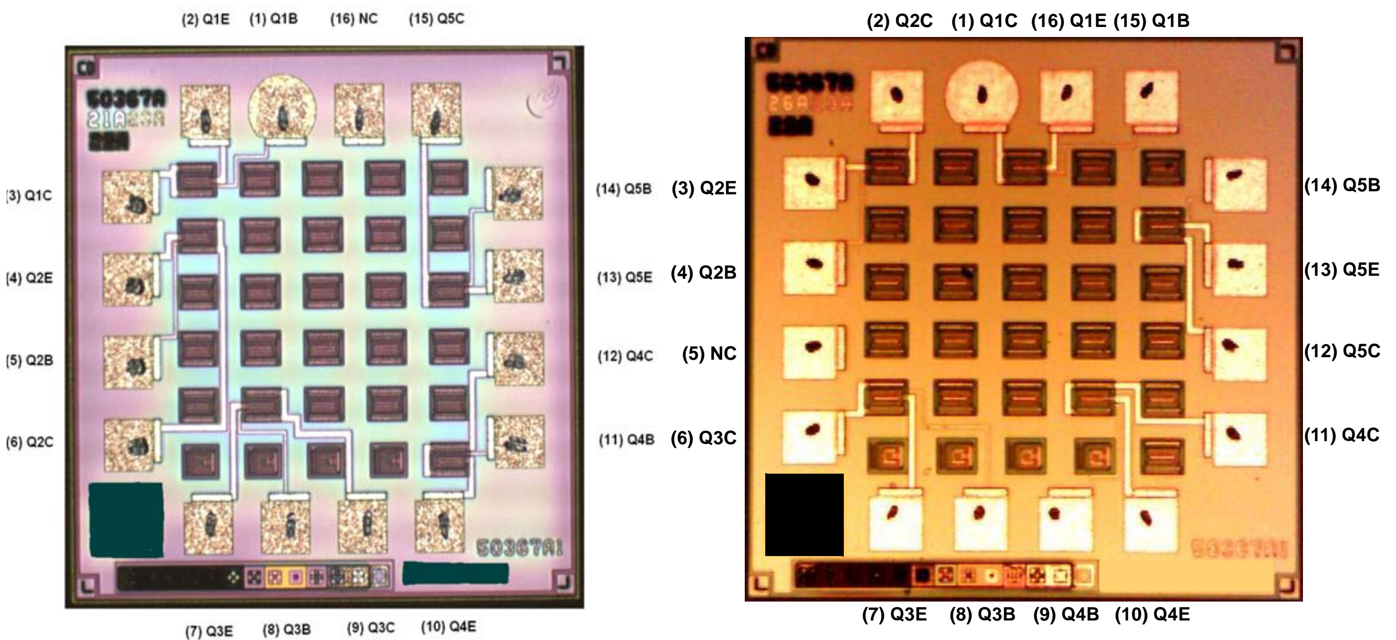

FIGURE 1. ISL73096RH, ISL73127RH

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Metallization Mask Layout (Continued)

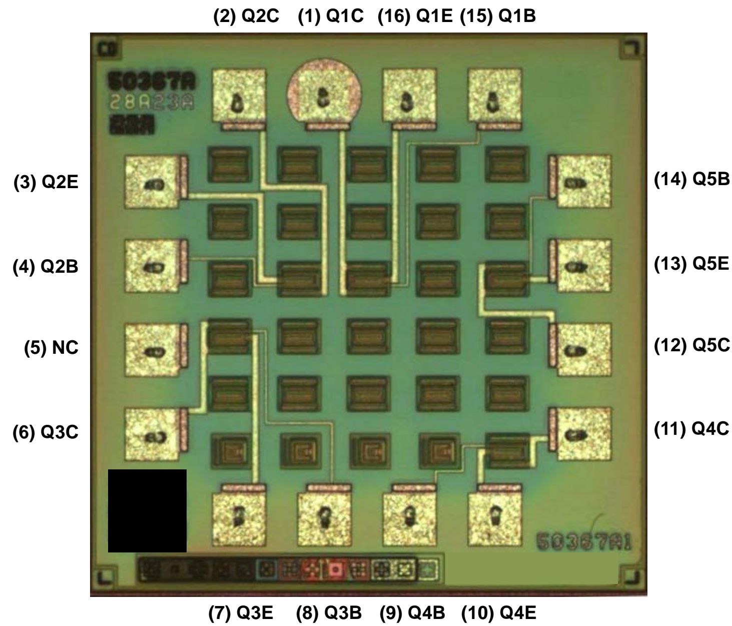

FIGURE 2. ISL73128RH

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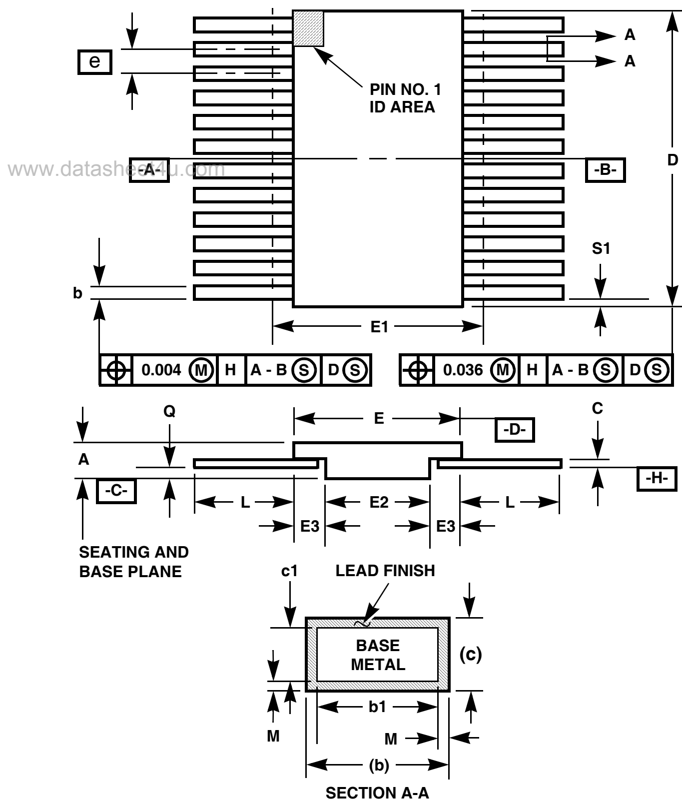
Ceramic Metal Seal Flatpack Packages (Flatpack)



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K16.A MIL-STD-1835 CDFP4-F16 (F-5A, CONFIGURATION B)
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.440	-	11.18	3
E	0.245	0.285	6.22	7.24	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	16		16		-

Rev. 1 2-20-95

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

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