PRELIMINARY | Data Sheet | November 28, 2006 | FN6392.0

Dual Synchronous Rectified MOSFET Drivers

The ISL6210 integrates two ISL6208A drivers and is optimized to drive two independent power channels in a synchronous-rectified buck converter topology. These drivers combined with an Intersil ISL62xx multiphase PWM controller forms a complete single-stage core-voltage regulator solution with high efficiency performance at high switching frequency for advanced microprocessors.

The IC is biased by a single low voltage supply (5V), minimizing driver switching losses in high MOSFET gate capacitance and high switching frequency applications. Each driver is capable of driving a 3nF load with less than 10ns rise/fall time. Bootstrapping of the upper gate driver is implemented via an internal low forward drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6210 features 4A typical sink current for the lower gate driver, enhancing the lower MOSFET gate hold-down capability during PHASE node rising edge, preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

The ISL6210 also features an input that recognizes a high-impedance state, working together with Intersil multiphase PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the schottky diode that may be utilized in a power system to protect the load from negative output voltage damage.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6210CRZ	62 10CRZ	-10 to +100	16 Ld 4x4 QFN	L16.4x4
ISL6210CRZ-T	62 10CRZ	-10 to +100	16 Ld 4x4 QFN	L16.4x4

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- 5V Quad N-Channel MOSFET Drives for Two Synchronous Rectified Bridges
- Adaptive Shoot-Through Protection
  - Active Gate Threshold Monitoring
  - Programmable Dead-Time
- 0.4Ω On-Resistance and 4A Sink Current Capability
- Supports High Switching Frequency
  - Fast Output Rise and Fall
  - Ultra Low Three-State Hold-Off Time (20ns)
- Low V_F Internal Bootstrap Diode
- Low Bias Supply Current
- Power-On Reset
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

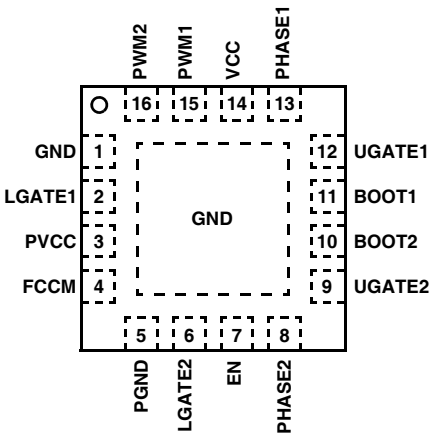
- Core Voltage Supplies for Intel® and AMD® Microprocessors
- High Frequency Low Profile High Efficiency DC/DC Converters
- High Current Low Voltage DC/DC Converters
- Synchronous Rectification for Isolated Power Supplies

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief 400 and Technical Brief 417 for Power Train Design, Layout Guidelines, and Feedback Compensation Design
- Technical Brief 447 “Guidelines for Preventing Boot-to-Phase Stress on Half-Bridge MOSFET Driver ICs”

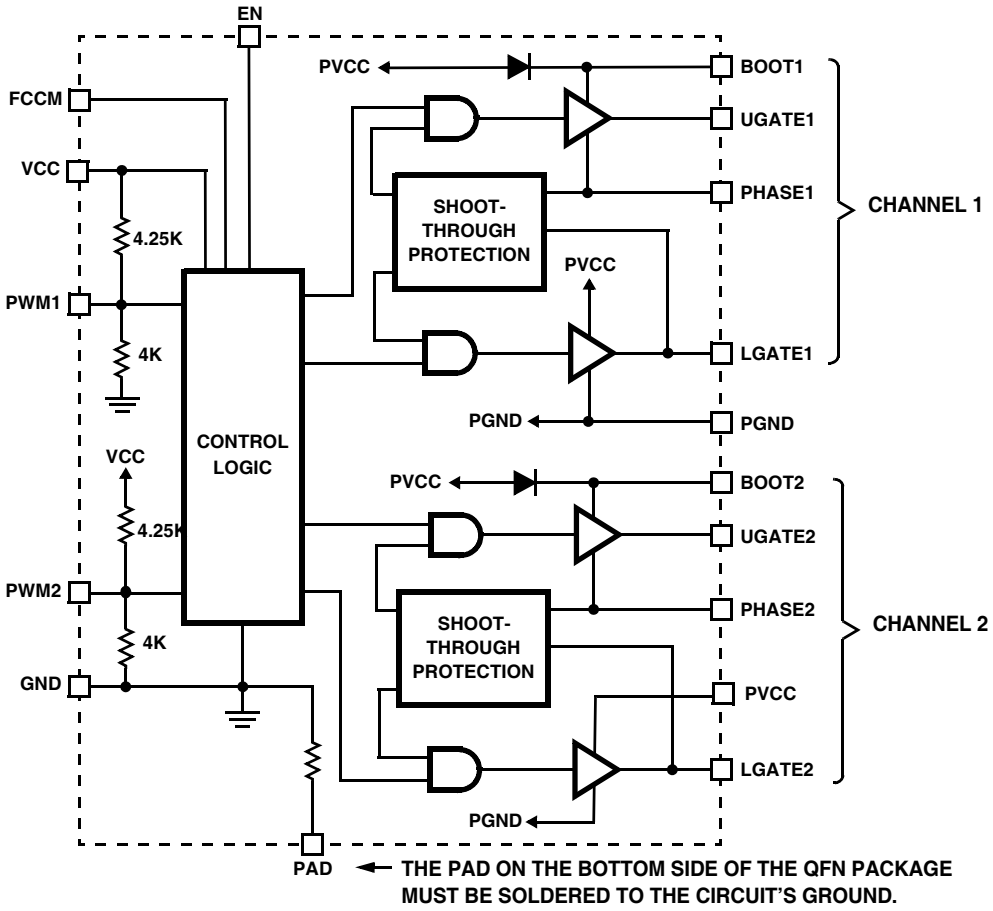
Pinout

ISL6210
(16 LD 4X4 QFN)
TOP VIEW

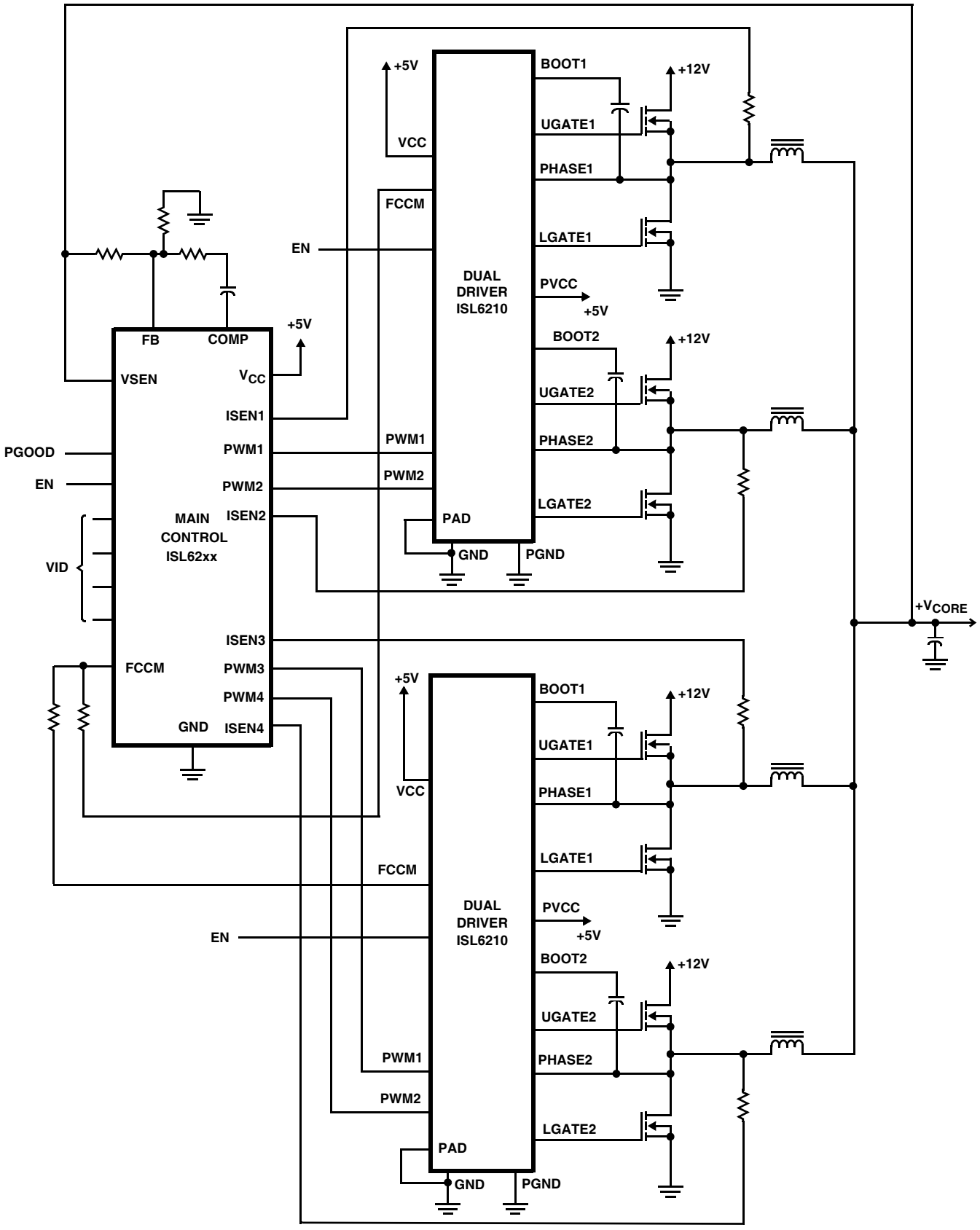


Block Diagram

ISL6210



Typical Application - Multiphase Converter Using ISL6210 Gate Drivers



Absolute Maximum Ratings

Supply Voltage (PVCC, VCC) . . . . . -0.3V to 7V
Input Voltage (V_{EN}, V_{PWM}) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . -0.3V to 33V (DC) or 36V (<200ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage . . . . . GND - 0.3V to 30V (DC)
GND -8V (<20ns Pulse Width, 10µJ)
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V
Ambient Temperature Range . . . . . -40°C to +125°C
HBM ESD Rating 2kV

Recommended Operating Conditions

Ambient Temperature Range . . . . . -10°C to +100°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

Thermal Information

Thermal Resistance (Notes 1 and 2)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
QFN Package	46	8.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
2. θ_{JC}, "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.

Electrical Specifications

These specifications apply for T_A = -10°C to +100°C, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	PWM pin floating, V_{VCC} = 5V	-	170	-	µA
POWER-ON RESET						
POR Rising			-	3.4	4.2	V
POR Falling			2.6	3.0	-	V
Hysteresis			-	400	-	mV
BOOTSTRAP DIODE						
Forward Voltage Drop	V_F	V_{VCC} = 5V, forward bias current = 2mA	0.3	0.60	0.7	V
PWM INPUT						
Sinking Impedance	R_{PWM_SNK}		8.0	10.4	15	kΩ
Source Impedance	R_{PWM_SRC}		8.3	10.6	25	kΩ
Three-State Rising Threshold		V_{VCC} = 5V	1.08	1.3	1.5	V
Three-State Falling Threshold		V_{VCC} = 5V	3.4	3.65	3.98	V
Three-State Shutdown Holdoff Time	t_{TSSHD}	t_{PDLU} or t_{PDLL} + Gate Falling Time	-	80	-	ns
Three-state to UG/LG Rising Propagation Delay	t_{PTS}		-	20	-	ns
SWITCHING TIME (See Figure 1)						
UGATE Rise Time (Note 3)	t_{RU}	V_{VCC} = 5V, 3nF Load	-	8.0	-	ns
LGATE Rise Time (Note 3)	t_{RL}	V_{VCC} = 5V, 3nF Load	-	8.0	-	ns
UGATE Fall Time (Note 3)	t_{FU}	V_{VCC} = 5V, 3nF Load	-	8.0	-	ns
LGATE Fall Time (Note 3)	t_{FL}	V_{VCC} = 5V, 3nF Load	-	4.0	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 5V, Outputs Unloaded	-	20	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 5V, Outputs Unloaded	-	27	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 5V, Outputs Unloaded; R_{SET} = 0Ω	-	26	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 5V, Outputs Unloaded; R_{SET} = 0Ω	-	26	-	ns

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, Unless Otherwise Noted **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 5V, Outputs Unloaded; R_{SET} = 80kΩ	-	41	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 5V, Outputs Unloaded; R_{SET} = 80kΩ	-	33	-	ns
Minimum LGATE On Time in DCM (Note 3)	t_{LGMIN}		-	400	-	ns
OUTPUT						
Upper Drive Source Resistance (Note 3)	R_{UG_SRC}	250mA Source Current	-	1.0	2.5	Ω
Upper Drive Source Current (Note 3)	I_{UG_SCR}	$V_{UGATE-PHASE}$ = 2.5V	-	2.00	-	A
Upper Drive Sink Resistance (Note 3)	R_{UG_SNK}	250mA Sink Current	-	1.0	2.5	Ω
Upper Drive Sink Current (Note 3)	I_{UG_SNK}	$V_{UGATE-PHASE}$ = 2.5V		2.00	-	A
Lower Drive Source Resistance (Note 3)	R_{LG_SRC}	250mA Source Current	-	1.0	2.5	Ω
Lower Drive Source Current (Note 3)	I_{LG_SCR}	V_{LGATE} = 2.5V	-	2.00	-	A
Lower Drive Sink Resistance (Note 3)	R_{LG_SNK}	250mA Sink Current	-	0.4	1.0	Ω
Lower Drive Sink Current (Note 3)	I_{LG_SNK}	V_{LGATE} = 2.5V	-	4.00	-	A

NOTE:

3. Guaranteed by Characterization. Not 100% tested in production.

Functional Pin Description

NUMBER	NAME	FUNCTION
1	GND	Bias and reference ground. All signals are referenced to this node.
2	LGATE1	Lower gate drive output of Channel 1. Connect to gate of the low-side power N-Channel MOSFET.
3	PVCC	This pin supplies power to both the lower and higher gate drives in ISL6614. Its operating range is +5V to 12V. Place a high quality low ESR ceramic capacitor from this pin to GND.
4	FCCM	Logic control input that will force continuous conduction mode (HIGH state) or allow discontinuous conduction mode (LOW state). Placing a series resistor in this input will allow the switching dead-time to be programmed.
5	PGND	It is the power ground return of both low gate drivers.
6	LGATE2	Lower gate drive output of Channel 2. Connect to gate of the low-side power N-Channel MOSFET.
7	EN	Logic control input that will enable (HIGH state) or disable (LOW state) the IC. Shutdown current is <1µA.
8	PHASE2	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET in Channel 2. This pin provides a return path for the upper gate drive.
9	UGATE2	Upper gate drive output of Channel 2. Connect to gate of high-side power N-Channel MOSFET.
10	BOOT2	Floating bootstrap supply pin for the upper gate drive of Channel 2. Connect the bootstrap capacitor between this pin and the PHASE2 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
11	BOOT1	Floating bootstrap supply pin for the upper gate drive of Channel 1. Connect the bootstrap capacitor between this pin and the PHASE1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
12	UGATE1	Upper gate drive output of Channel 1. Connect to gate of high-side power N-Channel MOSFET.
13	PHASE1	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET in Channel 1. This pin provides a return path for the upper gate drive.
14	VCC	Connect this pin to a +5V bias supply. It supplies power to internal analog circuits. Place a high quality low ESR ceramic capacitor from this pin to GND.
15	PWM1	The PWM signal is the control input for the Channel 1 driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
16	PWM2	The PWM signal is the control input for the Channel 2 driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
N/A	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Timing Diagram

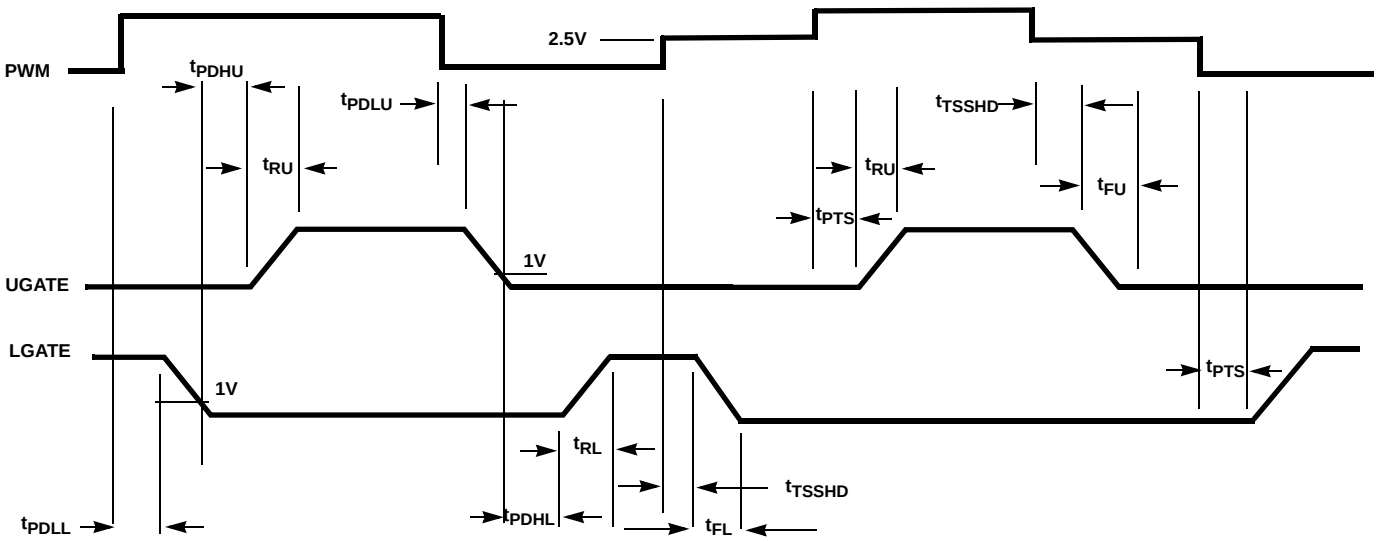


FIGURE 1. TIMING DIAGRAM

Description

Theory of Operation

Designed for speed, the ISL6210 dual MOSFET driver controls both high-side and low-side N-Channel FETs for two separate channels of a Multiphase PWM system from two independent PWM signals.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage. When LGATE has fallen below 1V, UGATE is allowed to turn ON. This prevents both the lower and upper MOSFETs from conducting simultaneously, or shoot-through.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The upper MOSFET gate-to-source voltage is monitored, and the lower gate is allowed to rise after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET.

This driver is optimized for converters with large step down compared to the upper MOSFET because the lower MOSFET conducts for a much longer time in a switching period. The lower gate driver is therefore sized much larger to meet this application requirement.

The 0.5Ω on-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected to the lower gate through the drain-to-gate capacitor of the lower MOSFET and prevent a shoot through caused by the high dv/dt of the phase node.

Diode Emulation

Diode emulation allows for higher converter efficiency under light-load situations. With diode emulation active, the ISL6210 will detect the zero current crossing of the output inductor and turn off LGATE. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal. Therefore, the ISL6210 will respond to the FCCM input immediately after it changes state.

NOTE: Intersil does not recommend Diode Emulation use with $r_{DS(ON)}$ current sensing topologies. The turn-OFF of the low side MOSFET can cause gross current measurement inaccuracies.

Three-State PWM Input

A unique feature of the ISL6210 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to turn on.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the upper MOSFET gate-to-source voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

In addition to gate threshold monitoring, a programmable delay between MOSFET switching can be accomplished by placing a resistor in series with the FCCM input. This delay allows for maximum design flexibility over MOSFET selection. The delay can be programmed from 5ns to 50ns and is obtained from the absolute value of the current flowing into the FCCM pin. If no resistor is used, the minimum 5ns delay is selected. Gate threshold monitoring is not affected by the addition or removal of the additional dead-time. Refer to Figure 2 and Figure 3 for more detail.

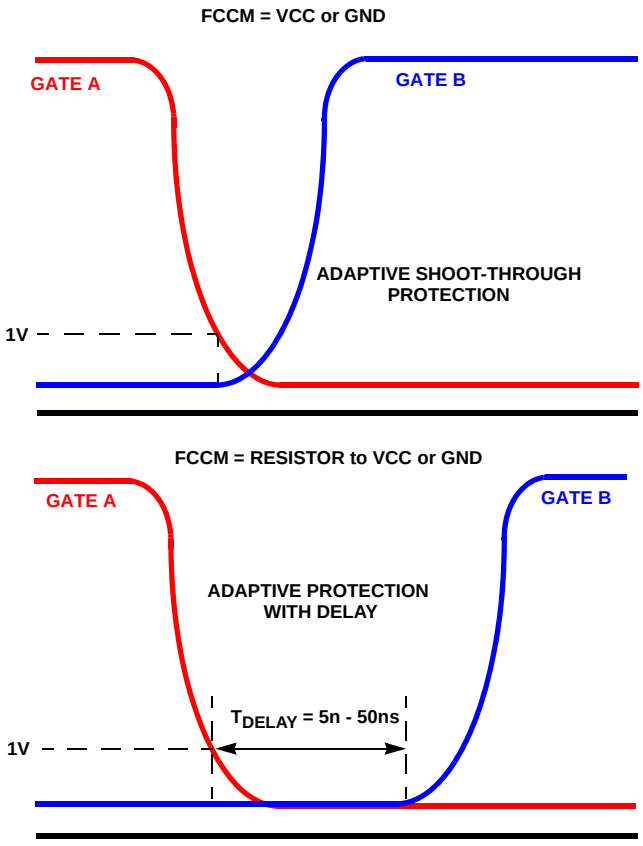


FIGURE 2. PROGRAMMABLE DEAD-TIME

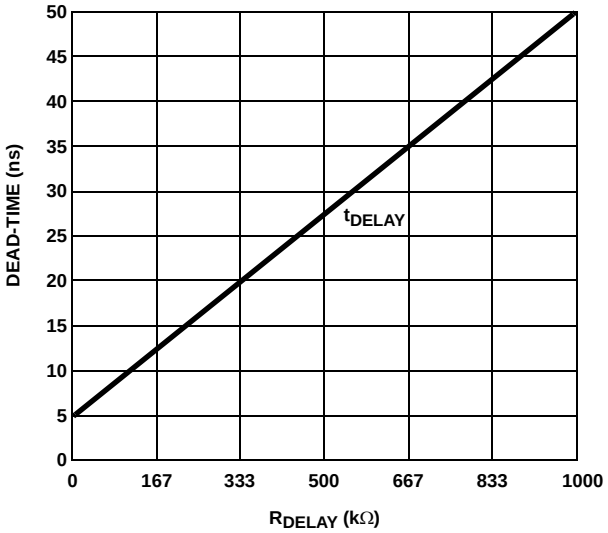


FIGURE 3. ISL6210 PROGRAMMABLE DEAD-TIME vs DELAY RESISTOR

The equation governing the dead-time seen in Figure 3 is expressed as:

$$T_{DELAY(ns)} = [0.045 \times R_{DELAY(k\Omega)}] + 5ns \quad \text{(EQ. 1)}$$

The equation can be rewritten to solve for R_{DELAY} as follows:

$$R_{DELAY}(k\Omega) = \frac{(T_{DELAY(ns)} - 5ns)}{0.045} \quad \text{(EQ. 2)}$$

Internal Bootstrap Diode

This driver features an internal bootstrap diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The following equation helps select a proper bootstrap capacitor size:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 3)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, Q_G, from the data sheet is 10nC at 4.5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 22nC at PVCC level. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.110µF is required. The next larger standard value

capacitance is 0.22µF. A good quality ceramic capacitor is recommended.

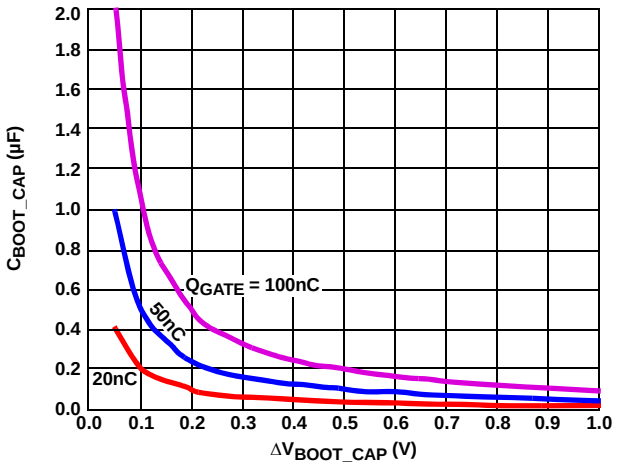


FIGURE 4. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO14 package is approximately 1W at room temperature, while the power dissipation capacity in the QFN packages, with an exposed heat escape pad, is around 2W. See Layout Considerations paragraph for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 4 and 5, respectively,

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \quad \text{(EQ. 4)}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet PVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet PVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \quad \text{(EQ. 5)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET data sheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively. The I_Q V_{CC} product is the quiescent power of the driver without capacitive load and is typically negligible.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}, should be a short to avoid interfering with the operation shoot-through protection circuitry) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 5 and 6 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \quad \text{(EQ. 6)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

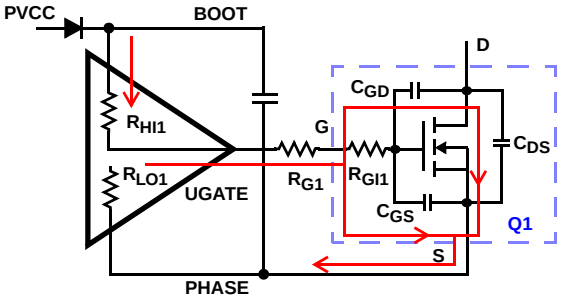


FIGURE 5. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

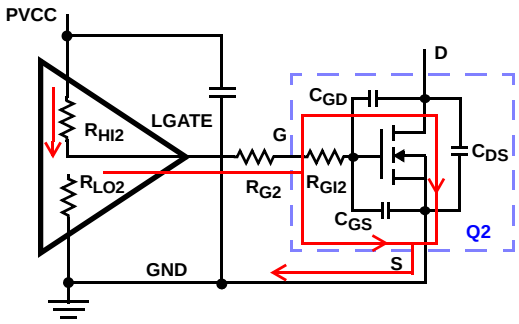


FIGURE 6. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Layout Considerations

Reducing Phase Ring

The parasitic inductances of the PCB and the power devices (both upper and lower FETs) could cause serious ringing, exceeding absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node could add charges to the bootstrap capacitor through the internal bootstrap diode, in some cases, it could cause over stress across BOOT and PHASE pins. Therefore, user should do a careful layout and select proper MOSFETs and drivers. The D^2PAK and DPAK package MOSFETs have high parasitic lead inductance, which can exacerbate this issue. FET selection plays an important role in reducing PHASE ring. If higher inductance FETs must be used, a Schottky diode is recommended across the lower MOSFET to clamp negative PHASE ring.

A good layout would help reduce the ringing on the phase and gate nodes significantly:

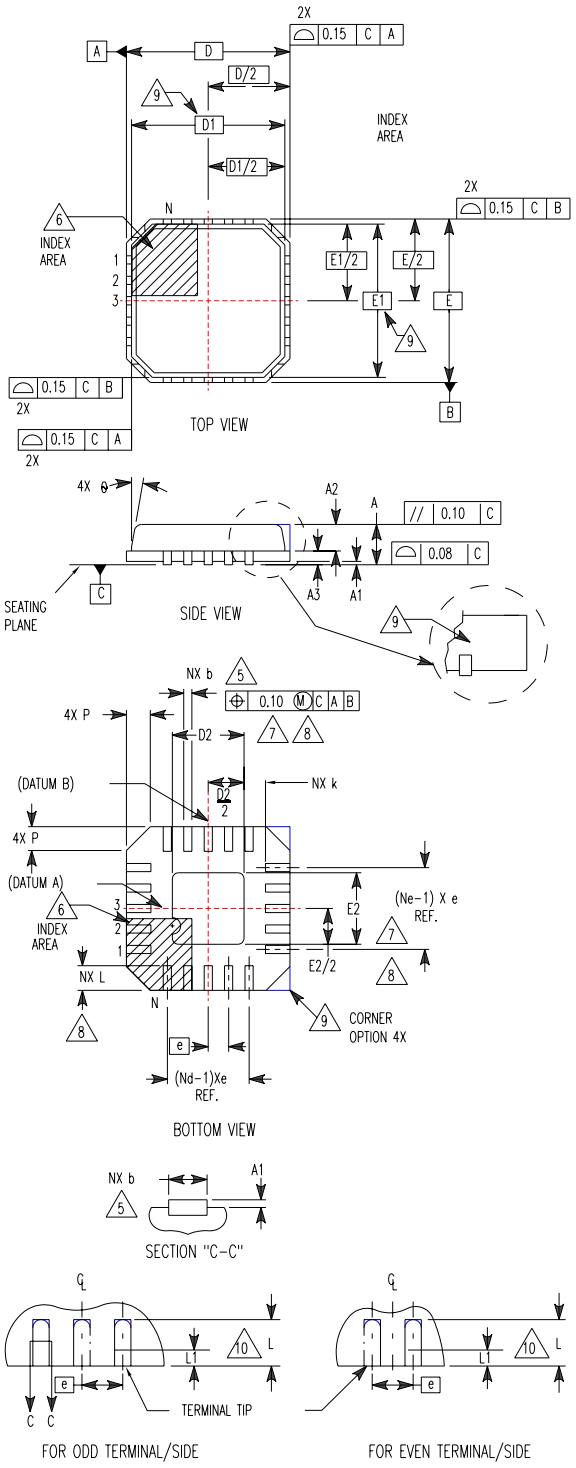
- Avoid uses via for decoupling components across BOOT and PHASE pins and in between VCC and GND pins. The decoupling loop should be short.
- All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, and avoid using via; otherwise, use two vias for interconnection when possible.
- Keep SOURCE of upper FET and DRAIN of lower FET as close as thermally possible.
- Keep connection in between SOURCE of lower FET and power ground wide and short.
- Input capacitors should be placed as close to the DRAIN of upper FET and SOURCE of lower FETs as thermally possible.

NOTE: Refer to Intersil Tech Brief TB447 for more information.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal pad of the QFN part to the power ground with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.