

Auto-Adjusting Sync Separator for HD and SD Video

The ISL59885 video sync separator is manufactured using high performance analog CMOS process. This device extracts ISL59885 sync timing information from both standard and non-standard video input in the presence of Macrovision pulses. It provides composite sync, vertical sync, SD and HDTV detection, and horizontal sync outputs. Fixed 70mV sync tip slicing provides sync edge detection when the video input level is between $0.5V_{P-P}$ and $2V_{P-P}$. Timing is adjusted automatically for various video standards. The composite sync output follows sync pulses and a vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The horizontal output gives horizontal timing with pre/post equalizing pulses. ISL59885 has an auto input frequency detect feature that sets the right timing for any input format.

The ISL59885 is available in an 8 Ld SO package and is specified for operation over the full -40°C to $+85^{\circ}\text{C}$ temperature range.

Ordering Information

| PART NUMBER | PACKAGE | TAPE & REEL | PKG. DWG. # |
|-------------------------------|----------------------|-------------|-------------|
| ISL59885IS | 8 Ld SO | - | MDP0027 |
| ISL59885IS-T7 | 8 Ld SO | 7" | MDP0027 |
| ISL59885IS-T13 | 8 Ld SO | 13" | MDP0027 |
| ISL59885ISZ (See Note) | 8 Ld SO (Pb-Free) | - | MDP0027 |
| ISL59885ISZ-T7 (See Note) | 8 Ld SO (Pb-Free) | 7" | MDP0027 |
| ISL59885ISZ-T13 (See Note) | 8 Ld SO (Pb-Free) | 13" | MDP0027 |
| ISL59885ISR5218 | 8 Ld SO | - | MDP0027 |
| ISL59885ISR5218 | 8 Ld SO (Pb-Free) | - | MDP0027 |
| ISL59885IS-T7R5218 | 8 Ld SO | 7" | MDP0027 |
| ISL59885ISZ-T7R5218 | 8 Ld SO (Pb-Free) | 7" | MDP0027 |
| ISL59885IS-T13R5218 | 8 Ld SO | 13" | MDP0027 |
| ISL59885ISZ-T13R5218 | 8 Ld SO (Pb-Free) | 13" | MDP0027 |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- NTSC, PAL, SECAM, HDTV, non-standard video sync separation
- Fixed 70mV slicing of video input levels from $0.5V_{P-P}$ to $2V_{P-P}$
- Single 3V to 5V supply
- Composite sync output
- Vertical output
- Horizontal output
- HDTV detection
- 81% to 90% Hsync blanking window (R5218)
- Macrovision compatible
- Available in 8 Ld SO package
- Pb-Free plus anneal available (RoHS compliant)

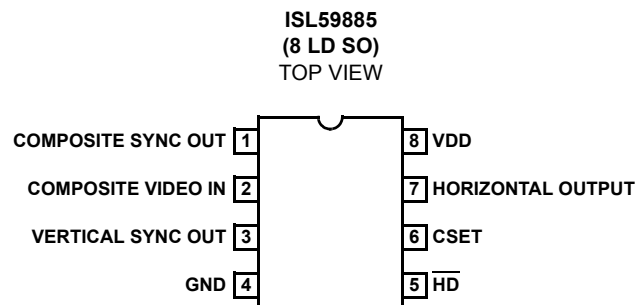
Applications

- High definition video equipment

Demo Board

- A dedicated demo board is available

Pinout



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

| | | | |
|-------------------------------------|--------------------------|--------------------------------|-----------------|
| V_{CC} Supply | .7V | Operating Junction Temperature | +150°C |
| Pin Voltages | -0.5V to $V_{CC} + 0.5V$ | Storage Temperature | -65°C to +150°C |
| Operating Ambient Temperature Range | -40°C to +85°C | Power Dissipation | .400mW |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications $V_{DD} = 3.3V$, $T_A = 25^\circ\text{C}$, $C_{SET} = 56\text{nF}$, unless otherwise specified.

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------------------------|-------------------------------------|------|------|------|---------------|
| I_{DD} , Quiescent | $V_{DD} = 3.3V$ | 1.5 | 2.2 | 4 | mA |
| Clamp Voltage | Pin 2, $I_{LOAD} = -100\mu\text{A}$ | 1.35 | 1.5 | 1.65 | V |
| Clamp Discharge Current | Pin 2 = 2V | 6 | 15 | 30 | μA |
| Clamp Charge Current | Pin 2 = 1V | -9 | -7.2 | -5.2 | mA |
| V_{OL} Output Low Voltage | $I_{OL} = 1.6\text{mA}$ | | 0.24 | 0.5 | V |
| V_{OH} Output High Voltage | $I_{OH} = -40\mu\text{A}$ | 3 | 3.2 | | V |
| | $I_{OH} = -1.6\text{mA}$ | 2.5 | 3.0 | | V |

Dynamic Characteristics

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|---------------|
| Comp Sync Prop Delay, t_{CS} | See Figure 9 | | 35 | 75 | ns |
| Horizontal Sync Delay, t_{HS} | See Figure 9 | | 40 | 80 | ns |
| Horizontal Sync Width, t_{HS-PW} | See Figure 9 | 3.8 | 5.2 | 6.2 | μs |
| Vertical Sync Width, t_{VS} | Normal or default trigger, 50% - 50%, see Figure 7 | 230 | 280 | 350 | μs |
| Vertical Sync Default Delay, t_{VSD} | See Figure 10 | 28 | 50 | 68 | μs |
| Hsync Blanking Window | ISL59885IS-R5218 only | 81 | 85 | 90 | % |
| Input Dynamic Range | Video input amplitude to maintain slice level spec, $V_{DD} = 3.3V$ | 0.5 | | 2 | V_{P-P} |
| Slice Level | V_{SLICE} above V_{CLAMP} | 50 | 70 | 90 | mV |
| \overline{HD} Pin Level | 720p, 1080i, 1080p | | 0 | | V |

Pin Descriptions

| PIN NUMBER | PIN NAME | PIN FUNCTION |
|------------|--------------------|---|
| 1 | COMPOSITE SYNC OUT | Composite sync pulse output; sync pulses start on a falling edge and end on a rising edge |
| 2 | COMPOSITE VIDEO IN | AC coupled composite video input; sync tip must be at the lowest potential (positive picture phase) |
| 3 | VERTICAL SYNC OUT | Vertical sync pulse output; the falling edge of vert sync is the start of the vertical period |
| 4 | GND | Supply ground |
| 5 | \overline{HD} | Low when input horizontal frequency is greater than 20kHz |
| 6 | CSET | (An external capacitor to ground); bypass pin for internal bias generator. |
| 7 | HORIZONTAL OUTPUT | Horizontal output; falling edge active |
| 8 | VDD | Positive supply |

Typical Performance Curves

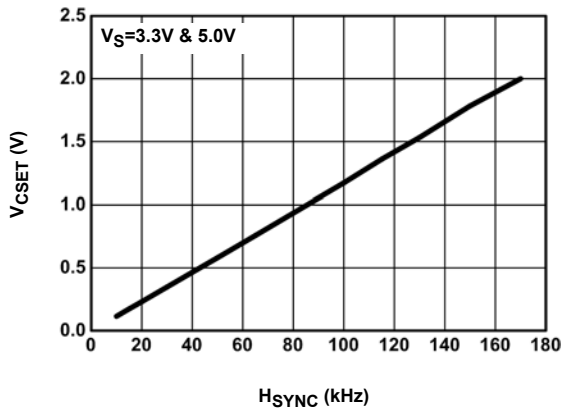


FIGURE 1. H_{SYNC} vs V_{CSET} ($R_{SET} = OPEN$)

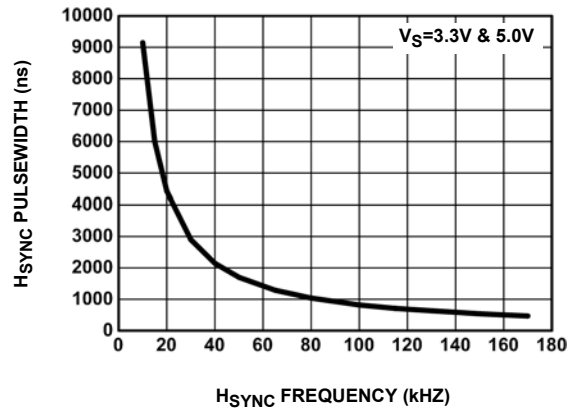


FIGURE 2. H_{SYNC} PULSEWIDTH vs H_{SYNC} FREQUENCY ($R_{SET} = OPEN$)

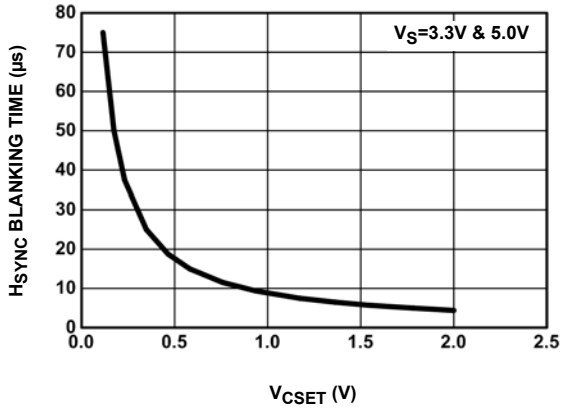


FIGURE 3. H_{SYNC} vs V_{CSET} ($R_{SET} = OPEN$)

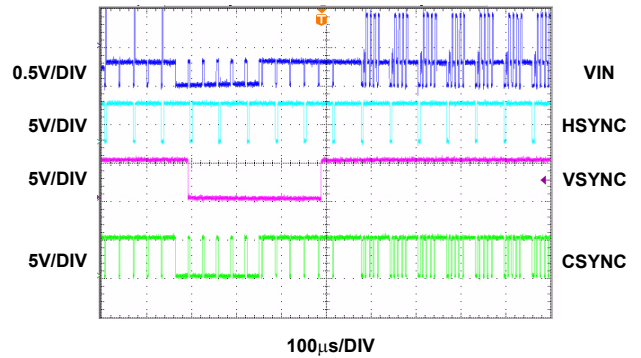


FIGURE 4. MACROVISION COMPATIBILITY (NTSC)

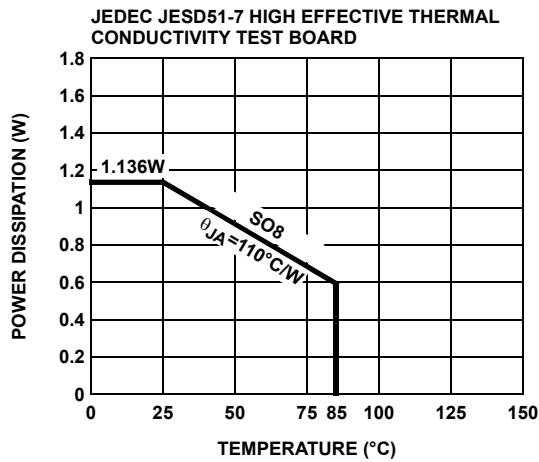


FIGURE 5. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

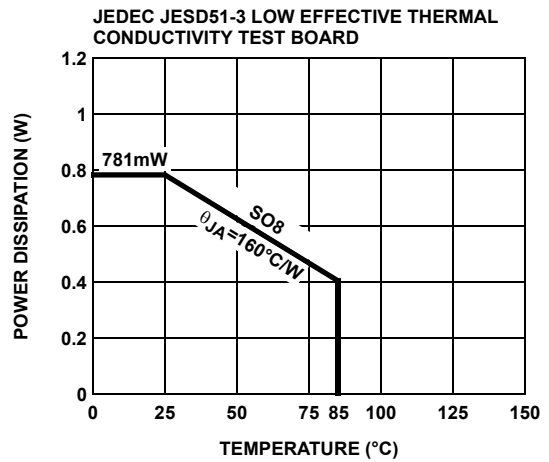
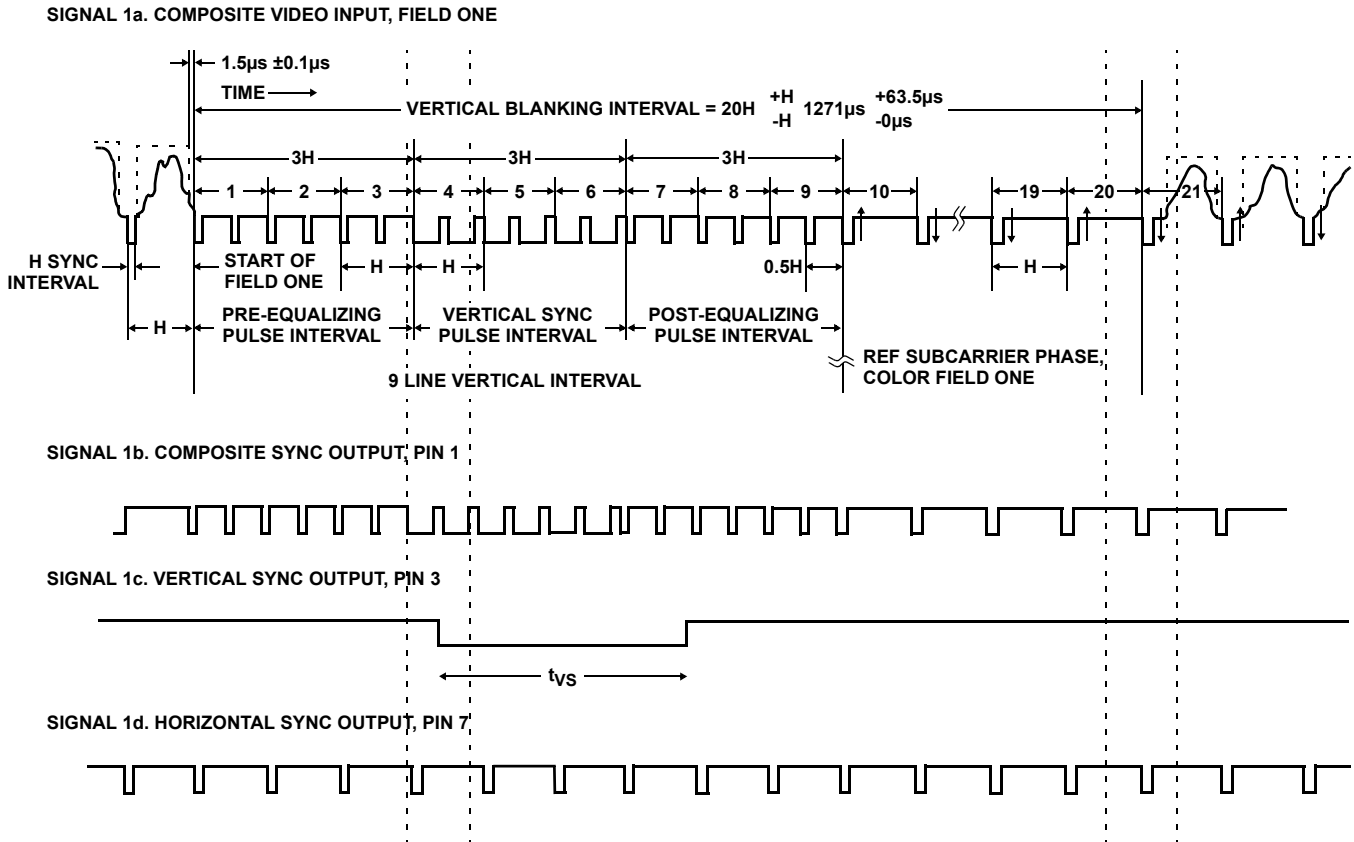


FIGURE 6. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE



NOTES:

- b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
- c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.
- d. Horizontal sync output produces the true "H" pulses of nominal width of $5\mu\text{s}$. It has the same delay as the composite sync.

FIGURE 7. TIMING DIAGRAM

CONDITIONS: $V_{CCA1} = V_{CCA2} = V_{CCD} = +5V$, $T_A = 25^\circ C$, NO FILTER (REGISTER 2 BIT 4=0)

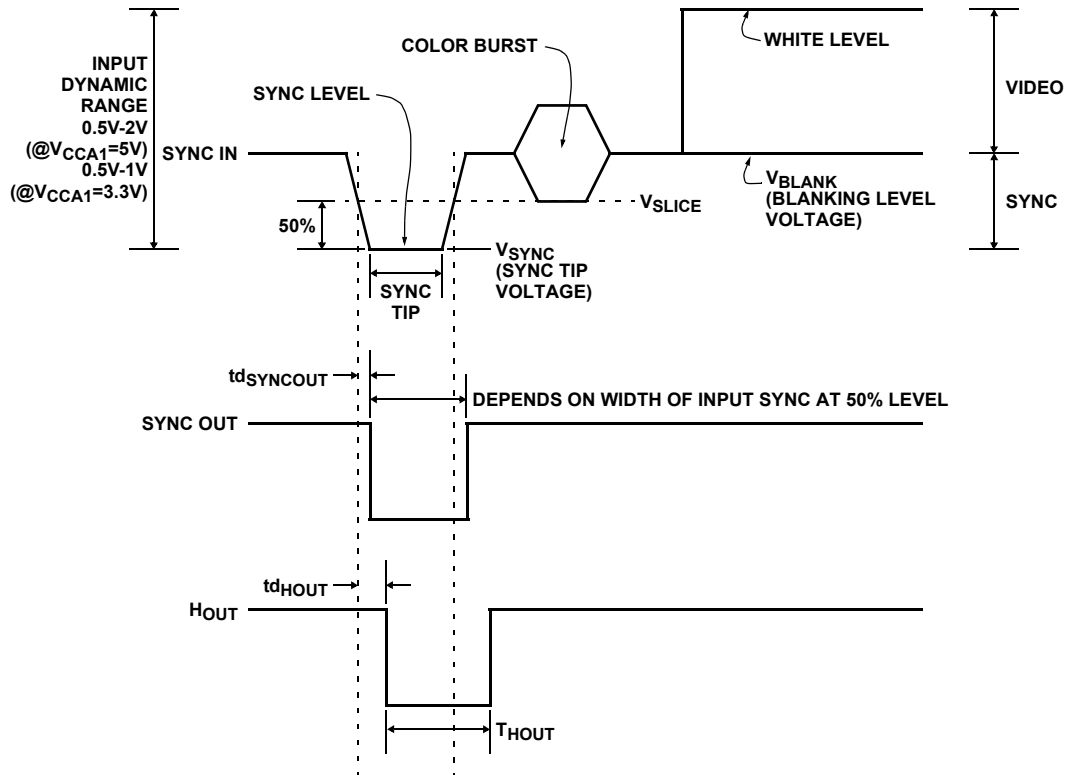


FIGURE 8. HORIZONTAL INTERVAL 525/625 LINE COMPOSITE

| PARAMETER | DESCRIPTION | CONDITIONS | TYP (Note 1) | UNIT |
|---------------|---------------------------------|--------------|--------------|------|
| td_{SYNCOU} | SYNCOU Timing Relative to Input | See Figure 8 | 65 | ns |
| td_{HOUT} | HOUT Timing Relative to Input | See Figure 8 | 470 | ns |
| T_{HOUT} | Horizontal Output Width | See Figure 8 | 5.2 | us |

NOTE:

1. Delay variation is less than 2.5ns over temperature range.

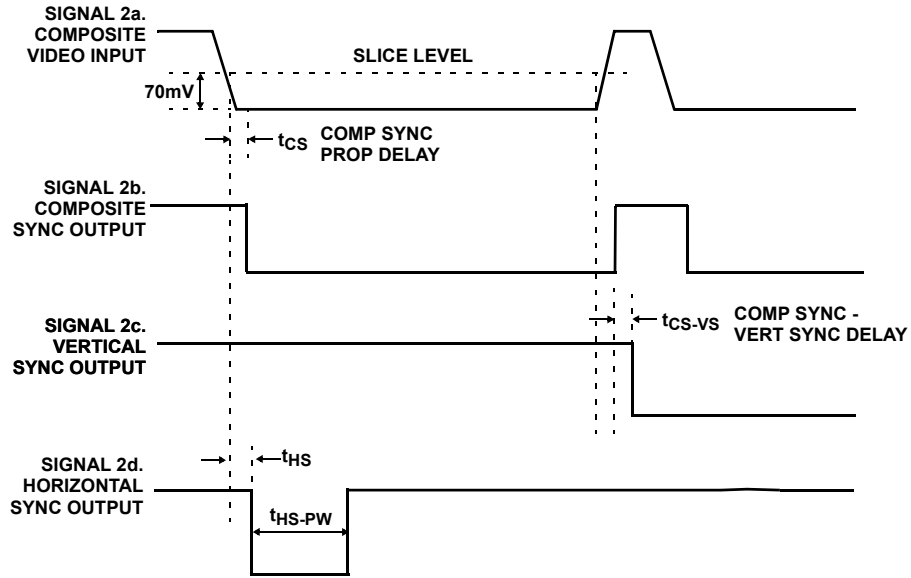


FIGURE 9. STANDARD VERTICAL TIMING

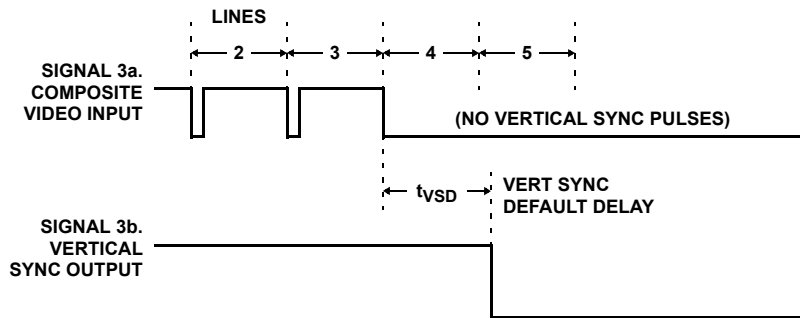
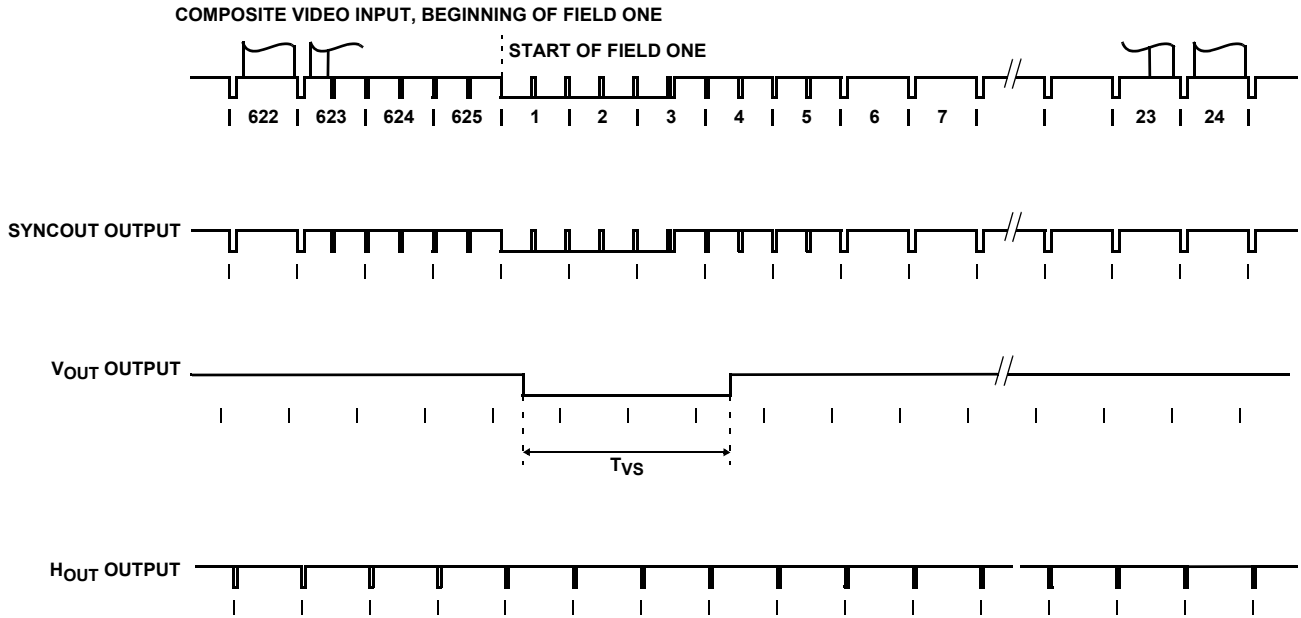


FIGURE 10. NON-STANDARD VERTICAL TIMING



NOTES:

- b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
- c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

FIGURE 11. EXAMPLE OF VERTICAL INTERVAL (625)

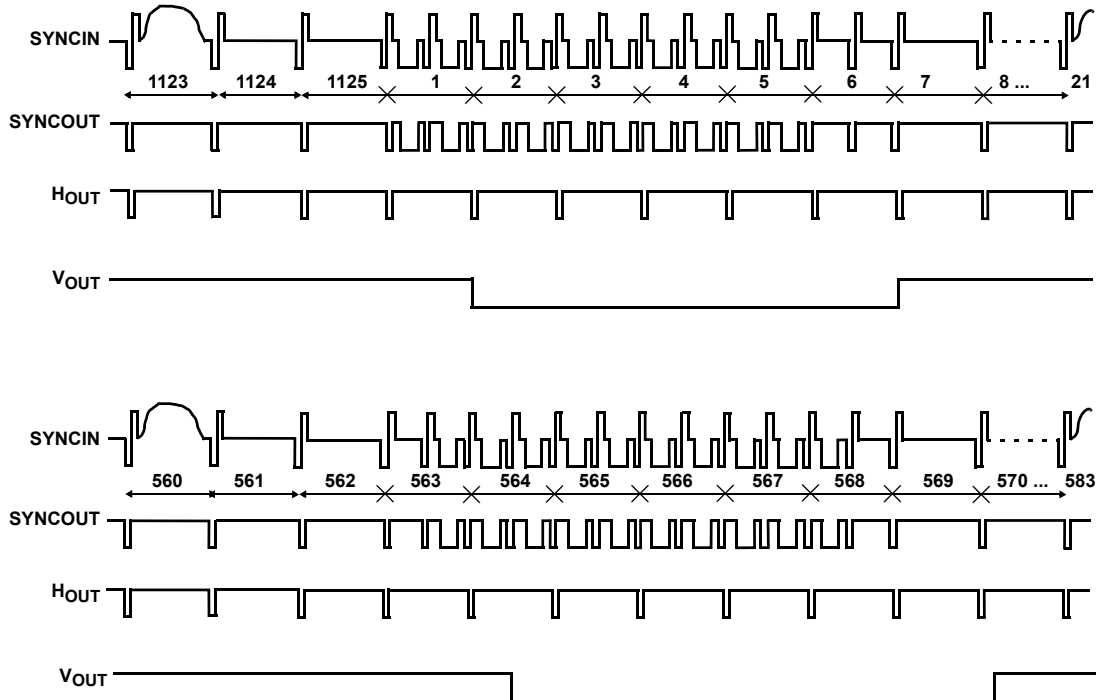


FIGURE 12. EXAMPLE OF HDTV 1080I/30 LINE COMPOSITE VIDEO: INTERLACED

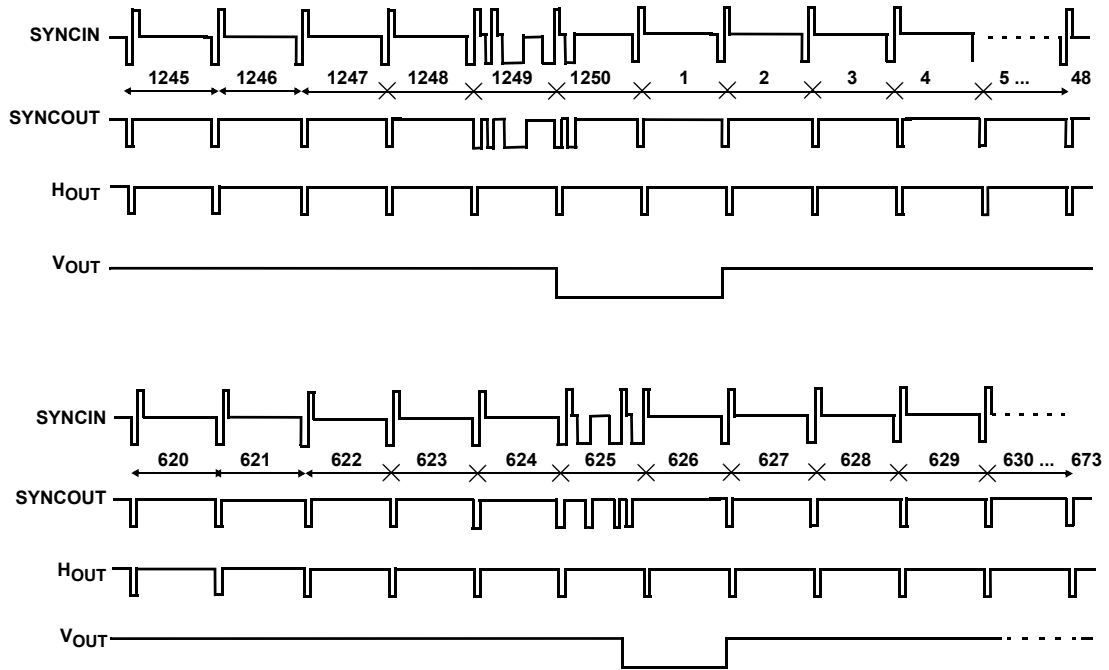


FIGURE 13. HDTV 1080I/25 LINE COMPOSITE VIDEO: INTERLACED (1250 LINES)

CONDITIONS: $V_{CCA1} = V_{CCA2} = V_{CCD} = +3.3V/+5V$, $T_A = 25^{\circ}C$, NO FILTER (REGISTER 2 BIT 4=0)

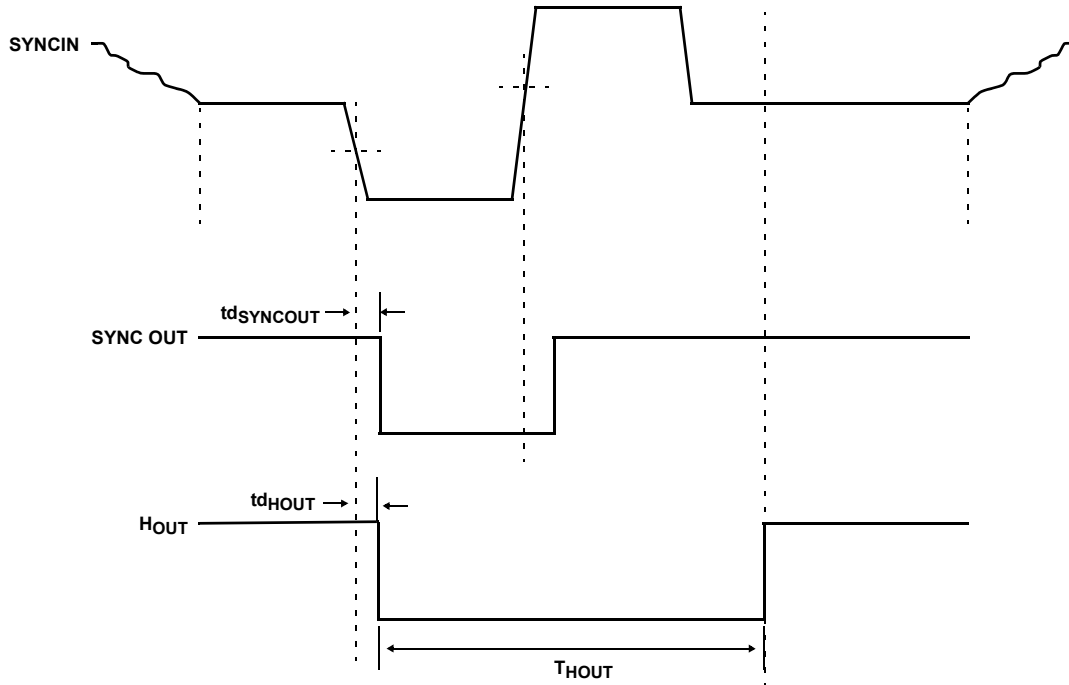


FIGURE 14. HORIZONTAL INTERVAL (HDTV) (720p)

H Timing for HDTV, No Filter (using 720p input signal)

| PARAMETER | DESCRIPTION | CONDITIONS | TYP @ 3.3V (Note 1) | TYP @ 5V (Note 1) | UNIT |
|---------------|---------------------------------|---------------|---------------------|-------------------|------|
| $t_{dSYNCOU}$ | SYNCOU Timing Relative to Input | See Figure 14 | 56 | 50 | ns |
| t_{dHOUT} | HOUT Timing Relative to Input | See Figure 14 | 48 | 36 | ns |
| T_{HOUT} | Horizontal Output Width | See Figure 14 | 1.90 | 1.90 | us |

NOTE:

1. Delay variation is less than 2.5ns over temperature range.

CONDITIONS: $V_{CCA1} = V_{CCA2} = V_{CCD} = +3.3V/+5V$, $T_A = 25^{\circ}C$, FILTER (REGISTER 2 BIT 4=1)

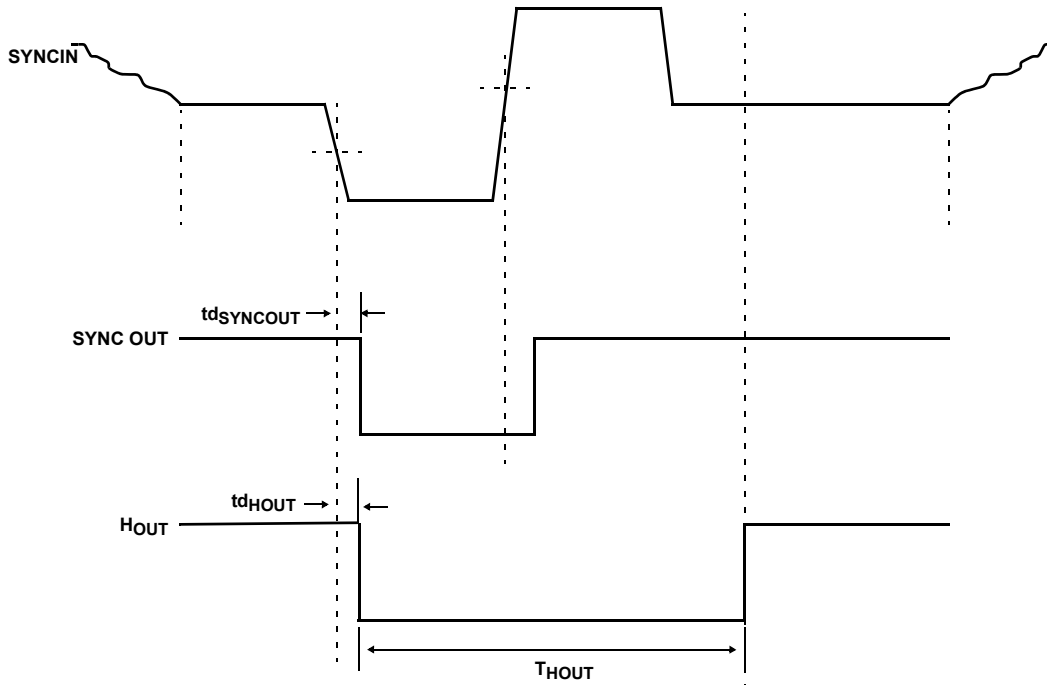


FIGURE 15. HORIZONTAL INTERVAL (HDTV) (720p)

H Timing for HDTV, With Filter (using 720p input)

| PARAMETER | DESCRIPTION | CONDITIONS | TYP @ 3.3V (Note 1) | TYP @ 5V (Note 1) | UNIT |
|----------------|----------------------------------|---------------|---------------------|-------------------|------|
| $t_{dSYNCOUT}$ | SYNCOUT Timing Relative to Input | See Figure 15 | 120 | 110 | ns |
| t_{dHOUT} | HOUT Timing Relative to Input | See Figure 15 | 112 | 100 | ns |
| T_{HOUT} | Horizontal Output Width | See Figure 15 | 200 | 200 | ns |

NOTE:

1. Delay variation is less than 2.5ns over temperature range.

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to Video In pin 2 via C_1 , nominally $0.1\mu\text{F}$. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1mA. A clamp discharge current of about $10\mu\text{A}$ is always attempting to discharge C_1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from $IT = CV$, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period - sync tip width), and C is C_1 .

An NTSC video signal has a horizontal frequency of 15.73kHz, and a sync tip width of $4.7\mu\text{s}$. This gives a period of $63.6\mu\text{s}$ and a time $T = 58.9\mu\text{s}$. The droop voltage will then be $V = 5.9\text{mV}$. This is less than 2% of a nominal sync tip amplitude of 286mV. The charge represented by this droop is replaced in a time given by $T = CV/I$, where $I =$ clamp charge current = 5.3mA. Here $T = 590\text{ns}$, about 12% of the sync pulse width of $4.7\mu\text{s}$. It is important to choose C_1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Composite Sync

The Composite Sync output is simply a reproduction of the input signal with the active video removed. The sync tip of the Composite video signal is clamped to 1.5V at pin 2 and then slices at 70mV above the sync tip reference. The output signal is buffered out to pin 1. When loss of sync, the Composite Sync output is held low.

Vertical Sync

A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the ISL59885 on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately $60\mu\text{s}$ after the last falling edge of the vertical equalizing phase.

Horizontal Sync

The horizontal circuit senses the composite sync edges and produces the true horizontal pulses of nominal width $5.2\mu\text{s}$. The leading edge is triggered from the leading edge of the input H sync, with the same propagation delay as composite sync. The half line pulses present in the input signal during vertical blanking are removed with an internal 2H line eliminator circuit. This is a circuit that inhibits horizontal output pulses until 75% of the line time is reached, then the horizontal output operation is enabled again. Any signals

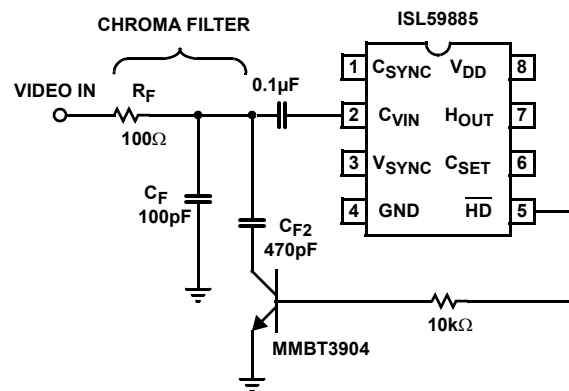
present on the I/P signal after the true H sync will be ignored, thus the horizontal output will not be affected by MacroVision copy protection. When loss of sync, the Horizontal Sync output is held high.

C_{SET}

An external C_{SET} capacitor connected from C_{SET} pin 6 to ground. C_{SET} capacitor should be a X7R grade or better as the Y5U general use capacitors may be too leaky and cause faulty operation. The C_{SET} capacitor should be very close to the C_{SET} pin to reduce possible board leakage. 56nF is recommended. C_{SET} simplified block diagram is shown in diagram 5. The C_{SET} capacitor rectifies 5 μs pulse current and creates a voltage on C_{SET} . The C_{SET} voltage is converted to bias current for H_{SYNC} and V_{SYNC} timing.

Chroma Filter

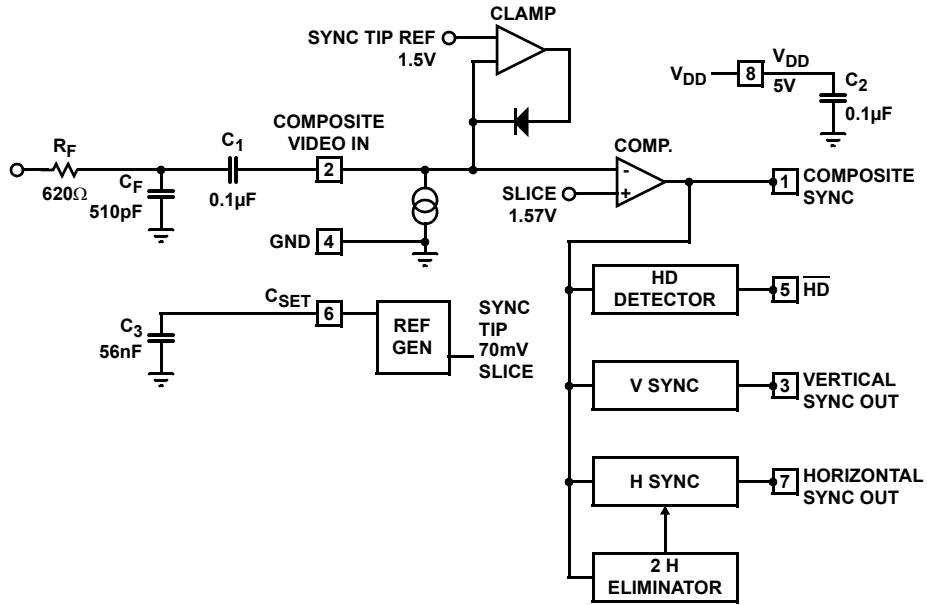
A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in the figure below. It can be implemented very simply and inexpensively with a series resistor of 100Ω and a capacitor of 570pF , which gives a single pole roll-off frequency of about 2.79MHz during NTSC or PAL. This sufficiently attenuates the 3.58MHz (NTSC) or 4.43MHz (PAL) color burst signal, yet passes the approximately 15kHz sync signals without appreciable attenuation. During HDTV, the transistor turns off and a 100pF capacitor is left to filter any noise present at the input. A chroma filter will increase the propagation delay from the composite input to the outputs.



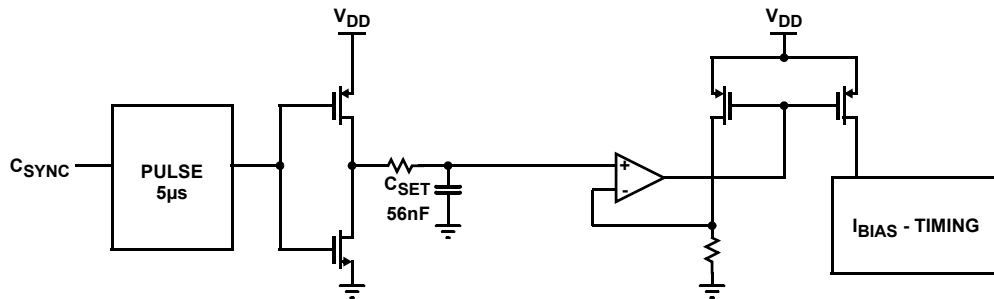
HD-Detect

High definition video is flagged by \overline{HD} going low when the input horizontal frequency is greater than 20kHz.

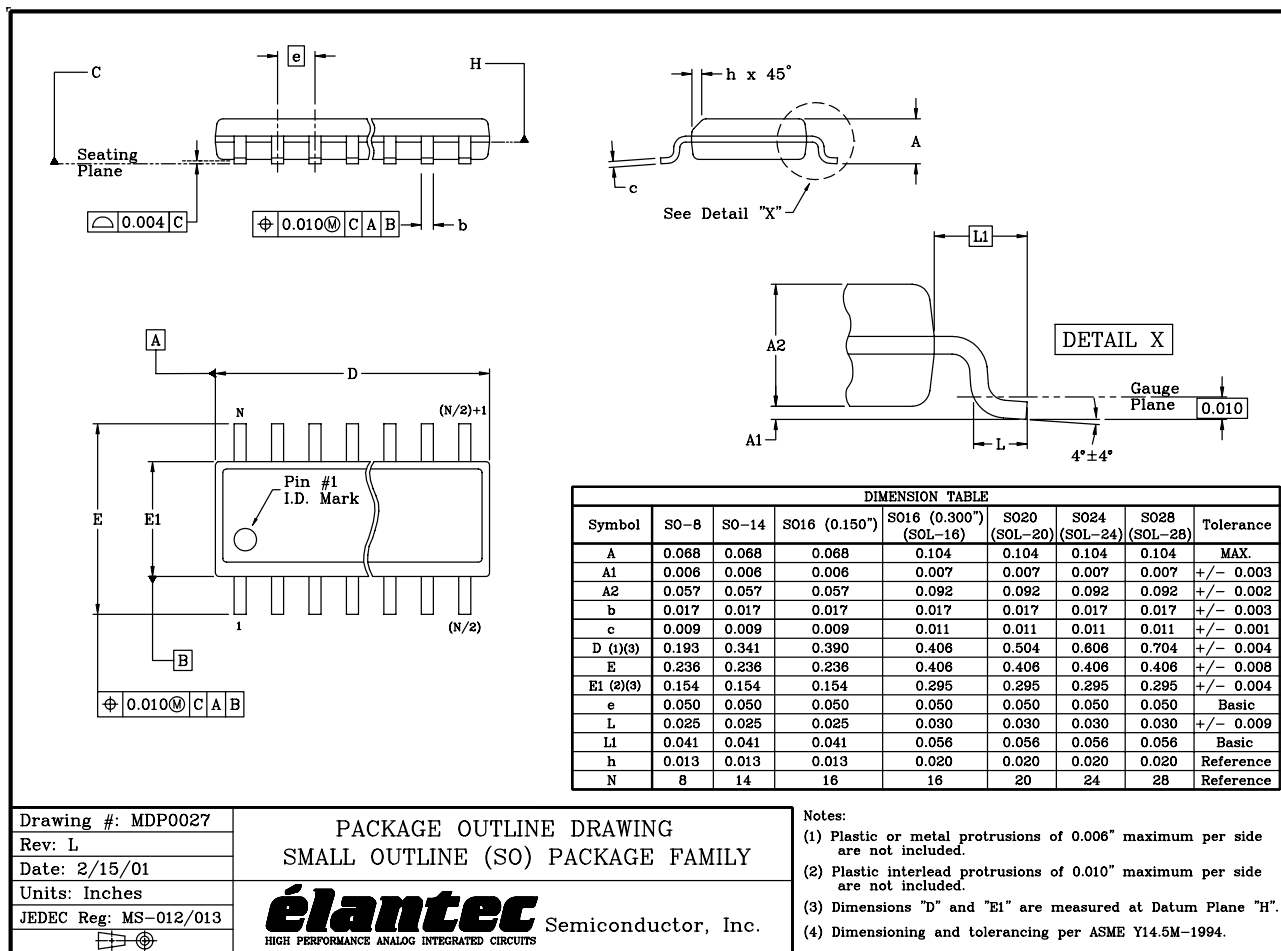
Simplified Block Diagram



C_{SET} Bias Circuit



Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

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