Data Sheet June 12, 2006 FN6220.1

16x16 Video Crosspoint

The ISL59530 is a 300MHz 16x16 Video Crosspoint Switch. Each input has an integrated DC-restore clamp and an input buffer. Each output has a fast On-Screen Display (OSD) switch (for inserting graphics or other video) and an output buffer. The switch is non-blocking, so any combination of inputs to outputs can be chosen, including one channel driving multiple outputs. The Broadcast Mode directs one input to all 16 outputs. The output buffers can be individually controlled through the SPI interface, the gain can be programmed to x1 or x2, and each output can be placed into a high impedance mode.

The ISL59530 offers a typical -3dB signal bandwidth of 300MHz. Differential gain of 0.025% and differential phase of 0.05°, along with 0.1dB flatness out to 50MHz, make the ISL59530 suitable for many video applications.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible three-wire serial interface. The ISL59530 interface is designed to facilitate both fast updates and initialization. On power-up, all outputs are high impedance to avoid output conflicts.

The ISL59530 is available in a 356 ball BGA package and specified over an extended -40°C to +85°C temperature range.

The single-supply ISL59530 can accommodate input signals from 0V to 3.5V and output voltages from 0V to 3.8V. Each input includes a clamp circuit that restores the input level to an externally applied reference in AC-coupled applications.

The ISL59531 is a fully differential input version of this device.

Features

- 16x16 non-blocking switch with buffered inputs and outputs
- 300MHz typical bandwidth
- 0.025%/0.05° dG/dP
- Output gain switchable x1 or x2 for each channel
- Individual outputs can be put in a high impedance state
- -90dB Isolation at 6MHz
- SPI digital interface
- Single +5V supply operation
- Pb-free plus anneal available (RoHS compliant)

Applications

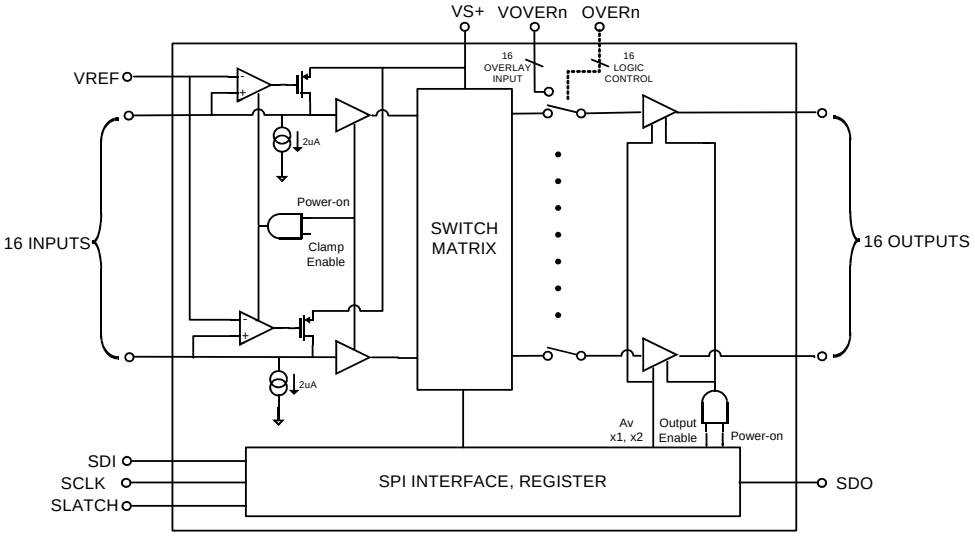
- Security camera switching
- RGB routing
- HDTV routing

Ordering Information

PART NUMBER	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59530IKZ (Note)	-	356 Ld PBGA (Pb-free)	V356.27x27

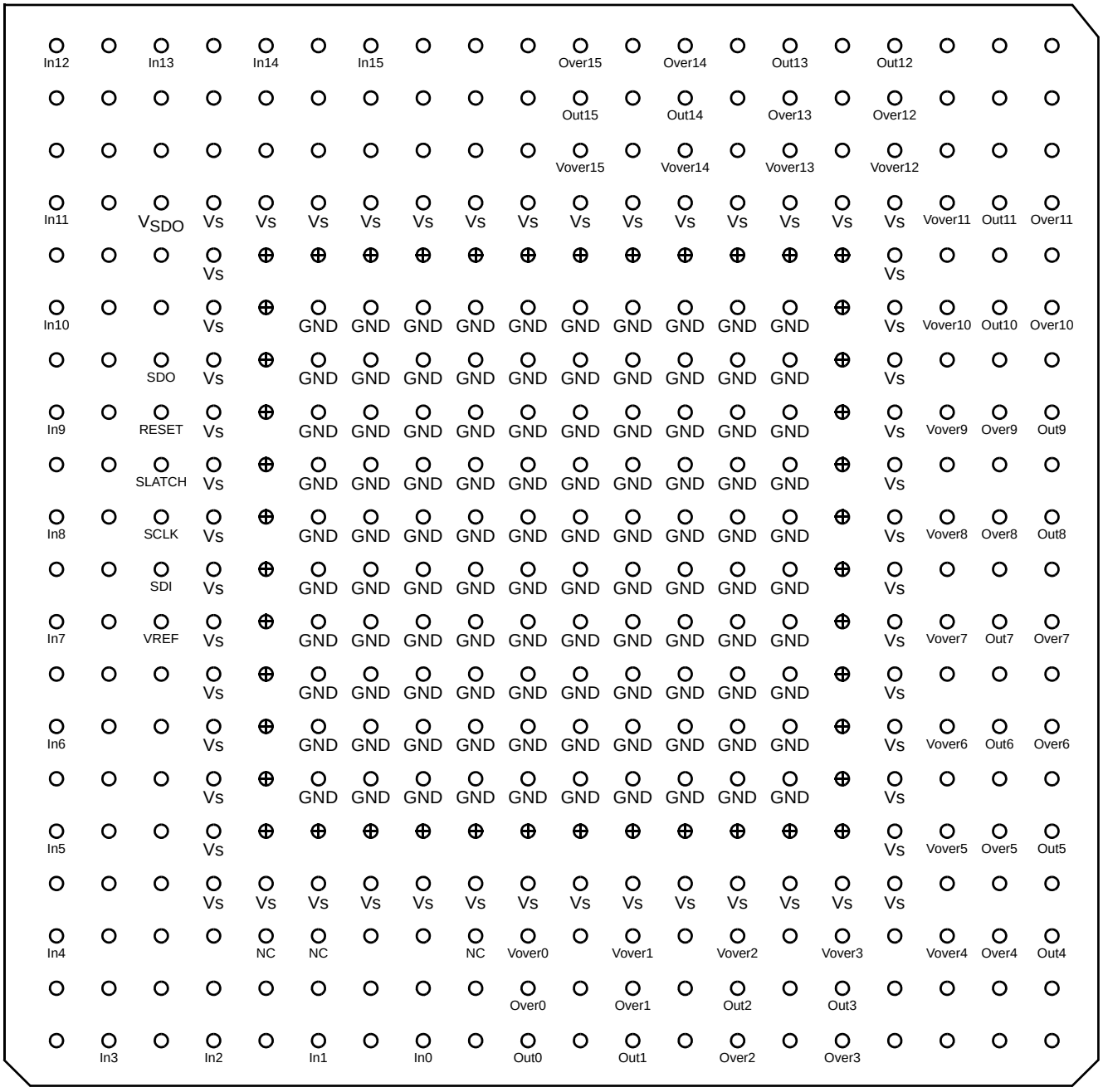
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pinout

ISL59530
(356 LD BGA)
TOP VIEW



⊕ = NO BALLS

Balls labelled "NC" should be left unconnected - do not tie them to ground!
Balls with no labels may be tied to ground to slightly reduce thermal impedance.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S and GND 6.0V
Maximum Continuous Output Current 40mA
Ambient Operating Temperature . . . . . -40°C to +85°C
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Maximum power supply (V_S) slew rate 1V/µs
ESD Classification
Human Body Model 1500V
Machine Model 100V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = 5V, R_L = 150Ω unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_S	Power Supply Voltage		4.5		5.5	V
V_{SDO}	Power Supply for SDO output pin	Establishes serial data output high level	1.2		5.5	V
A_V	Gain	A_V = 1	0.98	1	1.02	V/V
		A_V = 2	1.96	2	2.04	V/V
GM	Gain Matching (to average of all other outputs)	A_V = 1	-1.5		+1.5	%
		A_V = 2	-1.5		+1.5	%
V_{IN}	Video Input Voltage Range	A_V = 1	0		3.5	V
V_{OUT}	Video Output Voltage Range	A_V = 2	0.1		3.8	V
I_B	Input Bias Current	Clamp function disabled (DC coupled inputs)	-10	-5	1	µA
		Clamp function enabled, $V_{IN} = V_{REF}$ + 0.5V	0.5	2	10	µA
V_{OS}	Output Offset Voltage	A_V = 1	-20	8	35	mV
		A_V = 2	-70	-10	40	mV
I_{OUT}	Output Current	Sourcing, R_L = 10Ω to GND	60	108		mA
		Sinking, R_L = 10Ω to 2.5V	24	31		mA
PSRR	Power Supply Rejection Ratio	A_V = 1 and A_V = 2	50	70		dB
I_S	Supply Current	Enabled, all outputs enabled, no load current	275	320	360	mA
		Enabled, all outputs disabled, no load current	135	165	195	mA
		Disabled	1.2	1.8	2.4	mA

AC Electrical Specifications

V_S = 5V, R_L = 150Ω unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW -3dB	3dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		300		MHz
BW 0.1dB	0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		50		MHz
SR	Slew Rate	V_{OUT} = 2V_{P-P}, A_V = 2	300	520	740	V/µs
T_S	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}, A_V = 2		12		ns
Glitch	Switching Glitch, Peak	A_V = 1		40		mV
T_{over}	Overlay Delay Time	From OVER rising edge to output transition		6		ns
dG	Diff Gain	A_V = 2, R_L = 150Ω		0.025		%
dP	Diff Phase	A_V = 2, R_L = 150Ω		0.05		°
Xt	Hostile Crosstalk	6MHz		-85		dB
V_N	Input Referred Noise Voltage			18		nV/√Hz

Pin Descriptions

NAME	NUMBER	DESCRIPTION
IN0	Y8	Crosspoint Video Input
IN1	Y6	Crosspoint Video Input
IN2	Y4	Crosspoint Video Input
IN3	Y2	Crosspoint Video Input
IN4	V1	Crosspoint Video Input
IN5	T1	Crosspoint Video Input
IN6	P1	Crosspoint Video Input
IN7	M1	Crosspoint Video Input
IN8	K1	Crosspoint Video Input
IN9	H1	Crosspoint Video Input
IN10	F1	Crosspoint Video Input
IN11	D1	Crosspoint Video Input
IN12	A1	Crosspoint Video Input
IN13	A3	Crosspoint Video Input
IN14	A5	Crosspoint Video Input
IN15	A7	Crosspoint Video Input
OUT0	Y10	Crosspoint Video Output
OUT1	Y12	Crosspoint Video Output
OUT2	W14	Crosspoint Video Output
OUT3	W16	Crosspoint Video Output
OUT4	V20	Crosspoint Video Output
OUT5	T20	Crosspoint Video Output
OUT6	P19	Crosspoint Video Output
OUT7	M19	Crosspoint Video Output
OUT8	K20	Crosspoint Video Output
OUT9	H20	Crosspoint Video Output
OUT10	F19	Crosspoint Video Output
OUT11	D19	Crosspoint Video Output
OUT12	A17	Crosspoint Video Output
OUT13	A15	Crosspoint Video Output
OUT14	B13	Crosspoint Video Output
OUT15	B11	Crosspoint Video Output
OVER0	W10	Overlay Logic Control (with pulldown)
OVER1	W12	Overlay Logic Control (with pulldown)
OVER2	Y14	Overlay Logic Control (with pulldown)
OVER3	Y16	Overlay Logic Control (with pulldown)
OVER4	V19	Overlay Logic Control (with pulldown)
OVER5	T19	Overlay Logic Control (with pulldown)

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
OVER6	P20	Overlay Logic Control (with pulldown)
OVER7	M20	Overlay Logic Control (with pulldown)
OVER8	K19	Overlay Logic Control (with pulldown)
OVER9	H19	Overlay Logic Control (with pulldown)
OVER10	F20	Overlay Logic Control (with pulldown)
OVER11	D20	Overlay Logic Control (with pulldown)
OVER12	B17	Overlay Logic Control (with pulldown)
OVER13	B15	Overlay Logic Control (with pulldown)
OVER14	A13	Overlay Logic Control (with pulldown)
OVER15	A11	Overlay Logic Control (with pulldown)
VOVER0	V10	Overlay Video Input
VOVER1	V12	Overlay Video Input
VOVER2	V14	Overlay Video Input
VOVER3	V16	Overlay Video Input
VOVER4	V18	Overlay Video Input
VOVER5	T18	Overlay Video Input
VOVER6	P18	Overlay Video Input
VOVER7	M18	Overlay Video Input
VOVER8	K18	Overlay Video Input
VOVER9	H18	Overlay Video Input
VOVER10	F18	Overlay Video Input
VOVER11	D18	Overlay Video Input
VOVER12	C17	Overlay Video Input
VOVER13	C15	Overlay Video Input
VOVER14	C13	Overlay Video Input
VOVER15	C11	Overlay Video Input
VREF	M3	DC-restore clamp reference input. In an AC-coupled configuration (DC-Restore clamp enabled), the sync tip of composite video inputs will be restored to this level. Set to 0.3 to 0.7V for optimum performance. In an DC-coupled configuration (DC-Restore clamp disabled), this pin should be tied to ground. **Never let the** VREF **pin float!** A floating VREF pin drifts high (and if the clamp function is enabled) will cause all of the outputs to simultaneously try to drive ~4V DC into their 150Ω loads.
SLATCH	J3	Serial Latch. Serial data is latched into ISL59530 on rising edge of SLATCH.

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
SCLK	K3	Serial data clock
SDI	L3	Serial data input
SDO	G3	Serial data output. Can be tied to SDI of another ISL59530 to enable daisy-chaining of multiple devices.
RESET	H3	Reset input. Pull high then low to reset device, but not needed in normal operation. Tie to ground in final application.
V_{SDO}	D3	Power supply for SDO pin. Tie to +5V for a 0 to 5V SDO output signal swing.
V_S		+5V power supply
GND		Ground
NC		No Connect - *Do not electrically connect to anything, including ground*.

Typical Performance Curves

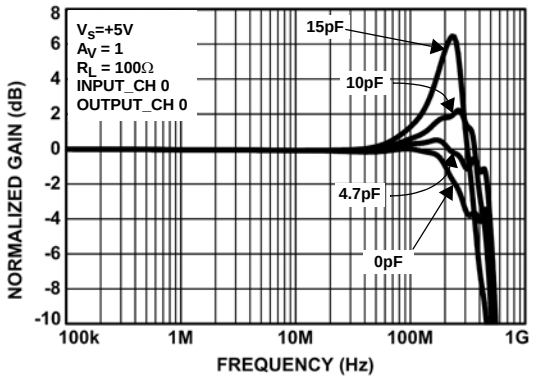


FIGURE 1. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, MUX MODE

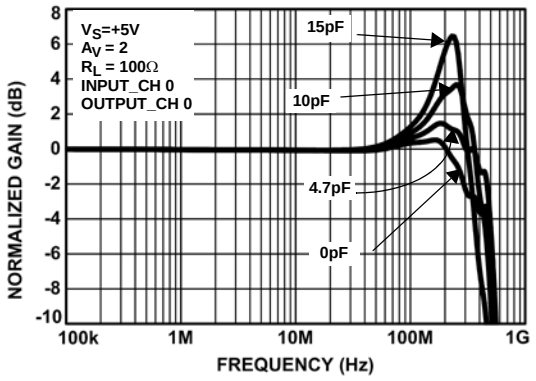


FIGURE 2. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, MUX MODE

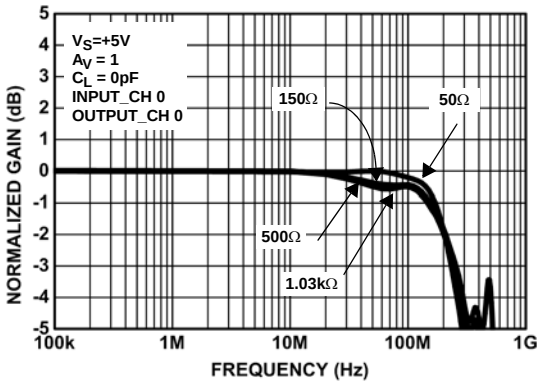


FIGURE 3. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, MUX MODE

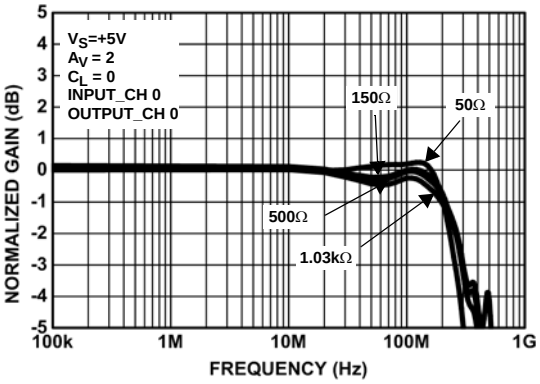


FIGURE 4. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, MUX MODE

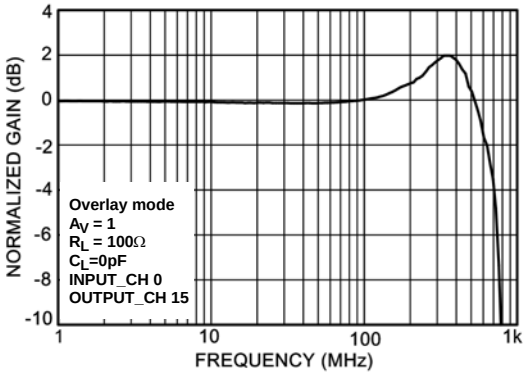


FIGURE 5. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 1

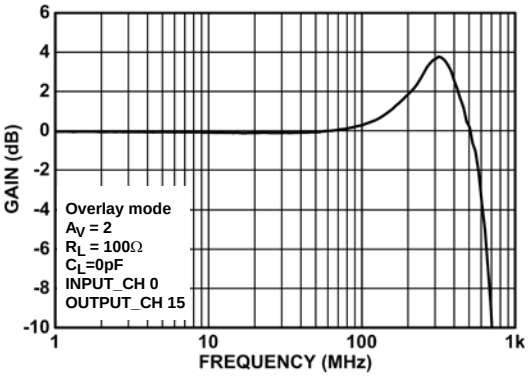


FIGURE 6. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 2

Typical Performance Curves (Continued)

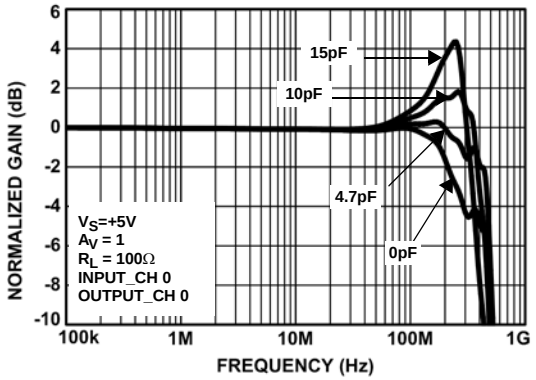


FIGURE 7. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, BROADCAST MODE

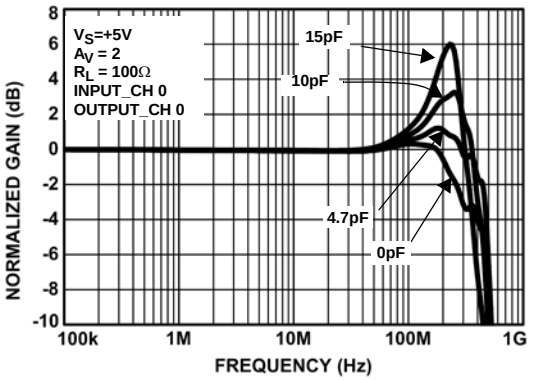


FIGURE 8. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, BROADCAST MODE

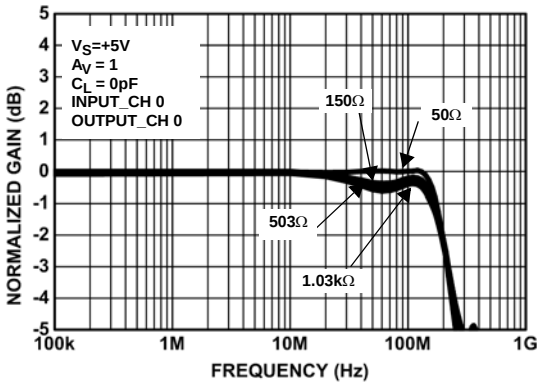


FIGURE 9A. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, BROADCAST MODE

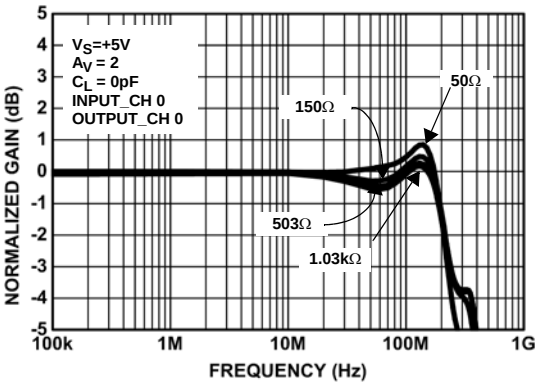


FIGURE 10. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, BROADCAST MODE

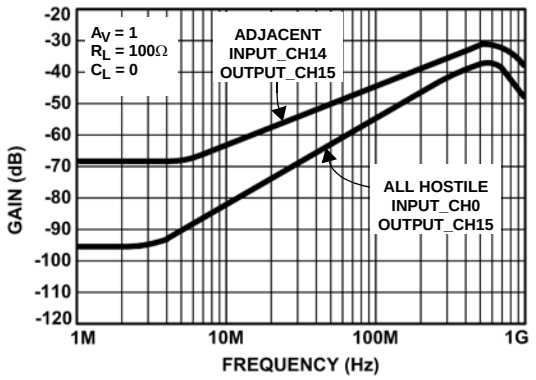


FIGURE 11. CROSSTALK - A_V = 1

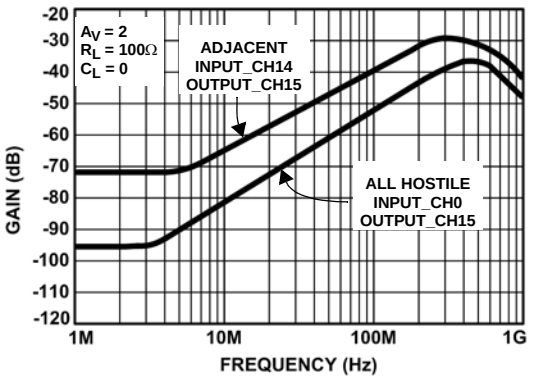


FIGURE 12. CROSSTALK - A_V = 2

Typical Performance Curves (Continued)

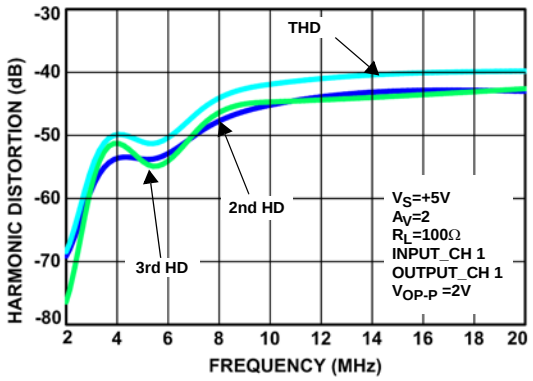


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

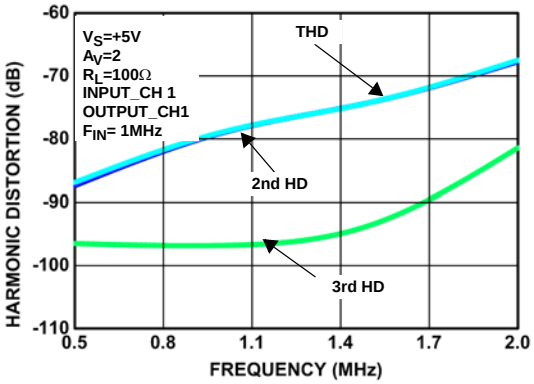


FIGURE 14. HARMONIC DISTORTION vs V_{OUT_P-P}

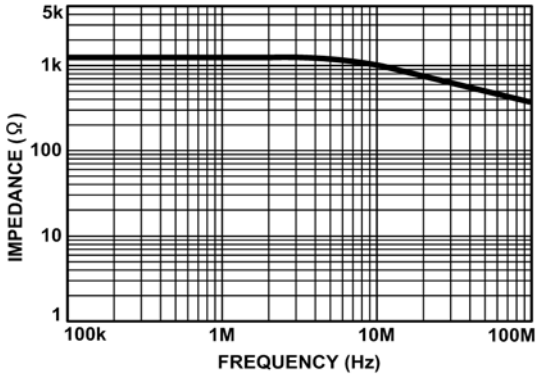


FIGURE 15. DISABLED OUTPUT IMPEDANCE

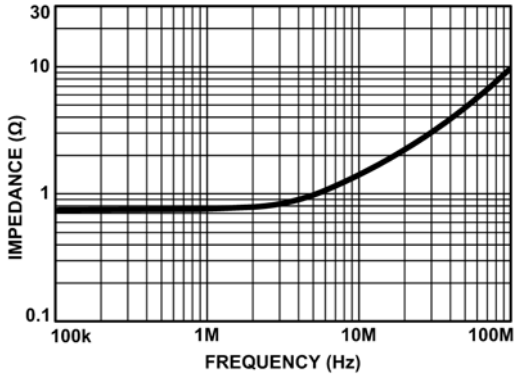


FIGURE 16. ENABLED OUTPUT IMPEDANCE

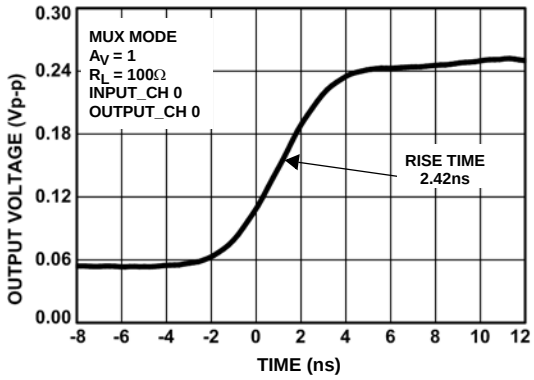


FIGURE 17. RISE TIME - A_V = 1

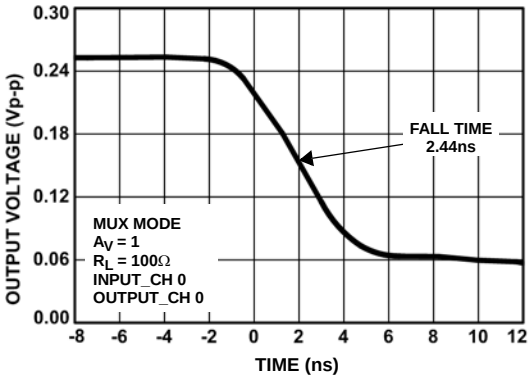


FIGURE 18. FALL TIME - A_V = 1

Typical Performance Curves (Continued)

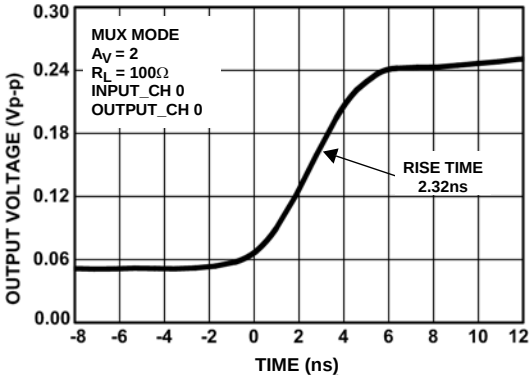


FIGURE 19. RISE TIME - A_V = 2

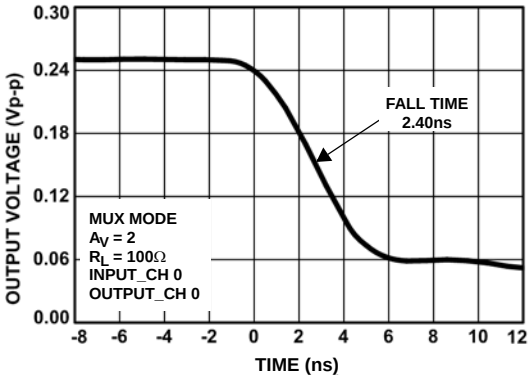


FIGURE 20. FALL TIME - A_V = 2

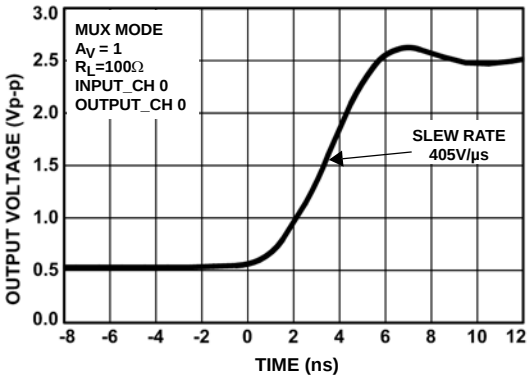


FIGURE 21. RISING SLEW RATE - A_V = 1

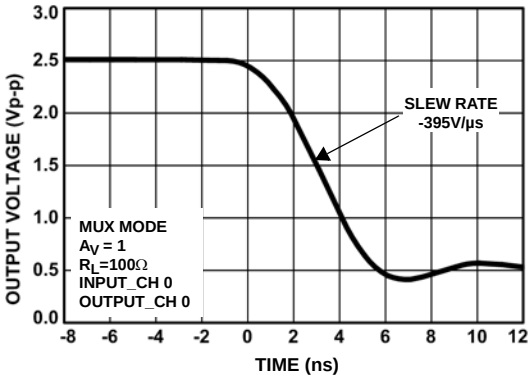


FIGURE 22. FALLING SLEW RATE - A_V = 1

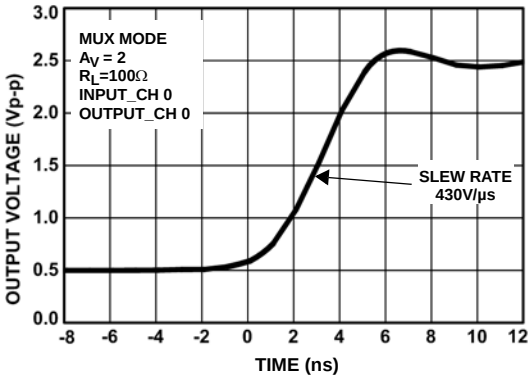


FIGURE 23. RISING SLEW RATE - A_V = 2

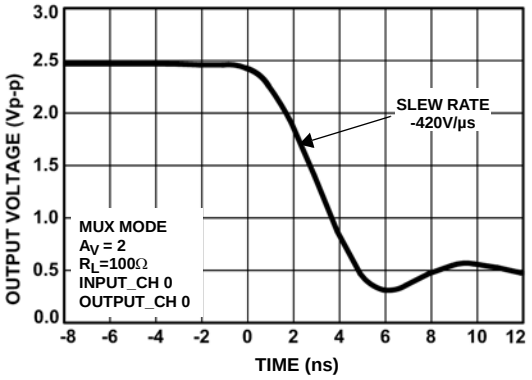


FIGURE 24. FALLING SLEW RATE - A_V = 2

Typical Performance Curves (Continued)

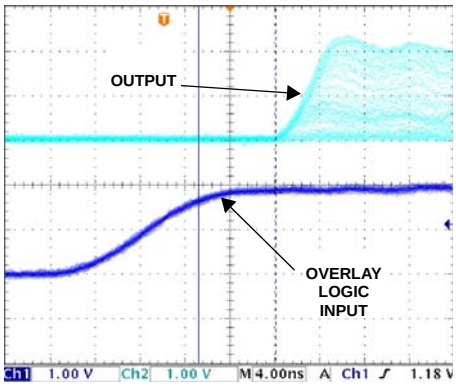


FIGURE 25. OVERLAY SWITCH TURN-ON DELAY TIME

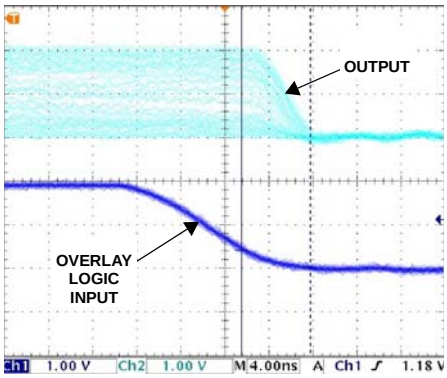


FIGURE 26. OVERLAY SWITCH TURN-OFF DELAY TIME

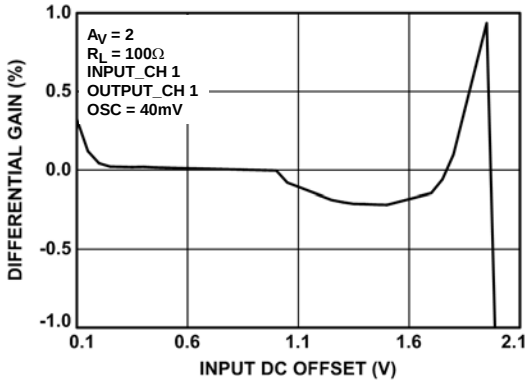


FIGURE 27. DIFFERENTIAL GAIN, A_V = 2

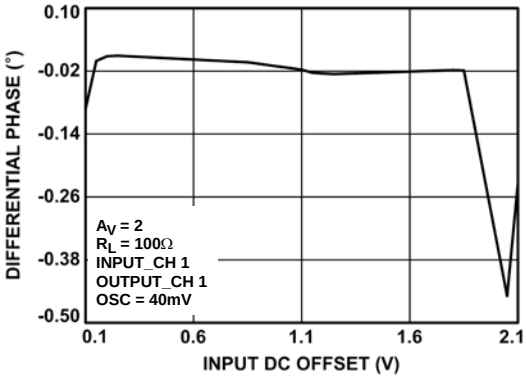


FIGURE 28. DIFFERENTIAL PHASE, A_V = 2

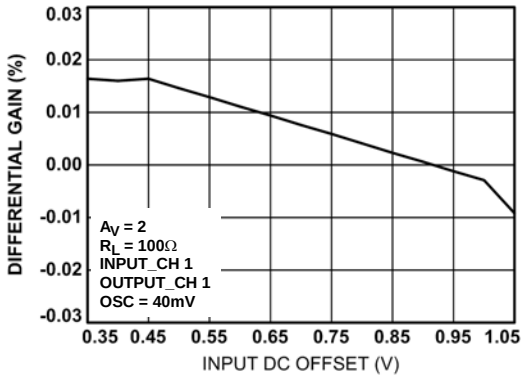


FIGURE 29. DIFFERENTIAL GAIN, A_V = 2

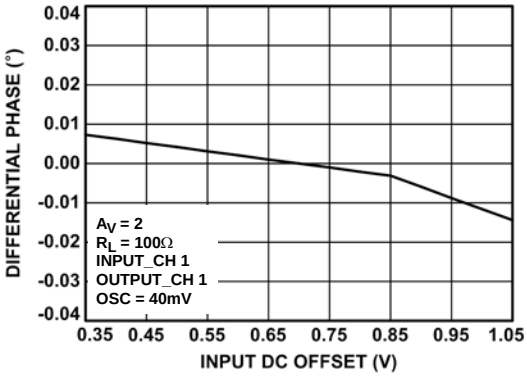


FIGURE 30. DIFFERENTIAL PHASE, A_V = 2

Typical Performance Curves (Continued)

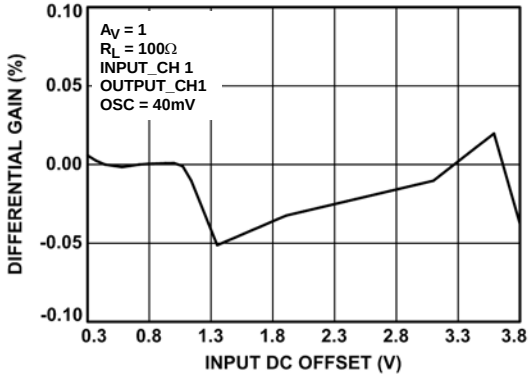


FIGURE 31. DIFFERENTIAL GAIN, A_V = 1

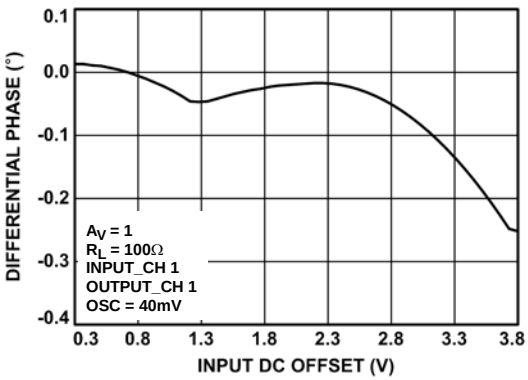


FIGURE 32. DIFFERENTIAL PHASE, A_V = 1

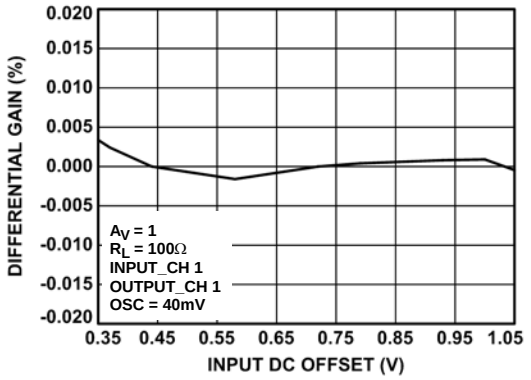


FIGURE 33. DIFFERENTIAL GAIN, A_V = 1

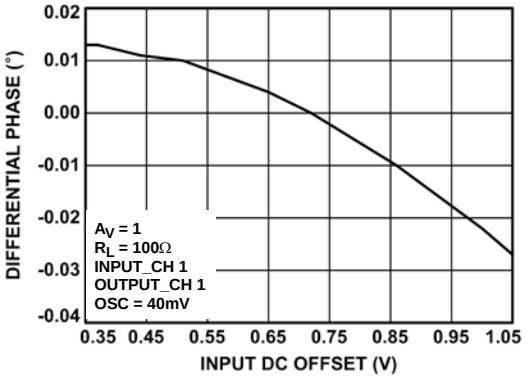


FIGURE 34. DIFFERENTIAL GAIN, A_V = 1

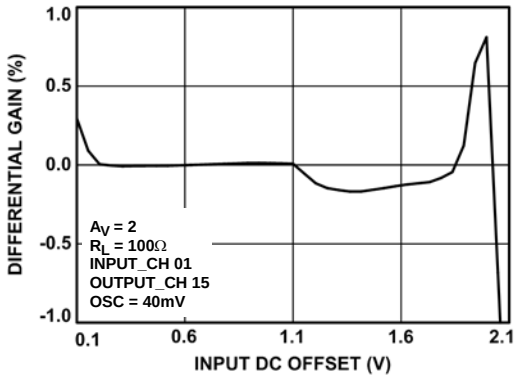


FIGURE 35. DIFFERENTIAL GAIN, A_V = 2

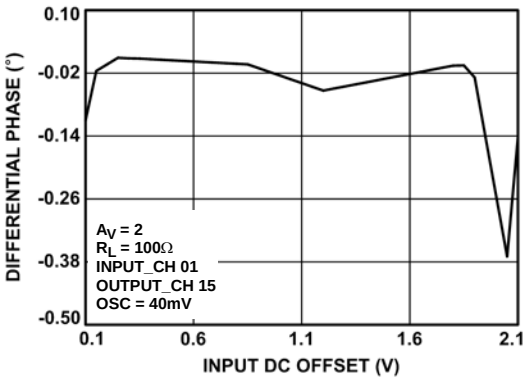


FIGURE 36. DIFFERENTIAL PHASE, A_V = 2

Typical Performance Curves (Continued)

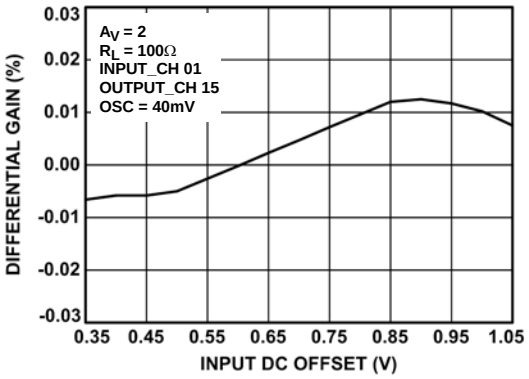


FIGURE 37. DIFFERENTIAL GAIN, A_V = 2

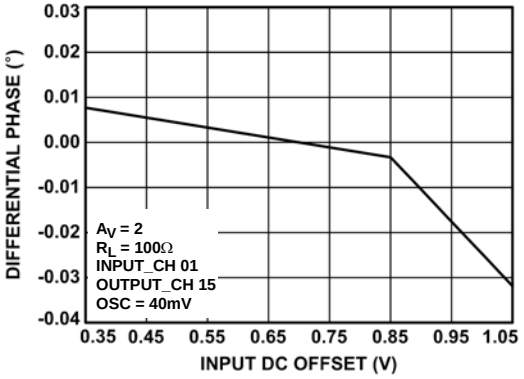


FIGURE 38. DIFFERENTIAL PHASE, A_V = 2

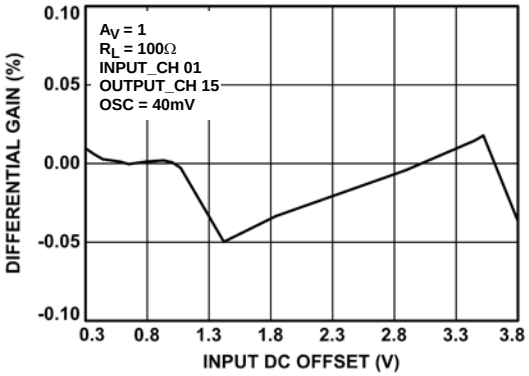


FIGURE 39. DIFFERENTIAL GAIN, A_V = 1

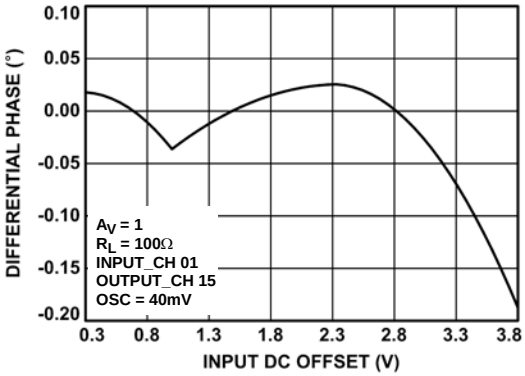


FIGURE 40. DIFFERENTIAL PHASE, A_V = 1

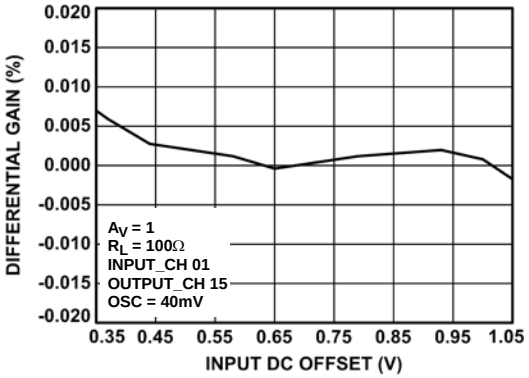


FIGURE 41. DIFFERENTIAL GAIN, A_V = 1

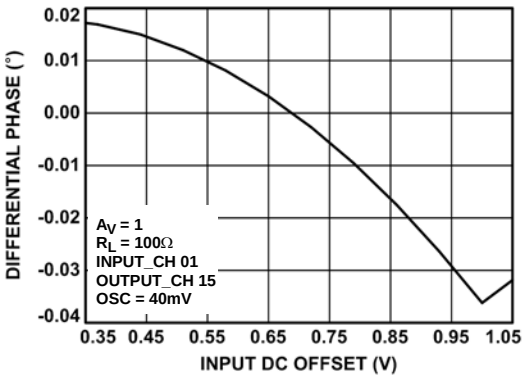


FIGURE 42. DIFFERENTIAL PHASE, A_V = 1

Typical Performance Curves (Continued)

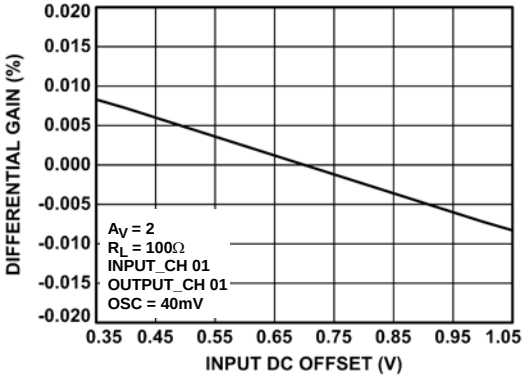


FIGURE 43. DIFFERENTIAL GAIN, OVERLAY, A_V = 2

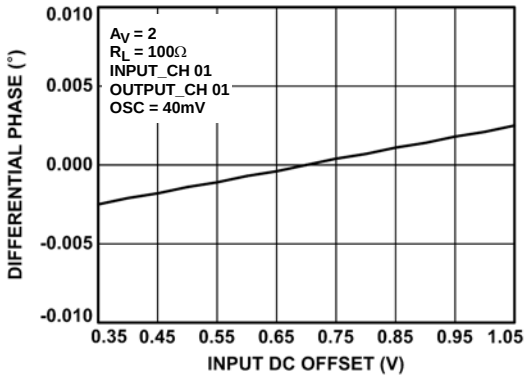


FIGURE 44. DIFFERENTIAL PHASE, OVERLAY, A_V = 2

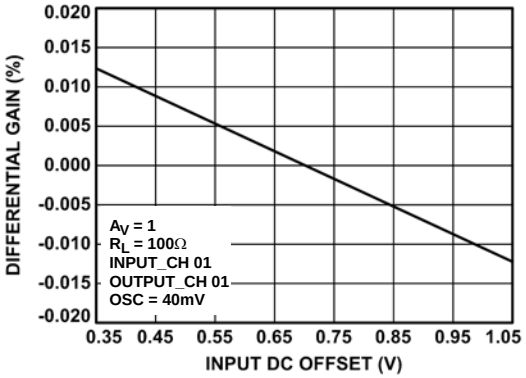


FIGURE 45. DIFFERENTIAL GAIN, OVERLAY, A_V = 1

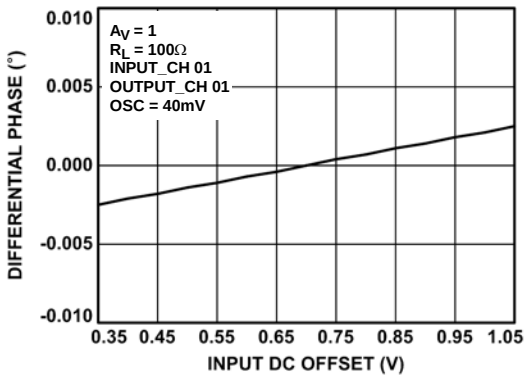


FIGURE 46. DIFFERENTIAL PHASE, OVERLAY, A_V = 1

3dB Bandwidth, MUX Mode, A_V = 1, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	255	229	229	210	222	221	224	190	169	152	233	190	212	189	207	166
	1	244	217						180	168						193	160
	2	257		235					186	171					204		169
	3	264			217				183	175				219			171
	4	255				220			174	177			202				167
	5	253					218		176	177		237					173
	6	247						226	171	178	157						170
	7	253	227	235	218	223	228	230	174	184	163	240	223	219	217	211	178
	8	255	236	240	239	223	236	231	175	187	168	241	242	222	235	213	183
	9	241						210	169	188	165						182
	10	235					236		168	186		230					185
	11	223				207			164	188			225				186
	12	220			209				161	192				205			185
	13	211		214					160	192					224		189
	14	199	212						160	194						197	193
	15	193	217	207	202	185	216	186	222	197	177	225	217	198	223	197	238

3dB Bandwidth, MUX Mode, A_V = 2, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	295	316	290	397	384	405	395	220	288	240	299	250	385	234	396	188
	1	268	290						211	183						291	183
	2	277		300					216	192					289		196
	3	279			408				213	196				392			196
	4	269				391			201	192			402				192
	5	263					407		201	196		298					200
	6	259						404	196	196	283						200
	7	263	411	307	402	387	412	398	201	205	407	307	402	387	413	398	211
	8	262	407	308	402	383	412	394	203	212	411	300	403	385	415	394	216
	9	253						388	194	210	410						214
	10	253					417		194	215		293					216
	11	246				385			187	213			412				217
	12	241			412				184	216				391			225
	13	236		272					182	220					419		225
	14	233	279						178	220						396	230
	15	227	274	244	396	367	407	230	183	223	324	276	400	379	413	385	293

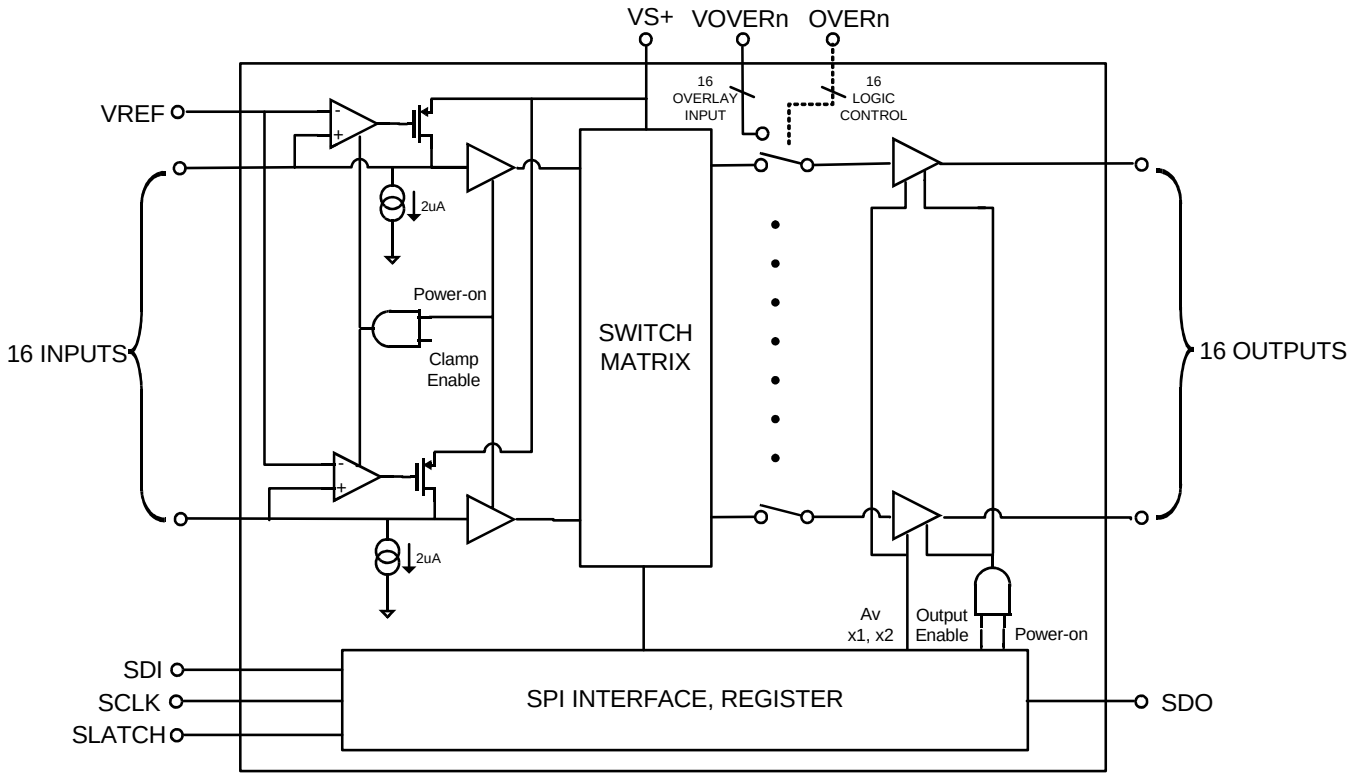
3dB Bandwidth, Broadcast Mode, A_V = 1, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	215	198	195	183	184	188	172	178	151	145	157	145	140	146	144	158
	1	214	195						174	152						144	158
	2	210		188					171	153					147		159
	3	212			178				171	157				143			164
	4	206				174			169	157			150				164
	5	203					177		165	159		161					164
	6	201						156	163	159	151						164
	7	204	187	182	170	170	175	160	167	167	156	168	157	151	158	154	170
	8	204	187	183	172	171	176	161	167	171	160	172	160	155	161	159	175
	9	202						157	164	170	160						174
	10	196					170		160	169		169					178
	11	194				161			157	171			160				174
	12	193			162				156	171				156			178
	13	191		170					151	174					164		178
	14	189	172						151	175						162	178
	15	187	173	167	157	155	161	149	153	178	167	179	167	160	166	164	181

3dB Bandwidth, Broadcast Mode, A_V = 2, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	234	216	209	199	204	205	190	196	169	160	172	162	158	163	161	178
	1	232	215						193	169						161	178
	2	228		204					189	171					164		178
	3	229			196				191	175				163			182
	4	223				193			186	177			168				183
	5	219					192		183	177		177					183
	6	217						174	181	178	167						183
	7	220	204	198	189	190	192	175	183	184	173	184	174	169	174	172	189
	8	220	205	199	190	191	193	177	184	187	178	188	178	173	178	178	193
	9	218						174	181	188	178						193
	10	220					185		176	186		187					192
	11	212				179			174	188			177				192
	12	211			179				174	192				176			195
	13	209		187					170	192					181		195
	14	208	191						167	194						181	196
	15	205	191	184	172	171	176	160	166	197	185	195	184	179	185	182	198

Block Diagram



General Description

The ISL59530 is a 16x16 integrated video crosspoint switch matrix with input and output buffers and On-Screen Display (OSD) insertion. This device operates from a single +5V supply. Any output can be generated from any of the 16 input video signal sources, and each output can have OSD information inserted through a dedicated, fast 2:1 mux located before the output buffer. There is also a Broadcast mode allowing any one input to be broadcast to all 16 outputs. A DC restore clamp function enables the ISL59530 to AC-couple incoming video.

The ISL59530 offers a -3dB signal bandwidth of 300MHz. Differential gain and differential phase of 0.025% and 0.05° respectively, along with 0.1dB flatness out to 50MHz make this ideal for multiplexing composite NTSC and PAL signals. The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59530 interface is designed to facilitate both fast initialization and configuration changes. On power-up, all outputs are initialized to the disabled state to avoid output conflicts in the user's system.

Digital Interface

The ISL59530 uses a serial interface to program the configuration registers. The serial interface uses three signals (SCLK, SDI, and SLATCH) for programming the ISL59530, while a fourth signal (SDO) enables optional daisy-chaining of multiple devices. The serial clock can run at up to 5MHz (5Mbits/s).

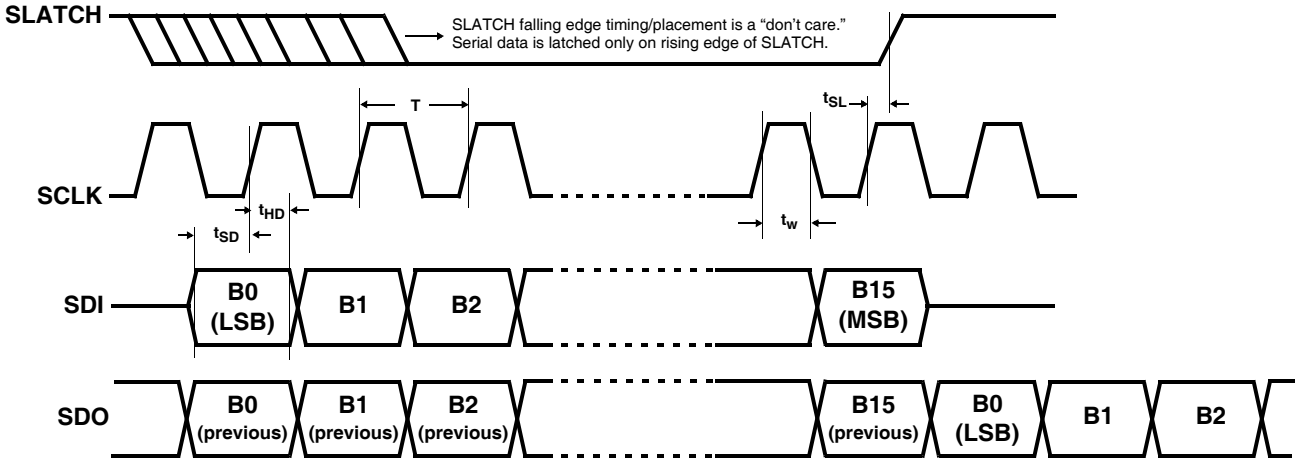
Serial Interface

The ISL59530 is programmed through a simple serial interface. Data on the SDI (serial data input) pin is shifted into a 16-bit shift register on the rising edge of the SCLK (serial clock) signal. (This is continuously done regardless of the state of the SLATCH signal.) The LSB (bit 0) is loaded first and the MSB (bit 15) is loaded last (see the Serial Timing Diagram). After all 16 bits of data have been loaded into the shift register, the rising edge of SLATCH updates the internal registers.

While the ISL59530 has an SDO (Serial Data Out) pin, it does not have a register readback feature. The data on the SDO pin is an exact replica of the incoming data on the SDI pin, delayed by 15.5 SCLKs (an input bit is latched on the rising edge of SLCK, and is output on SDO on the falling edge of SLCK 15.5 SCLKs later). Multiple ISL59530's can be daisy-chained by connecting the SDO of one to the SDI of the other, with SCLK and SLATCH common to all the daisy-chained parts. After all the serial data is transmitted (16 bits * n devices = 16*n SCLKs), the rising edge of SLATCH will update the configuration registers of all n devices simultaneously.

The Serial Timing Diagram and Serial Timing Parameters table show the timing requirements for the serial interface.

Serial Timing Diagram



SDO = SDI delayed by 15.5 SCLKs to allow daisy-chaining of multiple ISL59530s. SDO changes on the falling edge of SCLK.

TABLE 1. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	SCLK period
t_W	0.50 * T	Clock Pulse Width
t_{SD}	≥20ns	Data Setup Time
t_{HD}	≥20ns	Data Hold Time
t_{SL}	≥20ns	Final SLCK rising edge (latching B15) to SLATCH rising edge

Programming Model

The ISL59530 is configured by a series of 16 bit serial control words. The three MSBs (B15-13) of each serial word determine the basic command:

TABLE 2. COMMAND FORMAT

B15	B14	B13	COMMAND	NUMBER OF WRITES
0	0	0	INPUT/OUTPUT: Maps input channels to output channels	16 (1 channel per write)
0	0	1	OUTPUT ENABLE: Output enable for individual channels	4 (4 channels per write)
0	1	0	GAIN SET: Gain (x1 or x2) for each channel	4 (4 channels per write)
0	1	1	BROADCAST: Enables broadcast mode and selects the input channel to be broadcast to all output channels	1
1	1	1	CONTROL: Clamp on/off, operational/standby mode, and global output enable/disable	1

Mapping Inputs to Outputs

Inputs are mapped to their desired outputs using the input/output control word. Its format is:

TABLE 3. INPUT/OUTPUT WORD

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	I_3	I_2	I_1	I_0	0	0	0	0	O_3	O_2	O_1	O_0	0

I_3:I_0 form the 4 bit word indicating the input channel (0 to 15), and O_3:O_0 determine the output channel which that input channel will map to. One input can be mapped to one or multiple outputs. To fully program the ISL59530, 16 INPUT/OUTPUT words must be transmitted - one for each input channel.

Enabling Outputs

The output enable control word is used to enable individual outputs. There are 16 channels to configure, so this is accomplished by writing 4 serial words, each controlling a bank of four outputs at a time. The bank is selected by bits B9 and B8. The output enable control word format is:

TABLE 4. OUTPUT ENABLE FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	0	0	0	**0**	**0**		O_3		O_2		O_1		O_0
0	0	1	0	0	0	**0**	**1**		O_7		O_6		O_5		O_4
0	0	1	0	0	0	**1**	**0**		O_{11}		O_{10}		O_9		O_8
0	0	1	0	0	0	**1**	**1**		O_{15}		O_{14}		O_{13}		O_{12}

Setting the O_N bit = 0 tristates the output. Setting the O_N bit = 1 enables the output if the Global Output Enable bit is also set (the individual output enable bits are ANDed with the Global Output Enable bit before they are sent to the output stage).

Setting the Gain

The gain of each output may be set to x1 or x2 using the Gain Set word. It is in the same format as the output enable control word:

TABLE 5. GAIN SET FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	0	0	**0**	**0**		G_3		G_2		G_1		G_0
0	1	0	0	0	0	**0**	**1**		G_7		G_6		G_5		G_4
0	1	0	0	0	0	**1**	**0**		G_{11}		G_{10}		G_9		G_8
0	1	0	0	0	0	**1**	**1**		G_{15}		G_{14}		G_{13}		G_{12}

Set G_N = 0 for a gain of x1 or 1 for a gain of x2.

Broadcast Mode

The Broadcast Mode routes one input to all 16 outputs. The broadcast control word is:

TABLE 6. BROADCAST FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	I_3	I_2	I_1	I_0	0	0	0	0	0	0	0	0	Enable Broadcast 0: Broadcast Mode Disabled 1: Broadcast Mode Enabled

I_3:I_0 form the 4 bit word indicating the input channel (0 to 15) to be sent to all 16 outputs. Set the Enable Broadcast bit (B0) = 1 to enable Broadcast Mode, or to 0 to disable Broadcast Mode. When Broadcast Mode is disabled, the previous channel assignments are restored.

Control Word

The ISL59530's power-on reset disables all outputs and places the part in a low-power standby mode. To enable the device, the following control word should be sent:

TABLE 7. CONTROL WORD FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	0	0	Clamp 0: Clamp Disabled 1: Clamp Enabled	0	0	0	0	0	0	0	Power 0: Standby 1: Operational	Global Output Enable 0: All outputs tristated 1: Individual Output Enable bits control outputs

The Clamp bit enables the input clamp function, forcing the AC-coupled signal's most negative point to be equal to V_{REF}.

Note: The Clamp bit turns the DC-Restore clamp function on or off for *all* channels - there is no DC-Restore on/off control for individual channels. The DC-Restore function only works with signals with sync tips (composite video). Signals that do not have sync tips (the Chroma/C signal in s-video and the Pb, Pr signals in Component video), will be severely distorted if run through a DC-Restore/clamp function.

For this reason, the ISL59530 must be in DC-coupled mode (Clamp Disabled) to be compatible with s-video and component video signals.

Bandwidth Considerations

Wide frequency response (high bandwidth) in a video system means better video resolution. Four sets of frequency response curves are shown in Figure 47. Depending on the switch configurations, and the routing (the path from the input to the output), bandwidth can vary between 100MHz and 350MHz. A short discussion of the trade-offs — including matrix configuration, output buffer gain selection, channel selection, and loading — follows.

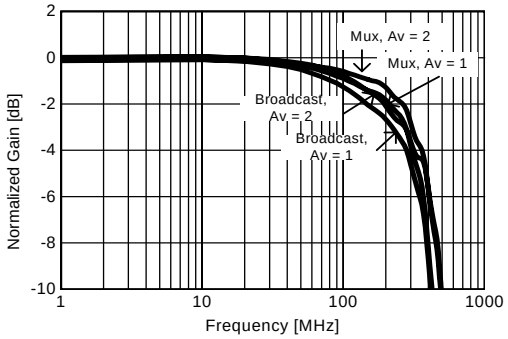


FIGURE 47. FREQUENCY RESPONSE FOR VARIOUS MODES

In multiplexer mode, one input typically drives one output channel, while in broadcast mode, one input drives all 16 outputs. As the number of outputs driven increases, the parasitic loading on that input increases. Broadcast Mode is the worst-case, where the capacitance of all 16 channels loads one input, reducing the overall bandwidth. In addition, due to internal device compensation, an output buffer gain of x2 has higher bandwidth than a gain of x1. Therefore, the highest bandwidth configuration is multiplexer mode (with each input mapped to only one output) and an output buffer gain of x2.

The relative locations of the input and output channels also have significant impact on the device bandwidth (due to the layout of the ISL59530 silicon). When the input and output channels are further away, there are additional parasitics as a result of the additional routing, resulting in lower bandwidth.

The bandwidth does not change significantly with resistive loading as shown in the typical performance curves. However several of the curves demonstrate that frequency response is sensitive to capacitance loading. This is most significant when laying out the PCB. If the PCB trace length between the output of the crosspoint switch and the back-termination resistor is not minimized, the additional parasitic capacitance will result in some peaking and eventually a reduction in overall bandwidth.

Linear Operating Region

In addition to bandwidth optimization, to get the best linearity the ISL59530 should be configured to operate in its most linear operating region. Figure 48 shows the differential gain curve. The ISL59530 is a single supply 5V design with its most linear region between 0.1 and 2V. This range is fine for most video signals whose nominal signal amplitude is 1V. The most negative input level (the sync tip for composite video) should be maintained at 0.3V or above for best operation.

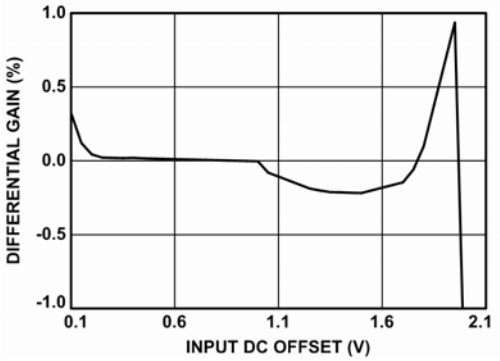


FIGURE 48. DIFFERENTIAL GAIN RESPONSE

In a DC-coupled application, it is the system designer's responsibility to ensure that the video signal is always in the optimum range.

When AC coupling, the ISL59530's DC restore function automatically adjusts the DC level so that the most negative portion of the video is always equal to V_{REF}.

A discussion of the benefits of the DC-restored system begins by understanding the block diagram of a typical DC-restore circuit (Figure 49). It consists of 4 sections: an AC coupling (DC blocking) capacitor at the input, an opamp, a FET switch, and a current source. In the absence of an input signal, R_{TERM} pulls the input node to ground. The 2µA current source slowly drains the input capacitor of charge, slowly lowering V_{OUT}. However when V_{OUT} goes below V_{REF}, Q1 turns on, sourcing current into the capacitor until V_{OUT} is equal to V_{REF}, at which point Q1 will turn off. So with no V_{IN} signal, the voltage at the noninverting input of the opamp will settle to approximately V_{REF}, with Q1 sourcing the same 2µA as the current source.

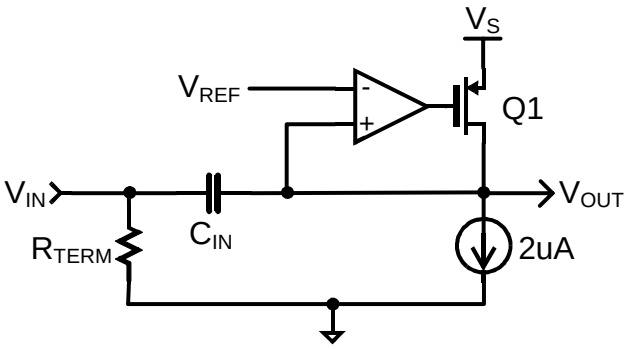


FIGURE 49. DC RESTORE BLOCK DIAGRAM

When a video signal is applied to V_{IN}, the most negative signal will be the sync tip. If the sync tip goes below V_{REF}, Q1 will turn on and quickly source enough current into C_{IN} so that the sync tip is forced to be equal to V_{REF}. After the sync tip, the video jumps up by 300mV or more, so V_{OUT} becomes >> V_{REF}, so Q1 will not turn on for the rest of the video line. However the 2µA current source continues to slowly discharge C_{IN}, so that by the end of the video line, the next sync tip will again be slightly below V_{REF}, forcing Q1 to source some current into C1 to make $V_{OUT} = V_{REF}$ during the sync tip.

This is how the video is “DC-restored” after being AC coupled into the ISL59530. The sync tip voltage will be equal to V_{REF}, on the right side of C_{IN}, regardless of the DC level of the video on the left side of C_{IN}. Due to various sources of offset in the actual clamp function, the actual sync tip level is typically about 75mV higher than V_{REF} (for V_{REF} = 0.5V).

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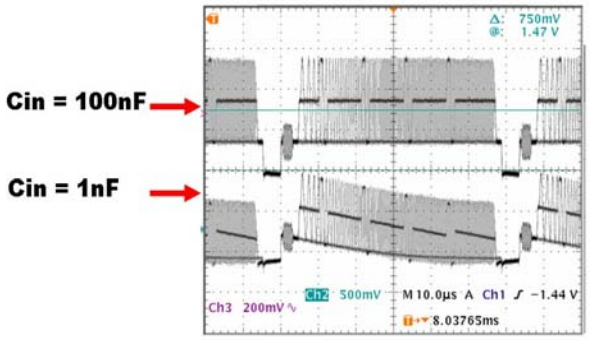


FIGURE 50. DC RESTORE VIDEO WAVEFORMS

It is important to choose the correct value for C_{IN}. Too small a value will generate too much droop, and the image will be visibly darker on the right than on the left. A C_{IN} value that is too large may cause the clamp to fail to converge. The droop rate (dV/dt) is $i_{PULLDOWN}/C_{IN}$ volts/second. In general, the droop voltage should be limited to <1 IRE over a period of one line of video; so for 1 IRE = 7mV, I_B = 10µA maximum, and an NTSC waveform we will set C_{IN} > 10µA*60µs/7mV = 0.086µF. Figure 50 shows the result of C_{IN} = 0.1µF delivering acceptable droop and C_{IN} = 0.001µF producing excessive droop

When the clamp function is disabled in the CONTROL register (Clamp = 0) to allow DC-coupled operation, the I_{CLAMP} current sinks/sources are disabled and the input passes through the DC Restore block unaffected. In this application V_{REF} may be tied to GND.

Overlay Operation

The ISL59530 features an overlay feature, that allows an external video signal or DC level to be inserted in place of that output channel’s video. When the $OVER_N$ signal is taken high, the output signal on the OUT_N pin is replaced with the signal on the $VOVER_N$ pin.

There are several ways the overlay feature can be used. Toggling the $OVER_N$ signal at the frame rate or slower will replace the video frame(s) on the OUT_N pin with the video supplied on the $VOVER_N$ pin.

Another option (for OSD displays, for example), is to put a DC level on the $VOVER_N$ line and toggle the $OVER_N$ signal at the pixel rate to create a monocolor image “overlaid” on channel N’s output signal.

Finally, by enabling the $OVER_N$ signal for some portion of each line over a certain amount of lines, a picture-in-picture function can be constructed.

It’s important to note that the overlay inputs do not have the DC Restore function previously described - the overlay signal is DC coupled into the output. It is the system designer’s responsibility to ensure that the video levels are in the ISL59530’s linear region and matching the output channel’s offset and amplitude. One easy way to do this is to run the video to be overlaid through one of the ISL59530’s unused channels and then into the $VOVER_N$ input.

The $OVER_N$ pins all have weak pulldowns, so if they are unused, they can either be left unconnected or tied to GND.

Power Dissipation and Thermal Resistance

With a large number of switches, it is possible to exceed the 150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the crosspoint switch in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature = 125°C
- T_{AMAX} = Maximum ambient temperature = 85°C
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

Where:

- V_S = Supply voltage = 5V
- I_{SMAX} = Maximum quiescent supply current = 360mA
- V_{OUT} = Maximum output voltage of the application = 2V
- R_{LOAD} = Load resistance tied to ground = 150
- n = 1 to 16 channels

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} = 2.44W$$

The required θ_{JA} to dissipate 2.44W is:

$$\Theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{PD_{MAX}} = 16.4(°C/W)$$

Table 8 shows θ_{JA} thermal resistance results with a Wakefield heatsink and without heatsink and various airflow. At the thermal resistance equation shows, the required thermal resistance depends on the maximum ambient temperature.

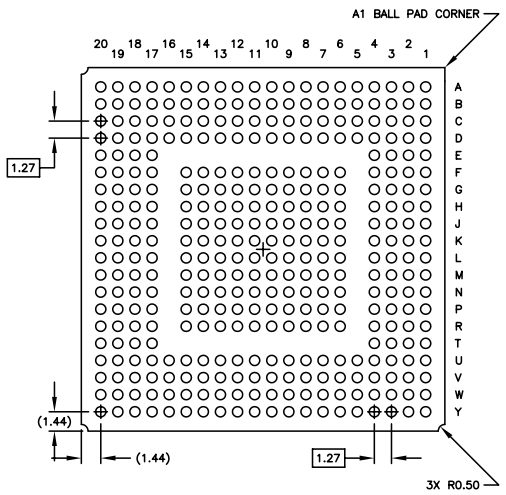
TABLE 8. θ_{JA} THERMAL RESISTANCE [°C/W]

Airflow [LFM]	0	250	500	750
No Heatsink	18	14.3	13.0	12.6
Wakefield 658-25AB Heatsink	16.0	7.0	6.0	4.7

356 Ld PBGA Package

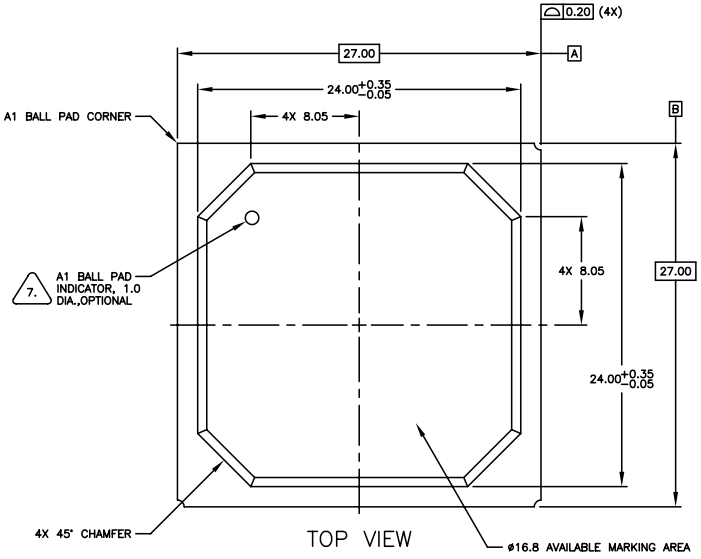
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.27mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 20 X 20.
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 400.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. A1 BALL PAD CORNER I.D. FOR PLATE MOLD: TO BE MARKED BY INK. AUTO MOLD: DIMPLE TO BE FORMED BY MOLD CAP.
8. REFERENCE SPECIFICATIONS:
   A. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS–034/A VARIATION BAL–2.

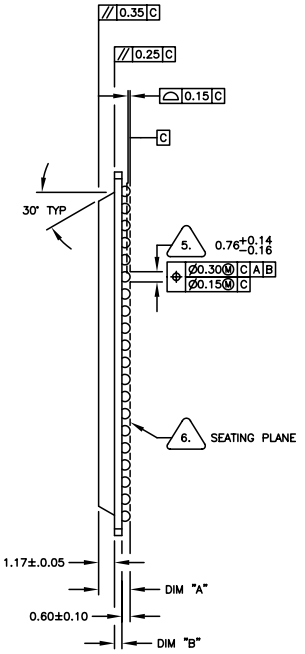


BOTTOM VIEW

356 SOLDER BALLS



TOP VIEW



SIDE VIEW

Drawing #: V356.27x27	PACKAGE OUTLINE DRAWING– 356 PBGA 27 x 27 mm x 1.17 mm MOLD CAP, 1.27 mm PITCH SUBSTRATE
Rev: 0	
Date: 2/28/06	
Units: mm	

4	2.38±0.21	0.61±0.06	STANDARD
NO. LAYERS	DIM "A"	DIM "B"	NOTES
PBGA THICKNESS SCHEDULE			