Data Sheet December 22, 2006 FN6164.0

10-Bit Video Analog Front End (AFE) with Measurement and Auto-Adjust Features

The ISL51002 3-channel, 10-bit Analog Front End (AFE) contains all the functionality needed to digitize analog YPbPr video from HDTV tuners, settop boxes, SD and HD DVDs, as well as RGB graphics signals from personal computers and workstations. The fourth generation analog design delivers 10-bit performance and a 165MSPS maximum conversion rate supporting resolutions up to 1080p/UXGA at 60Hz. The front end's programmable input bandwidth ensures sharp, low noise images at all resolutions.

To accelerate and simplify mode detection, the ISL51002 integrates a sophisticated set of measurement tools that fully characterizes the video signal and timing, offloading the host microcontroller. Automatic Black Level Compensation (ABLC™) eliminates part-to-part offset variation, ensuring perfect black level performance in every application.

The ISL51002's Digital PLL generates a pixel clock from the analog source's HSYNC or SOG (Sync-On-Green) signals. Pixel clock output frequencies range from 10MHz to 165MHz with sampling clock jitter of 250ps peak to peak.

Applications

- Flat Panel TVs
- Front/Rear Projection TVs
- PC LCD Monitors and Projectors
- High Quality Scan Converters
- Video/Graphics Processing

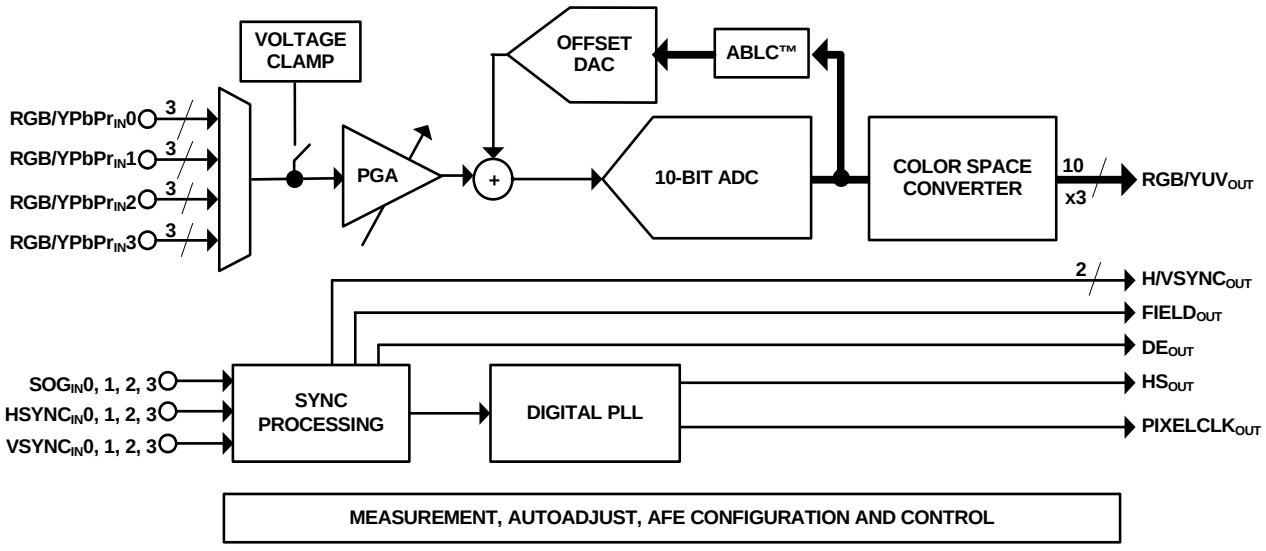
Features

- Automatic sampling phase adjustment
- 10-bit triple Analog to Digital Converters with oversampling up to 8x in video modes
- 165MSPS maximum conversion rate (ISL51002CQZ-165)
- Robust, glitchless Macrovision®-compliant sync separator
- Analog VCR “Trick Mode” support
- ABLC™ for perfect black level performance
- 4 channel input multiplexer
- Precision sync timing measurement
- RGB to YUV color space converter
- Low PLL clock jitter (250ps p-p)
- Programmable input bandwidth (10MHz to 450MHz)
- 64 interpixel sampling positions
- ±6dB gain adjustment rate
- Pb-free plus anneal available (RoHS compliant)

Related Literature

Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”.

Simplified Block Diagram

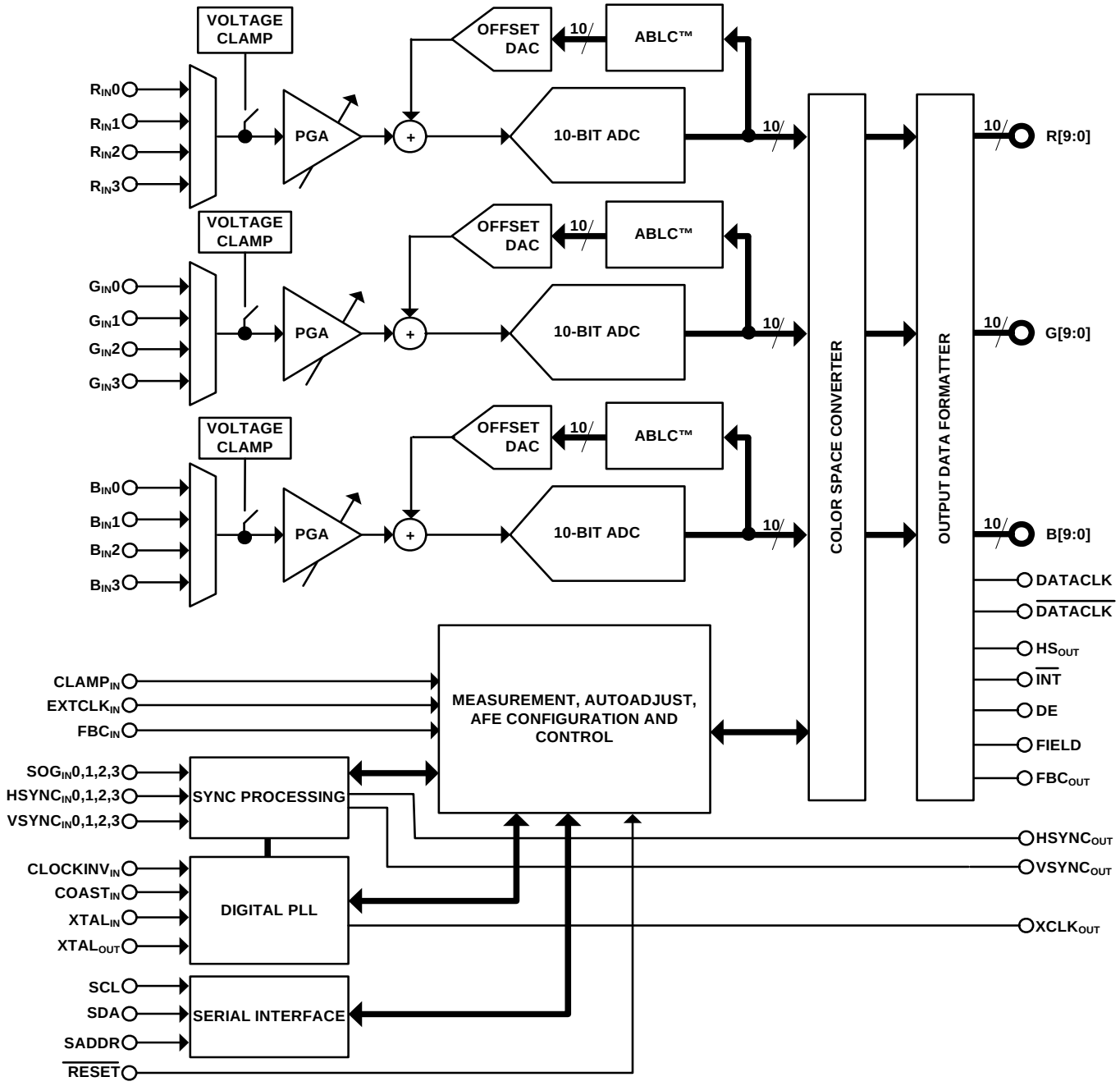


Ordering Information

PART NUMBER/PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG #
ISL51002CQZ-110 (Note)	0 to +70	128 Ld MQFP (Pb-free)	MDP0055
ISL51002CQZ-150 (Note)	0 to +70	128 Ld MQFP (Pb-free)	MDP0055
ISL51002CQZ-165 (Note)	0 to +70	128 Ld MQFP (Pb-free)	MDP0055
ISL51002EVALZ	Evaluation Platform		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Absolute Maximum Ratings

3.3V Supply Voltage ($V_{A3.3}$, $V_{D3.3}$, $VPLL_{A3.3}$) 4.6V
1.8V Supply Voltage ($V_{A1.8}$, $V_{D1.8}$, $VADC_{D1.8}$). 2.5V
Voltage on any Input Pin . . . . . -0.5V to 6V
Output Current . . . . . ±20mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .3000V
Machine Model (Per EIAJ ED-4701 Method C-111). 300V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . .1000V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
MQFP Package	30	16

Maximum Power Dissipation. . . . . 1.2 W
Maximum Junction Temperature . . . . . +125°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC, PLCC, etc. Lead Tips Only)

Operating Conditions

Temperature Range . . . . . 0°C to +70°C
Supply Voltage Range . . . . . 3.3V ±10%, 1.8V ±10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Specifications apply for $V_{A3.3} = V_{D3.3} = V_{PLLA3.3} = 3.3V$, $V_{A1.8} = V_{D1.8} = V_{PLLD1.8} = V_{ADCD1.8} = 1.8V$, pixel rate = 110MHz for ISL51002-110, 150MHz for ISL51002-150, 165MHz for ISL51002-165, f_{XTAL} = 25MHz, and T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST LEVEL or NOTES	MIN	TYP	MAX	UNITS
FULL CHANNEL CHARACTERISTICS						
	Conversion Rate					
	ISL51002-110		10		110	MHz
	ISL51002-150		10		150	MHz
	ISL51002-165		10		165	MHz
	ADC Resolution		10			Bits
	Missing Codes	Guaranteed monotonic			None	
DNL (Full-Channel)	Differential Non-Linearity					
	ISL51002-110		-0.99	±0.5	+1.2	LSB
	ISL51002-150		-0.99	±0.7	+1.3	LSB
	ISL51002-165		-0.99	±0.8	+1.4	LSB
INL (Full-Channel)	Integral Non-Linearity					
	ISL51002-110			±1.9	±3.6	LSB
	ISL51002-150			±2.0	±3.8	LSB
	ISL51002-165			±2.6	±4.0	LSB
	Gain Adjustment Range			±6		dB
	Gain Adjustment Resolution			10		Bits
	Gain Matching Between Channels	Percent of full scale		±2		%
	Full Channel Offset Error, ABLC™ enabled	ADC LSBs, over time and temperature		±0.5	±3.0	LSB
	Offset Adjustment Range (ABLC™ enabled or disabled)	(see ABLC™ applications information section)		±50%		ADC Fullscale
ANALOG VIDEO INPUT CHARACTERISTICS (R_{IN}0-3, G_{IN}0-3, B_{IN}0-3)						
	Input Range		0.35	0.7	2.2	V_{P-P}
	Input Bias Current	DC restore clamp off		±0.01	±1	µA
	Input Capacitance			5		pF

Electrical Specifications

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SYMBOL	PARAMETER	TEST LEVEL or NOTES	MIN	TYP	MAX	UNITS
	Full Power Bandwidth	Programmable		10 to 450		MHz
SOG INPUT CHARACTERISTICS (SOG_{IN}0-3)						
	Sync Tip Clamp			600		mV
	SOG Pull Down			1		µA
V_{IH}/V_{IL}	Input Threshold Voltage (relative to bottom of sync tip)	Programmable - See Register Listing for Details		0 to 0.3		V
	Input Capacitance			5		pF
HSYNC INPUT CHARACTERISTICS ($HSYNC_{IN}$0-3)						
V_{IH}/V_{IL}	Input Threshold Voltage	Programmable - See Register Listing for Details		0.4 to 3.2		V
	Hysteresis	Centered around threshold voltage		240		mV
I	Input Leakage Current (Note 1)			±10		nA
C_{IN}	Input Capacitance			5		pF
DIGITAL INPUT CHARACTERISTICS (ALL DIGITAL INPUT PINS EXCEPT SCL, $VSYNC_{IN}$0-3)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I	Input Leakage Current (Note 1)	$\overline{RESET}$ has a 65kΩ pullup to $V_{D3.3}$		±10		nA
C_{IN}	Input Capacitance			5		pF
SCHMITT DIGITAL INPUT CHARACTERISTICS (SCL, $VSYNC_{IN}$0-3)						
V_T+	Low To High Threshold Voltage		1.45			V
V_T-	High To Low Threshold Voltage				0.95	V
I	Input Leakage Current (Note 1)			±10		nA
C_{IN}	Input Capacitance			5		pF
DIGITAL OUTPUT CHARACTERISTICS (ALL OUTPUT PINS EXCEPT $\overline{INT}$ AND SDA)						
V_{OH}	Output HIGH Voltage, I_O = 8mA		2.4			V
V_{OL}	Output LOW Voltage, I_O = -8mA				0.4	V
DIGITAL OUTPUT CHARACTERISTICS ($\overline{INT}$)						
V_{OL}	Output LOW Voltage, I_O = -8mA	Open-drain, with 65kΩ pull-up to $V_{D3.3}$			0.4	V
DIGITAL OUTPUT CHARACTERISTICS (SDA)						
V_{OL}	Output LOW Voltage, I_O = -4mA	Open-drain			0.4	V
POWER SUPPLY REQUIREMENTS						
$V_{A3.3}$	Analog Supply Voltage, 3.3V	Includes $VPLL_{A3.3}$	3.0	3.3	3.6	V
$V_{A1.8}$	Analog Supply Voltage, 1.8V		1.65	1.8	2.0	V
$V_{D3.3}$	Digital Supply Voltage, 3.3V		3.0	3.3	3.6	V
$V_{D1.8}$	Digital Supply Voltage, 1.8V	Includes $VADC_{D1.8}$, $VPLL_{D1.8}$	1.65	1.8	2.0	V
$I_{A3.3}$	Analog Supply Current, 3.3V (Note 1)			45	90	mA
$IPLL_{A3.3}$				14	25	mA

Electrical Specifications

Specifications apply for $V_{A3.3} = V_{D3.3} = V_{PLLA3.3} = 3.3V$, $V_{A1.8} = V_{D1.8} = V_{PLLD1.8} = V_{ADCD1.8} = 1.8V$, pixel rate = 110MHz for ISL51002-110, 150MHz for ISL51002-150, 165MHz for ISL51002-165, $f_{XTAL} = 25MHz$, and $T_A = +25°C$, unless otherwise specified. **(Continued)**

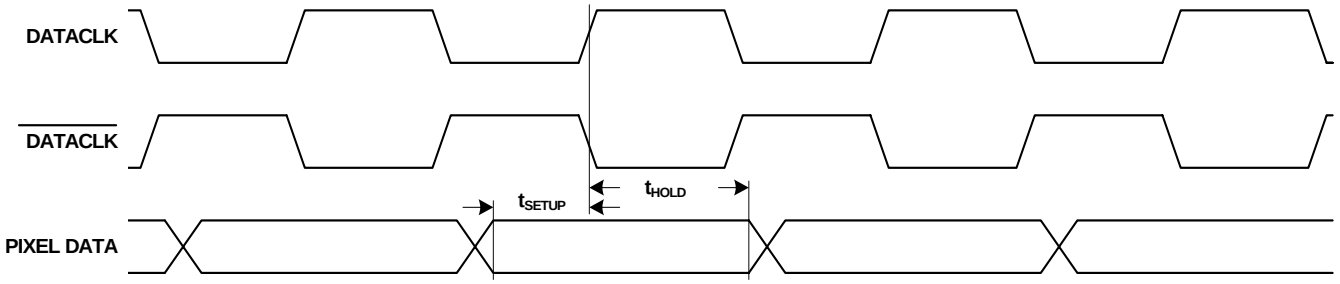
SYMBOL	PARAMETER	TEST LEVEL or NOTES	MIN	TYP	MAX	UNITS
$I_{A1.8}$	Analog Supply Current, 1.8V (Note 1)	Includes 1.8V ADC reference current draw		270	375	mA
$I_{D3.3}$	Digital Supply Current, 3.3V (Note 1)	Grayscale ramp input		30	60	mA
$I_{D1.8}$	Digital Supply Current, 1.8V (Note 1)	Grayscale ramp input		65	95	mA
$IADC_{D1.8}$				33	65	mA
$IPLL_{D1.8}$				1.8	10	mA
P_D	Total Power Dissipation	Grayscale ramp input		0.98	1.25	W
		Standby Mode		50	100	mW
AC TIMING CHARACTERISTICS						
	PLL Jitter (Note 2)			250	450	ps p-p
	Sampling Phase Steps	5.6° per step	64			
	Sampling Phase Tempco			±1		ps/°C
	Sampling Phase Differential Nonlinearity	Degrees out of +360°		±3		°
	Hsync Frequency Range		10		150	kHz
f_{XTAL}	Crystal Frequency Range		12	25	27	MHz
t_{SETUP}	Data Valid Before Rising Edge of Dataclk	20pF DATACLK load, 20pF DATA load	1.8			ns
t_{HOLD}	Data Valid After Rising Edge of Dataclk	20pF DATACLK load, 20pF DATA load	3.4			ns

NOTES:

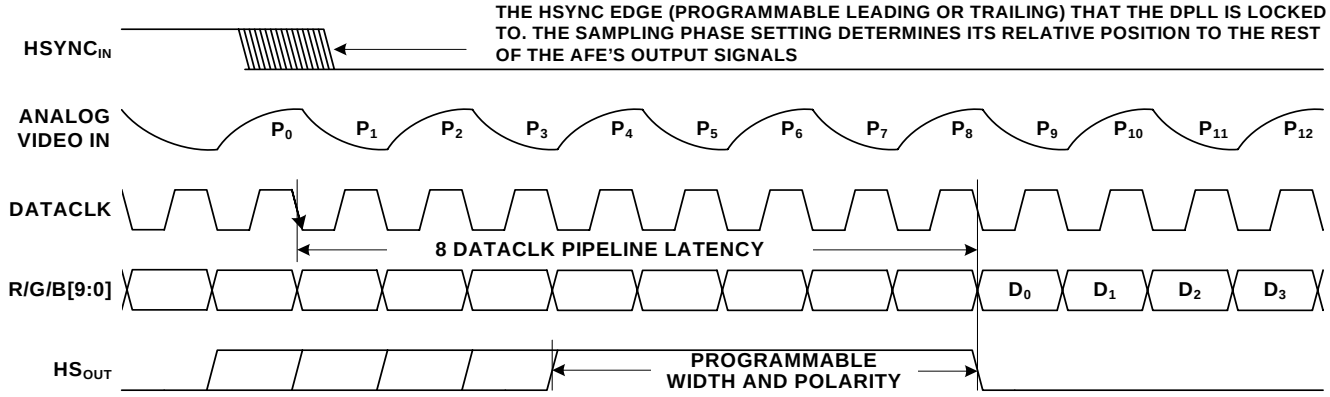
1. Supply current specified at max pixel rate (165MHz) with gray scale video applied.
2. Jitter tested at rated frequencies (165MHz, 150MHz, 110MHz) and at minimum frequency (10MHz).

Timing Diagrams

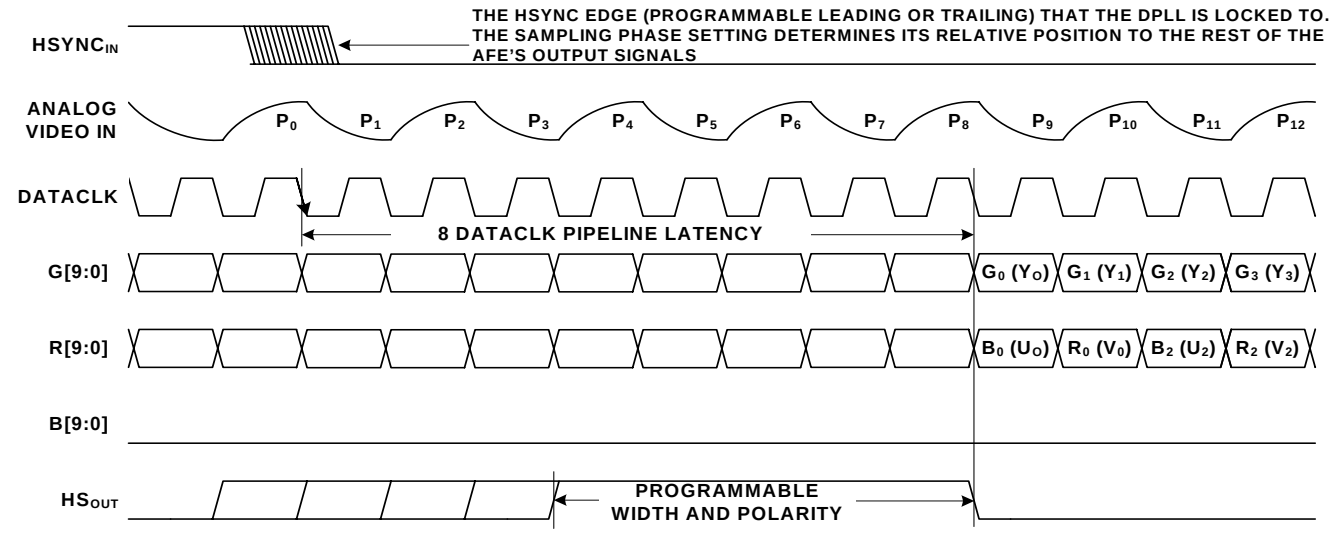
Data Output Setup and Hold Timing



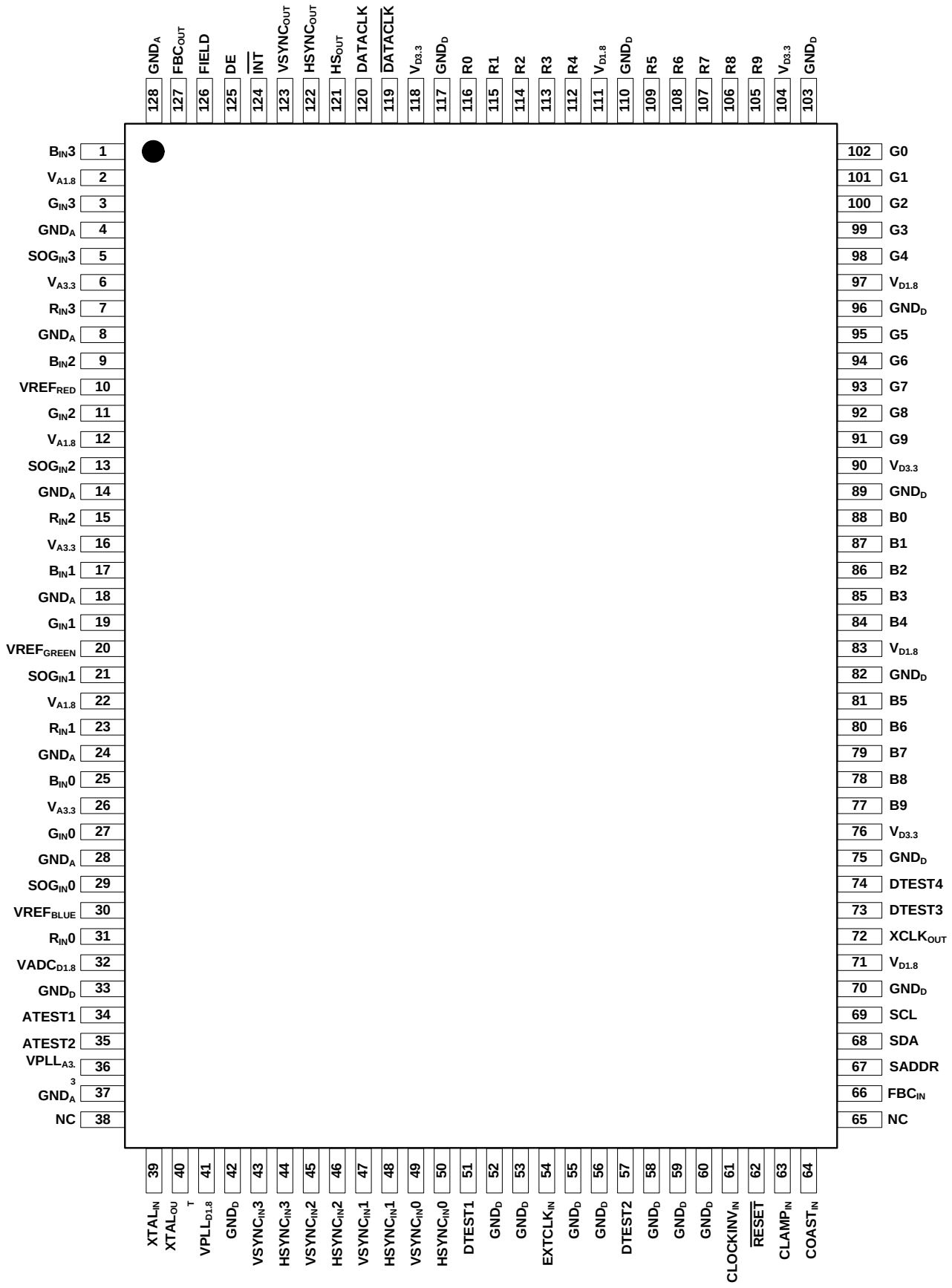
RGB Output Data Timing and Latency



YUV Output Data Timing and Latency



Pin Configuration (MQFP, ISL51002)



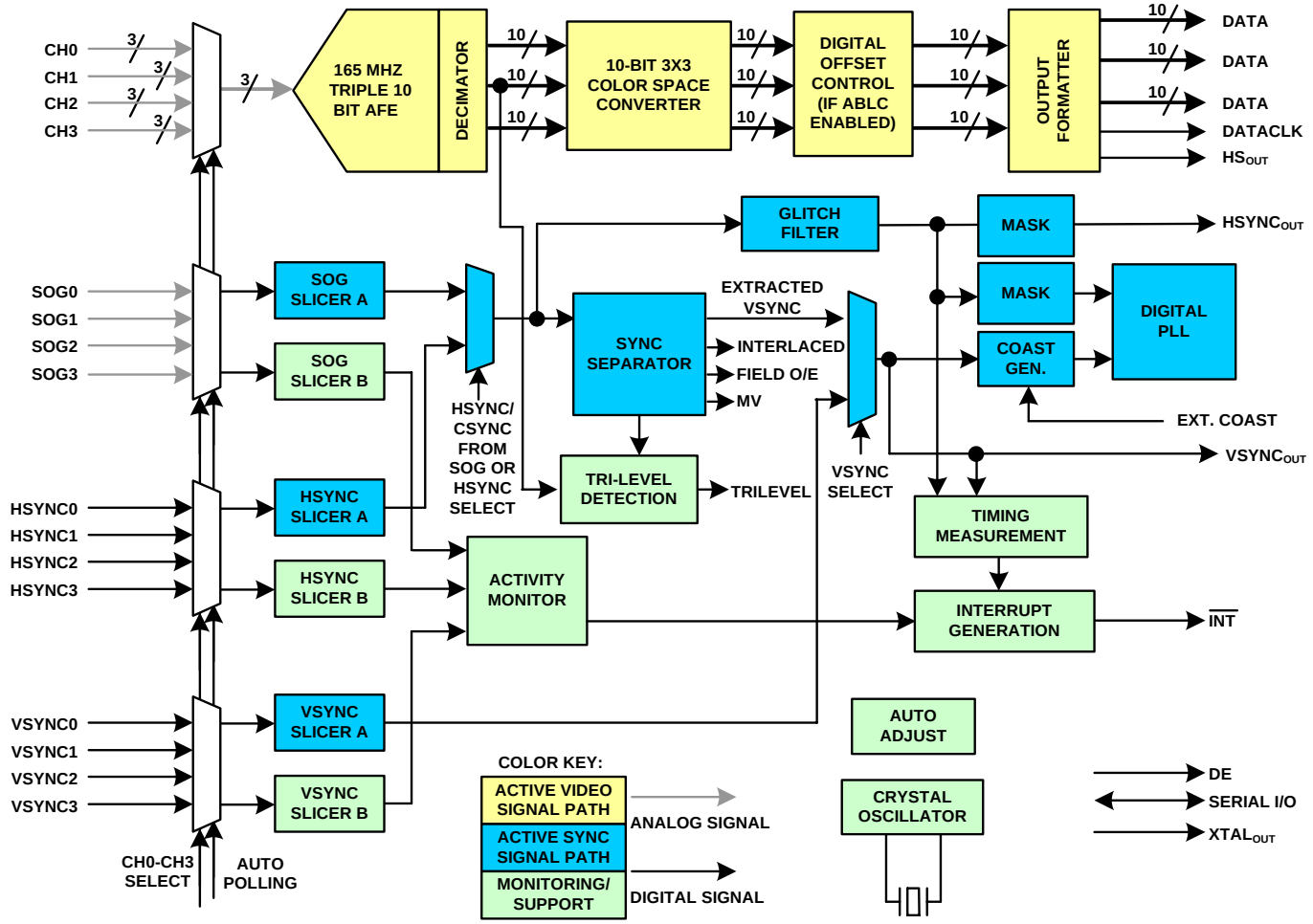
Pin Description

SYMBOL	DESCRIPTION
R_{IN}0, 1, 2, 3	Analog inputs. Red channels. AC couple through 0.1µF.
G_{IN}0, 1, 2, 3	Analog inputs. Green channels. AC couple through 0.1µF.
B_{IN}0, 1, 2, 3	Analog inputs. Blue channels. AC couple through 0.1µF.
$VREF_{RED}$, $VREF_{GREEN}$, $VREF_{BLUE}$	Analog inputs. Reference voltage for ADCs. Tie to 1.8V reference voltage ($V_{A1.8}$ is acceptable if low noise). Decouple with 0.1µF capacitor to GND_A.
SOG_{IN}0, 1, 2, 3	Analog inputs. Sync on Green. Connect to corresponding Green channel video source through a 0.01µF capacitor in series with a 500Ω resistor.
$HSYNC_{IN}$0, 1, 2, 3	Digital *high impedance* 3.3V inputs with 240mV hysteresis. Connect to corresponding channel's HSYNC source. For 5V signals divide input with a 1k/1.9k divider. Place the divider as close as possible to the device pin. Place a 50pFcapacitor in parallel with the 1k resistor to reduce the filtering effect of the divider.
$VSYNC_{IN}$0, 1, 2, 3	Digital *high impedance* 3.3V inputs with 240mV hysteresis. Connect to corresponding channel's VSYNC source. For 5V signals divide input with a 1k/1.9k divider. Place the divider as close as possible to the device pin. Place a 50pF capacitor in parallel with the 1k resistor to reduce the filtering effect of the divider.
$COAST_{IN}$	Digital 3.3V input. When this input is high and external COAST is selected, the PLL will coast, ignoring all transistions on the active channel's HSYNC/SOG.
$CLAMP_{IN}$	Digital 3.3V input.When this input is high and external CLAMP is selected, connects the selected channels inputs to the clamp DAC.
$CLOCKINV_{IN}$	Digital 3.3V input. When high, changes the pixel sampling phase by +180°. Toggle at frame rate during VSYNC to allow 2x undersampling to sample odd and even pixels on sequential frames. Tie to D_{GND} if unused.
FBC_{IN}	Digital 3.3V input.Connect to the Fast Blank signal of a SCART connector.
FBC_{OUT}	3.3V digital output. A delayed version of the FBC_{IN} signal, aligned with the digital pixel data.
RESET	Digital 3.3V input, active low, 70kΩ pullup to V_D. Take low for at least 1µs and then high again to reset the ISL51002. This pin is not necessary for normal use and may be tied directly to the V_D supply.
$XTAL_{IN}$	Analog input. Connect to external 12MHz to 27MHz crystal and load capacitor (see crystal spec for recommended loading). Typical oscillation amplitude is $1.0V_{P-P}$ centered around 0.5V.
$XTAL_{OUT}$	Analog output. Connect to external 12MHz to 27MHz crystal and load capacitor (see crystal spec for recommended loading). Typical oscillation amplitude is $1.0V_{P-P}$ centered around 0.5V.
$XCLK_{OUT}$	3.3V digital output. Buffered crystal clock output at f_{XTAL} or $f_{XTAL}/2$. May be used as system clock for other system components.
SADDR	Digital 3.3V input. Address = 0x98 (1001100x) when tied low. Address = 0 x 9A (1001101x) when tied high.
SCL	Digital input, 5V tolerant, 500mV hysteresis. Serial data clock for 2-wire interface.
SDA	Bidirectional Digital I/O, open drain, 5V tolerant. Serial data I/O for 2-wire interface.
$EXTCLK_{IN}$	Digital 3.3V input. External clock input for AFE.
R[9:0]	3.3V digital output. 10-bit Red channel pixel data.
G[9:0]	3.3V digital output. 10-bit Green channel pixel data.
B[9:0]	3.3V digital output. 10-bit Blue channel pixel data.
DATACLK	3.3V digital output. Data (pixel) clock output.
DATACLK	3.3V digital output. Inverse of DATACLK.
HS_{OUT}	3.3V digital output. HSYNC output aligned with pixel data. Use this output to frame the digital output data. This output is always purely horizontal sync (without any composite sync signals)
$HSYNC_{OUT}$	3.3V digital output. Buffered HSYNC (or SOG or CSYNC) output. This is typically used for measuring HSYNC period. This output will pass composite sync signals and Macrovision signals if present on $HSYNC_{IN}$ or SOG_{IN}.
$VSYNC_{OUT}$	3.3V digital output. Buffered VSYNC output. For composite sync signals, this output will be asserted for the duration of the disruption of the normal HSYNC pattern. This is typically used for measuring VSYNC period.

Pin Description

SYMBOL	DESCRIPTION
$\overline{INT}$	Digital output, open drain, 5V tolerant. Interrupt output indicating mode change or command execution status. Pull high with a 4.7k resistor.
DE	3.3V digital output. High when there is valid video data, low during horizontal and vertical blanking periods.
FIELD	3.3V digital output. For interlaced video, this output will changes states to indicate whether current field is even or odd. Polarity is determined by configuration register.
$V_{A3.3}$	Power supply for the analog section. Connect to a 3.3V supply and bypass each pin to GND_A with 0.1µF.
$V_{A1.8}$	Power supply for the analog section. Connect to a 1.8V supply and bypass each pin to GND_A with 0.1µF.
$VPLL_{A3.3}$	Power supply for the analog PLL section. Connect to a 3.3V supply and bypass to GND_A with 0.1µF.
GND_A	Ground return for $V_{A3.3}$, $V_{A1.8}$, and $VPLL_{A1.8}$.
$V_{D3.3}$	Power supply for all digital I/Os. Connect to a 3.3V supply and bypass each pin to GND_D with 0.1µF.
$V_{D1.8}$	Power supply for digital core logic. Connect to a 1.8V supply and bypass each pin to GND_D with 0.1µF.
$VADC_{D1.8}$	Power supply for the digital ADC section. Connect to a 1.8V supply and bypass to GND_D with 0.1µF.
$VPLL_{D1.8}$	Power supply for the digital PLL section. Connect to a 1.8V supply and bypass to GND_D with 0.1µF.
GND_D	Ground return for $V_{D3.3}$, $V_{D1.8}$, $VADC_{D1.8}$, and $VPLL_{D1.8}$.
ATEST1, 2	For production use only. Tie to GND_A.
DTEST1, 2, 3, 4	For production use only. Tie to GND_D.
NC	Reserved. Do not connect anything to these pins.

Sync Flow



Register Listing

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
STATUS AND INTERRUPT REGISTERS				
0x00	Device ID and revision, (read only, 0x21)	3:0	Device Revision	0x1 = second revision silicon
		7:4	Device ID	0x2 = ISL51002
0x01	Selected Input Channel Characteristics, (read only)	1:0	SYNC Type	00: Automatic Sync Selection logic could not find good sync on H, V, or SOG (Automatic Sync mode only) 01: SYNC on HSYNC/VSYNC 10: CSYNC on HSYNC 11: CSYNC on Green Channel (SOG)
		2	HSYNC Polarity	0: HSYNC Active High 1: HSYNC Active Low
		3	VSYNC Polarity	0: VSYNC Active High 1: VSYNC Active Low
		4	Tri-level Sync	0: Bi-level SOG (if SOG is active) 1: Tri-level SOG
		5	Interlaced (Only for CSYNC)	0: Non-interlaced or progressive signal 1: Interlaced signal
		6	Macrovision	0: No Macrovision detected 1: Macrovision encoding detected
		7	PLL Locked	0: PLL unlocked 1: PLL locked to incoming HSYNC
0x02	CH0 and CH1 Activity Status, (read only)	0	HSYNC0 Activity	0: HSYNC0 Inactive 1: HSYNC0 Active – There is a periodic signal with frequency >1kHz and consistent low/high times on this input
		1	VSYNC0 Activity	0: VSYNC0 Inactive 1: VSYNC0 Active – There is a periodic signal with frequency >20Hz and consistent low/high times on this input
		3:2	SOG0 Activity	00: SOG0 Inactive – No transitions detected at the SOG Slicer output. 01: SOG0 Active – Non-periodic transitions detected at the SOG Slicer output – possibly valid SOG with a bad slicer threshold, or simply video with no valid SOG. 10: SOG0 Periodic – There is a periodic signal with frequency >1kHz and consistent low/high times on this input. This is most likely a valid SOG signal.
		4	HSYNC1 Activity	See HSYNC0 Activity description
		5	VSYNC1 Activity	See VSYNC0 Activity description
		7:6	SOG1 Activity	See SOG0 Activity description
0x03	CH2 and CH3 Activity Status, (read only)	0	HSYNC2 Activity	See HSYNC0 Activity description
		1	VSYNC2 Activity	See VSYNC0 Activity description
		3:2	SOG2 Activity	See SOG0 Activity description
		4	HSYNC3 Activity	See HSYNC0 Activity description
		5	VSYNC3 Activity	See VSYNC0 Activity description
		7:6	SOG3 Activity	See SOG0 Activity description

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x04	Interrupt Status, Write a 1 to each bit to clear it, 0xFF to clear all.	0	CH0 Sync Changed	0: No change 1: CH0 activity or polarity changed
		1	CH1 Sync Changed	0: No change 1: CH1 activity or polarity changed
		2	CH2 Sync Changed	0: No change 1: CH2 activity or polarity changed
		3	CH3 Sync Changed	0: No change 1: CH3 activity or polarity changed
		4	Selected Input Channel Disrupted	0: No change 1: Currently selected Input Channel's HSYNC or VSYNC signal has changed (fast notification of a mode change)
		5	Selected Input Channel Changed	0: No change 1: Currently selected Input Channel's HSYNC or VSYNC period or pulse width has settled to a new value and can be measured
		6	VSYNC INT	0: Default state 1: VSYNC occurred
		7	PADJ INT	0: Default state 1: Phase Adjustment function completed.
0x05	Interrupt Mask Register, (0xFF)	0	CH0 Mask	0: Generate interrupt if CH0 sync activity, polarity, period, or pulse width changes 1: Mask CH0 interrupt
		1	CH1 Mask	0: Generate interrupt if CH1 sync activity, polarity, period, or pulse width changes 1: Mask CH1 interrupt
		2	CH2 Mask	0: Generate interrupt if CH2 sync activity, polarity, period, or pulse width changes 1: Mask CH2 interrupt
		3	CH3 Mask	0: Generate interrupt if CH3 sync activity, polarity, period, or pulse width changes 1: Mask CH3 interrupt
		4	Input Disrupted Mask	0: Generate interrupt if selected Input Channel's sync inputs are disrupted 1: Mask Input Channel interrupt
		5	Input Changed Mask	0: Generate interrupt after selected Input Channel period or pulse width settles to new value 1: Mask Input Channel interrupt
		6	VSYNC INT Mask	0: Generate interrupt every VSYNC 1: Mask VSYNC Interrupt
		7	PADJ INT Mask	0: Generate interrupt upon phase adjustment block request completion 1: Mask Phase adjustment interrupt

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
CONFIGURATION REGISTERS				
0x10	Input Configuration, (0x00)	1:0	Input Channel Select	Sets video muxes as well as HSYNC, VSYNC, and SOG input muxes. 0: CH0 1: CH1 2: CH2 (single-ended mode only) 3: CH3 (single-ended mode only)
		2	Differential Mode Enable	0: Single-Ended Mode 1: Differential Mode
		3	DC Coupled Input Enable	0: AC-coupled Inputs 1: DC-coupled Inputs
		4	RGB YUV	0: RGB inputs (Clamp DAC = 300mV for R, G, B, half scale analog shift for R, G, and B, base ABLC target code = 0x00 for R, G, and B) 1: YPbPr inputs (Clamp DAC = 600mV for R and B, 300mV for G, half scale analog shift for G channel only, base ABLC target code = 0x00 for G, = 0x80 for R and B)
		5	High Voltage Enable	0: Normal Input Range 1: Expanded 2.2V Input Range
		6	EXT Clamp SEL	0: Internal CLAMP generation 1: External CLAMP source
		7	EXT Clamp POL	0: Active high external CLAMP 1: Active low external CLAMP
0x11	Sync Source Selection, (0x00)	0	Sync Select	0: Automatic (HSYNC, VSYNC sources selected based on sync activity. Multiplexer settings chosen are displayed in the Input Characteristics register.) 1: Manual (bits 1and 2 determine HSYNC and VSYNC source)
		1	HSYNC Source	0: HSYNC input pin 1: SOG
		2	VSYNC Source	0: VSYNC input pin 1: Sync Separator output
0x12	Red Gain MSB,(0x55)	7:0	Red Gain MSB	Red channel gain, where: gain (V/V) = 0.5 + [9:0]/682 MSB/LSB 0x00 00: gain = 0.5 V/V (1.4VP-P input = full range of ADC) 0x55 00: gain = 1.0 V/V (0.7VP-P input = full range of ADC) 0xFF C0: gain = 2.0 V/V (0.35VP-P input = full range of ADC)
0x13	Red Gain LSB,(0x00)	5:0	N/A	
		7:6	Red Gain LSB	2 LSBs of 10-bit gain word
0x14	Green Gain MSB,(0x55)	7:0	Green Gain MSB	See Red Gain
0x15	Green Gain LSB,(0x00)	5:0	N/A	
		7:6	Green Gain LSB	See Red Gain
0x16	Blue Gain MSB,(0x55)	7:0	Blue Gain MSB	See Red Gain
0x17	Blue Gain LSB,(0x00)	5:0	N/A	
		7:6	Blue Gain LSB	See Red Gain
0x18	Red Offset MSB,(0x80)	7:0	Red Offset MSB	ABLC off: upper 8 bits to Red offset DAC ABLC enabled: Red digital offset 0x00 00 = min DAC value or -0x80 digital offset 0x80 00 = mid DAC value or 0x00 digital offset, 0xFF C0= max DAC value or +0x7F digital offset

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x19	Red Offset LSB,(0x00)	5:0	N/A	
		7:6	Red Offset LSB	2 LSBs of 10-bit offset word
0x1A	Green Offset MSB, (0x80)	7:0	Green Offset MSB	ABLC off: upper 8 bits to Green offset DAC ABLC enabled: Green digital offset (See Red Offset)
0x1B	Green Offset LSB, (0x00)	5:0	N/A	
		7:6	Green Offset LSB	See Red Offset
0x1C	Blue Offset MSB, (0x80)	7:0	Blue Offset MSB	ABLC off: upper 8 bits to Blue offset DAC ABLC enabled: Blue digital offset (See Red Offset)
0x1D	Blue Offset LSB, (0x00)	5:0	N/A	
		7:6	Blue Offset LSB	See Red Offset
0x1E	PLL Htotal MSB,(0x06)	5:0	PLL Htotal MSB	14-bit HTOTAL PLL updated on LSB write only.
0x1F	PLL Htotal LSB,(0x98)	7:0	PLL Htotal LSB	PLL updated on LSB write only. SXGA default
0x20	PLL Phase, (0x00)	5:0	PLL Sampling Phase	Used to control the phase of the ADC's sample point relative to the period of a pixel. Adjust to obtain optimum image quality. One step = 5.625° (1.56% of pixel period).
0x21	PLL Pre-coast, (0x04)	7:0	Pre-coast	Number of lines the PLL will coast prior to the start of VSYNC.
0x22	PLL Post-coast, (0x04)	7:0	Post-coast	Number of lines the PLL will coast after the end of VSYNC.
0x23	PLL Misc, (0x00)	0	PLL Lock Edge HSYNC	0: PLL locks to trailing edge of selected HSYNC (default) 1: PLL locks to leading edge of selected HSYNC
		1	CLKINV ENABLE	0: CLKINV input ignored 1: CLKINV input enabled
		2	Ext Coast SEL	0: Internal COAST generation 1: External COAST source
		3	Ext Coast POL	0: Active high external COAST 1: Active low external COAST
		4	EXT CLOCK	0: Internal pixel clock from DPLL 1: External pixel clock from EXTCLKin pin
0x24	DC Restore and ABLC starting pixel MSB, (0x00)	5:0	DC Restore and ABLC starting pixel (MSB)	Pixel after Raw HSYNC trailing edge to begin DC restore and ABLC. 14 bits.
0x25	DC Restore and ABLC starting pixel LSB, (0x02)	7:0	DC Restore and ABLC starting pixel (LSB)	
0x26	DC Restore Clamp Width, (0x10)	7:0	DC Restore clamp width	Only applies to DC restore clamp used for AC-coupled configurations. A value of 0x00 means the clamp DAC is never connected to the input.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x27	ABLC Configuration, (0x40)	0	ABLC Disable	0: ABLC on (default) - use 10-bit digital offset control. 0x000 = -0x200 LSB offset, 0x3FF = +0x1FF LSB offset, 0x200 = 0x000 LSB offset 1: ABLC off - use 10-bit offset DACs, bypass digital adder (add/subtract nothing, but keep same delay through channel)
		1	Offset DAC Range	0: ±1/2 ADC fullscale (1 LSB = 1 ADC LSBs) 1: ±1/4 ADC fullscale (1 LSB = 0.5 ADC LSBs)
		3:2	ABLC Pixel Width	Number of black pixels averaged every line for ABLC function 00: 16 pixels [default] 01: 32 pixels 10: 64 pixels 11: 128 pixels
		6:4	ABLC Bandwidth	ABLC Time constant (lines) = $2^{([5+6:4])}$ 000 = 32 lines 100 = 512 lines (default) 111 = 4096 lines
0x28	Output Format 1, (0x00)	0	Data Output Format	0: 4:4:4 (24/30-bit output) 1: 4:2:2 (16/20-bit output on G and R)
		1	4:2:2 Order	0: First pixel on R channel is U 1: First pixel on R channel is V
		2	4:2:2 Processing	0: U, V fitered (high quality) 1: Odd U, V pixels dropped (lower quality)
		3	8-bit Mode	0: All 10 bits of each channel active 1: 2 LSBs of each channel driven low (in 8-bit applications, keep the LSBs from switching and generating noise)
		5:4	Oversampling	00: Normal operation (1x sampling) 01:2x oversampling, 2 samples averaged at ADC output 10:4x oversampling, 4 samples averaged at ADC output 11:8x oversampling, 8 samples averaged at ADC output In Oversampling mode, the HTOTAL, DC Restore/ABLC Start, DC Restore Width, and ABLC width values are automatically multiplied by the oversampling ratio. The pixel clock is divided by the oversampling ratio when the data is decimated. Decimator is reset on trailing edge of HSYNC.
		6	RGB2YUV Color Space Conversion Enable	0: CSC Disabled 1: CSC Enabled Note: The data delay through the entire AFE is identical with CSC on and CSC off.

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x29	Output Format 2, (0x00)	0	DATACLK Polarity	0: Pixel data changes on falling edge (default) 1: Pixel data changes on rising edge
		1	FIELD output polarity	0: Odd = low, Even = high (default) 1: Odd = high, Even = low
		2	Macrovision	0: Digitize Macrovision encoded signals (default) 1: Blank AFE output for Macrovision encoded signals. If Macrovision is detected, AFE output is always 0x00 0x00 0x00 for RGB, or 0x00, 0x80, 0x80 for YUV.
		3	HSOUT Polarity	0: Active High (default) 1: Active Low
		4	HSOUT Lock Edge	0: HSOUT's leading edge is locked to selected HSYNCin's lockedge. Trailing edge moves forward in time as HSout width is increased (default). 1: HSOUT's trailing edge is locked to selected HSYNCin's lockedge. Leading edge moves backward in time as HSout width is increased.
		5	XTALCLKOUT Frequency	0: XTALCLKOUT= $f_{CRYSTAL}$ (default) 1: XTALCLKOUT= $f_{CRYSTAL}/2$
		6	Enable XTALCLKOUT	0 = XTALCLKOUT is logic low (default) 1 = XTALCLKOUT enabled
0x2A	HSOUT Width, (0x10)	7:0	HSOUT Width	HSOUT Width in pixels, 0x00 to 0xFF. HSOUT Lock Edge determines whether leading or trailing edge is locked to HSYNCin
0x2B	Output Signal Disable, (0xFF) Note: All digital outputs are tristated by default to ease multiplexing with other AFEs	0	Tri-state Red	0 = Outputs enabled 1 = Outputs in tristate
		1	Tri-state Green	0 = Outputs enabled 1 = Outputs in tristate
		2	Tri-state Blue	0 = Outputs enabled 1 = Outputs in tristate
		3	Tri-state SYNC	0 = HSout, HSYNCout, VSYNCout enabled 1 = Outputs in tristate
		4	Tri-state DATACLK	0 = Output enabled 1 = Output in tristate
		5	Tri-state DATACLKb	0 = Output enabled 1 = Output in tristate
		6	Tri-state DE	0 = Output enabled 1 = Output in tristate
		7	Tri-state Field	0 = Output enabled 1 = Output in tristate
0x2C	Power Control, (0x00)	0	Red Power Down	0 = Red ADC operational (default) 1 = Red ADC powered down
		1	Green Power Down	0 = Green ADC operational (default) 1 = Green ADC powered down
		2	Blue Power Down	0 = Blue ADC operational (default) 1 = Blue ADC powered down
		3	PLL Power Down	0 = PLL operational (default) 1 = PLL powered down

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x2D	XTAL CLOCK FREQ, (0x19)	4:0	Crystal Clock Frequency	Crystal clock frequency in MHz (decimal). 0x00: Test Mode, Do not use. 0x01 - 0x0A: 10MHz, APLL DIV = 35 (0x23) 0x0B: 11MHz, APLL DIV = 32 0x0C: 12MHz, APLL DIV = 30 0x0D: 13MHz, APLL DIV = 27 0x0E: 14MHz, APLL DIV = 25 0x0F: 15MHz, APLL DIV = 24 0x10: 16MHz, APLL DIV = 22 0x11: 17MHz, APLL DIV = 21 0x12: 18MHz, APLL DIV = 20 0x13: 19MHz, APLL DIV = 19 0x14: 20MHz, APLL DIV = 18 0x15: 21MHz, APLL DIV = 17 0x16: 22MHz, APLL DIV = 16 0x17: 23MHz, APLL DIV = 16 0x18: 24MHz, APLL DIV = 15 0x19: 25MHz, APLL DIV = 14 0x1A: 26MHz, APLL DIV = 14 0x1B: 27MHz, APLL DIV = 13 0x1C: 28MHz, APLL DIV = 13 0x1D: 29MHz, APLL DIV = 13 0x1E: 30MHz, APLL DIV = 12 0x1F: 31MHz, APLL DIV = 12
0x2E	AFE Bandwidth, (0x0E)	3:0	AFE BW	-3dB point for AFE lowpass filter 0: 9MHz 1: 10MHz 2: 11MHz 3: 12MHz 4: 14MHz 5: 17MHz 6: 21 MHz 7: 24MHz 8: 30MHz 9: 38MHz A: 50MHz B: 75MHz C: 83MHz D: 105MHz E: 149MHz (default) F: 450MHz
0x2F	HSYNC Slicer Thresholds, (0x44) All values referred to voltage at HSYNC input pin, 300mV hysteresis	3:0	Selected HSYNC Threshold	HSYNC slicer threshold for selected input channel (only 3 bits used, lowest bit is ignored): 0000 = lowest (0.4V) 0100 = default (1.15V) 1111 = highest (3.2V)
		7:4	Unselected HSYNC Threshold	HSYNC threshold for monitoring unselected inputs. See Selected HSYNC Threshold for values.
0x30	SOG Slicer Thresholds, (0x66)	3:0	SOG Threshold	SOG slicer threshold: 0000 = lowest (0mV) 0110 = default (120mV) 1111 = highest (300mV)

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x31	HSYNC/SOG Config, (0x04)	3:0	Glitch Filter Width	0: 16 crystal clocks 1: 17 crystal clocks 2: 1 crystal clocks 3: 2 crystal clocks 4: 3 crystal clocks (default) 5: 4 crystal clocks 6: 5 crystal clocks 7: 6 crystal clocks 8: 7 crystal clocks 9: 8 crystal clocks 10: 9 crystal clocks 11: 10 crystal clocks 12: 11crystal clocks 13: 12 crystal clocks 14: 13 crystal clocks 15: 14 crystal clocks
		4	Sync Glitch Filter Disable	0: glitch filter enabled 1: glitch filter disabled
		5	SOG Hyst Disable	0: 40mV hysteresis enabled 1: 40mV hysteresis disabled
		6	SOG LPF Disable	0: 14MHz SOG Low Pass Filter Enabled 1: 14MHz SOG Low Pass Filter Disabled
0x32	Sync Polling Control, (0x00)	0	CH0 Polling	0: Enable 1: Disable
		1	CH1 Polling	0: Enable 1: Disable
		2	CH2 Polling	0: Enable 1: Disable
		3	CH3 Polling	0: Enable 1: Disable
		4	CH0 Connector Type	0: RGB DB15 (poll for HSYNC, CSYNC, and SOG) 1: Component (poll for SOG only)
		5	CH1 Connector Type	0: RGB DB15 (poll for HSYNC, CSYNC, and SOG) 1: Component (poll for SOG only)
		6	CH2 Connector Type	0: RGB DB15 (poll for HSYNC, CSYNC, and SOG) 1: Component (poll for SOG only)
		7	CH3 Connector Type	0: RGB DB15 (poll for HSYNC, CSYNC, and SOG) 1: Component (poll for SOG only)
MEASUREMENT REGISTERS				
0x40	HSYNC Period MSB, (read only)	7:0	HSYNC Period MSB	These registers report a 16-bit value containing the number of crystal clocks inside a 16 consecutive HSYNC period window. This means the 16-bit number will reflect one HSYNC period with 1/16 LSB resolution - the last 4 -bits of the measurement will be fractional.
0x41	HSYNC Period LSB, (read only)	7:0	HSYNC Period LSB	
0x42	HSYNC Width MSB, (read only)	7:0	HSYNC Width MSB	These registers report a 16-bit value containing the number of crystal clocks inside 16 consecutive HSYNC pulses. This means the 16-bit number will reflect one HSYNC pulse width with 1/16 LSB resolution - the last 4 bits of the measurement will be fractional.
0x43	HSYNC Width LSB, (read only)	7:0	HSYNC Width LSB	

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x44	VSYNC Period MSB, (read only)	3:0	VSYNC Period MSB	These bit report a 12-bit value containing the width of one frame (= 2 fields for interlaced, = 1 field for progressive) of video. VSYNC period for measured channel = 256* VSYNC Period MSB + VSYNC Period LSB Units are either number of HSYNC periods or number of fCRYSTAL/512 periods, depending on setting of VSYNC Units register.
0x45	VSYNC Period LSB, (read only)	7:0	VSYNC Period LSB	
0x46	VSYNC Width, (read only)	6:0	VSYNC Width	This register reports a 7-bit value containing the width the VSYNC pulse. The value returned is for true VSYNC only: it does not include serrations, EQ pulses, Macrovision pulses, etc. Units are either number of HSYNC periods or number of fCRYSTAL/512 periods, depending on setting of VSYNC Units register.
0x47	DE Start MSB, (0x00)	1:0	DE Start MSB	10-bit value containing the number of pixel clocks between the trailing edge of HSout and the first valid pixel. SXGA default values.
0x48	DE Start LSB, (0xF6)	7:0	DE Start LSB	
0x49	DE Width MSB, (0x05)	3:0	DE Width MSB	12-bit value containing the number of visible image pixels. SXGA default values.
0x4A	DE Width LSB, (0x00)	7:0	DE Width LSB	
0x4B	Line Start MSB, (0x00)	1:0	Line Start MSB	10-bit value containing the number of lines between the trailing edge of VSYNCOUT and the first valid line. SXGA default values.
0x4C	Line Start LSB, (0x26)	7:0	Line Start LSB	
0x4D	Line Width MSB, (0x04)	3:0	Line Width MSB	12-bit value containing the number of visible lines. SXGA default values.
0x4E	Line Width LSB, (0x00)	7:0	Line Width LSB	
0x4F Measurement Configuration, (0x00)		0	VSYNC Units	0: VSYNC measurement reported in units of lines (HSYNC periods) 1: VSYNC measurement reported in units of 512 crystal clock periods
		1	VSYNC_Linecount_Mode	0: New method (Integer count of HSouts) 1: Old method (Time measurement with rounding errors)
AUTO ADJUST REGISTERS				
0x50	Phase ADJ CMD FN, (0x00)	2:0	PADJ Function	Note: A write to this register executes the command contained in the three LSBs of the word written. Commands: 000: Reserved 001: Reserved 010: Reserved 011: SetPhase 100: Set DE 101: Reserved 110: Reserved 111: Reserved
0x51	Phase ADJ STATUS, (read only)	7	PADJ Busy	0: Phase Adjustment function idle 1: Phase Adjustment in progress

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x52	Phase ADJ MASK V, (0x01)	2:0	PADJ Exclude v2	Vertical line mask: How many lines to exclude before the leading edge of vsync 000: 0 lines 001: 1 lines (default) 010: 2 lines 011: 4 lines 100: 6 lines 101: 8 lines 110: 10 lines 111: 12 lines
		3	N/A	
		6:4	PADJ Exclude v1	Choose how many lines to exclude after the leading edge of vsync (typically used to exclude VBI data) 000: 5 lines (default) 001: 18 lines 010: 19 lines (480i) 011: 20 lines (1080i) 100: 22 lines (576i) 101: 25 lines (720p) 110: 41 lines (480p/1080p) 111: 44 lines (576p)
0x53	Horizontal pixel mask 1, (0x01)	7:0	PADJ Exclude h1	If a value of 'N' is programmed in this register, 2*N pixels after the active edge of HSOUT will be excluded from data collection. Must be >0 for proper operation.
0x54	Horizontal pixel mask 2, (0x01)	7:0	PADJ Exclude h2	If a value of 'N' is programmed in this register, 2*N pixels before the active edge of HSOUT will be excluded from data collection. Must be >0 for proper operation.
0x55	Phase Adjust Command Options, (0x20)	0	PADJ Blue Disable	Enable/disable blue color for measurement 0: enable 1: disable
		1	PADJ Green Disable	Enable/disable green color for measurement 0: enable 1: disable
		2	PADJ Red Disable	Enable/disable red color for measurement 0: enable 1: disable
		3	PADJ Adjust Search Option	Search option for auto phase adjustment 0: best phase 1: worst phase
		4	PADJ Adjust Speed	This is a hidden bit for customers. It decides whether the search steps are 28 (fast) or 64 vsync intervals (slow). 0: 28 VSYNCs 1: 64 VSYNCs
		5	Update Phase on VSYNC	0: phase updated immediately 1: phase updated on VSYNC (default)
		6	PADJ Soft Reset	0: Normal operation 1: Reset all phase adjust state machines Take high then low to reset phase adjust block
		7	Reserved	Set to 0

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BITS	FUNCTION NAME	DESCRIPTION
0x56	Transition threshold, (0x0A)	7:0	PADJ Threshold	Threshold of transitions visible for capturing. These are the 8 MSBs of the 10-bit threshold word used for phase quality measurements. The actual 10-bit threshold used equals the value in this register times 4.
0x57	Phase Adjust Data 3, (read only)	7:0	Reserved	Reserved
0x58	Phase Adjust Data 2, (read only)	7:0	Reserved	Reserved
0x59	Phase Adjust Data 1, (read only)	7:0	Reserved	Reserved
0x5A	Phase Adjust Data 0, (read only)	7:0	Reserved	Reserved
0x60	AFE CTRL, (0x00)	0	Reserved	Set to 0
		1	700mV calibration	0: Normal operation 1: All three inputs connected to internal ~700mV reference voltage
		2	Coast Clamp Enable	0: DC restore clamping and ABLC suspended during Coast and Macrovision (default) 1: DC restore clamping and ABLC continue during Coast
		3	Reserved	Set to 0
		4	Blue Midscale	0: Half scale analog shift not added to Blue Channel (UV) 1: Half scale analog shift added to Blue Channel (YRGB)
		5	Green Midscale	0: Half scale analog shift not added to Green Channel (UV) 1: Half scale analog shift added to Green Channel (YRGB)
		6	Red Midscale	0: Half scale analog shift not added to Red Channel (UV) 1: Half scale analog shift added to Red Channel (YRGB)
		7	Midscale Override	0: Midscale determined by RGB/YUV bit in User Control section – settings in 0x60[6:4] are ignored (default). 1: Midscale determined by 0x60[6:4]
0x61	ADC CTRL, (0x00)	0	Dither Enable	0: Dither disabled (default) 1: Dither enabled
		1	Dither Amplitude	0: 16 LSBs (default) 1: 8 LSBs
		3:2	Dither Increment	00: Every Pixel (default) 01: Every HSYNC 10 and 11: Every VSYNC
		4	Dither Seed Reset	Set to 1 and then to 0 to reset

Technical Highlights

The ISL51002 provides all the features of traditional triple channel video AFEs, but adds several next-generation enhancements, bringing performance and ease of use to new levels.

DPLL

All video AFEs must phase lock to an HSYNC signal, supplied either directly or embedded in the video stream (Sync On Green). Historically this has been implemented as a traditional analog PLL. At SXGA and lower resolutions, an analog PLL solution has proven adequate, if somewhat troublesome (due to the need to adjust charge pump currents, VCO ranges and other parameters to find the optimum trade-off for a wide range of pixel rates).

As display resolutions and refresh rates have increased, however, the pixel period has shrunk. An XGA pixel at a 60Hz refresh rate has 15.4ns to change and settle to its new value. But at UXGA 75Hz, the pixel period is 4.9ns. Most consumer graphics cards (even the ones with “350MHz” DACs) spend most of that time slewing to the new pixel value. The pixel may settle to its final value with 1ns or less before it begins slewing to the next pixel. In many cases it rings and never settles at all. So precision, low-jitter sampling is a fundamental requirement at these speeds, and a difficult one for an analog PLL to meet.

The ISL51002's DPLL has less than 250ps of jitter, peak to peak, and independent of the pixel rate. The DPLL generates 64 phase steps per pixel (vs. the industry standard 32), for fine, accurate positioning of the sampling point. The crystal-locked NCO inside the DPLL completely eliminates drift due to charge pump leakage, so there is inherently no frequency or phase change across a line. An intelligent all-digital loop filter/controller eliminates the need for the user to have to program or change anything (except for the number of pixels) to lock over a range from interlaced video (10MHz or higher) to UXGA 60Hz (165MHz, with the ISL51002-165).

The DPLL eliminates much of the performance limitations and complexity associated with noise-free digitization of high speed signals.

Automatic Black Level Compensation (ABLC™) and Gain Control

Traditional video AFEs have an offset DAC prior to the ADC, to both correct for offsets on the incoming video signals and add/subtract an offset for user “brightness control” without sacrificing the 10-bit dynamic range of the ADC. This solution is adequate, but it places significant requirements on the system's firmware, which must execute a loop that detects the black portion of the signal and then servos the offset DACs until that offset is nulled (or produces the desired ADC output code). Once this has been accomplished, the offset (both the offset in the AFE and the offset of the video card generating the signal) is subject to drift - the temperature inside a monitor or projector can easily change +50°C between power-on/offset calibration on a cold morning and the temperature reached once the monitor and the monitor's environment have reached steady state. Offset can drift significantly over +50°C, reducing image quality and requiring that the user do a manual calibration once the monitor has warmed up.

In addition to drift, many AFEs exhibit interaction between the offset and gain controls. When the gain is changed, the magnitude of the offset is changed as well. This again increases the complexity of the firmware as it tries to optimize gain and offset settings for a given video input signal. Instead of adjusting just the offset, then the gain, both have to be adjusted interactively until the desired ADC output is reached.

The ISL51002 simplifies offset and gain adjustment and completely eliminates offset drift using its Automatic Black Level Compensation (ABLC™) function. ABLC™ monitors the black level and continuously adjusts the ISL51002's 10-bit offset DACs to null out the offset. Any offset, whether due to the video source or the ISL51002's analog amplifiers, is eliminated with 10-bit accuracy. Any drift is compensated for well before it can have a visible effect. Manual offset adjustment control is still available (a 10-bit register allows the firmware to adjust the offset ±64 codes in exactly 1 ADC LSB increments). Gain is now completely independent of offset (adjusting the gain no longer affects the offset, so there is no longer a need to program the firmware to cope with interactive offset and gain controls).

Finally, there should be no concerns over ABLC™ itself introducing visible artifacts; it doesn't. ABLC™ functions at a very low frequency, changing the offset in 1 LSB increments, so it can't cause visible brightness fluctuations. And once ABLC™ is locked, if the offset doesn't drift, the DACs won't change. If desired, ABLC™ can be disabled, allowing the firmware to work in the traditional way, with 10-bit offset DACs under the firmware's control.

Gain and Offset Control

To simplify image optimization algorithms, the ISL51002 features fully-independent gain and offset adjustment. Changing the gain does not affect the DC offset, and the weight of an Offset DAC LSB does not vary depending on the gain setting.

The full-scale gain is set in the three sets of registers (0x12 and 0x13-0x16 and 0x17).Each set of gain registers is divided into an 8-bit MSB register (0x12, 0x14 and 0x16) and a 2-bit LSB register providing a 10-bit gain value that both allows for 8-bit control compatible with the 8-bit family of AFEs and allows for the expansion of the gain resolution in future AFEs without significant firmware changes. The ISL51002 can accept input signals with amplitudes ranging from $0.35V_{P-P}$ to $1.4V_{P-P}$.

The offset controls shift the entire RGB input range, changing the input image brightness. Three separate registers provide independent control of the R, G, and B channels. Their nominal setting is 0x8000, which forces the ADC to output code 0x0000 (or 0x200 for the R (Pr) and B (Pb) channels in YPbPr mode) during the back porch period when ABLC™ is enabled.

Functional Description

Inputs

The ISL51002 digitizes analog video inputs in both RGB and Component (YPbPr) formats, with or without embedded sync (SOG).

RGB Inputs

For RGB inputs, the black/blank levels are identical and equal to 0V. The range for each color is typically 0V to 0.7V from black to white. HSYNC and VSYNC are separate signals.

Component YPbPr Inputs

In addition to RGB and RGB with SOG, the ISL51002 has an option that is compatible with the component YPbPr video inputs typically generated by DVD players. While the ISL51002 digitizes signals in these color spaces, it does not perform color space conversion; if it digitizes an RGB signal, it outputs digital RGB, while if it digitizes a YPbPr signal, it outputs digital YCbCr, also called YUV.

The Luminance (Y) signal is applied to the Green Channel and is processed in a manner identical to the Green input with SOG described previously. The color difference signals Pb and Pr are bipolar and swing both above and below the black level. When the YPbPr mode is enabled, the black level output for the color difference channels shifts to a mid scale value of 0x200. Setting configuration register 0x10[4] = 1 enables the YPbPr signal processing mode of operation.

TABLE 1. YUV MAPPING (4:4:4)

INPUT SIGNAL	ISL51002 INPUT CHANNEL	ISL51002 OUTPUT ASSIGNMENT	OUTPUT SIGNAL
Y	Green	Green	$Y_0Y_1Y_2Y_3$
Pb	Blue	Blue	$U_0U_1U_2U_3$
Pr	Red	Red	$V_0V_1V_2V_3$

The ISL51002 can optionally decimate the incoming data to provide a 4:2:2 output stream (configuration register 0x28[0] = 1) as shown in Table 2.

TABLE 2. YUV MAPPING (4:2:2)

INPUT SIGNAL	ISL51002 INPUT CHANNEL	ISL51002 OUTPUT ASSIGNMENT	OUTPUT SIGNAL
Y	Green	Green	$Y_0Y_1Y_2Y_3$
Pb	Blue	Blue	Driven Low
Pr	Red	Red	$U_0V_0U_2V_2$

Input Coupling

Inputs can be either AC-coupled (default) or DC-coupled (See register 0x10[3]). AC coupling is usually preferred since it allows video signals with substantial DC offsets to be accurately digitized. The ISL51002 provides a complete internal DC-restore function, including the DC restore clamp (See Figure 1) and programmable clamp timing (registers 0x24, 0x25, and 0x26).

When AC-coupled, the DC restore clamp is applied every line, a programmable number of pixels after the trailing edge of HSYNC. If register 0x60[2] = 0 (the default), the clamp will not be applied while the DPLL is coasting, preventing any clamp voltage errors from composite sync edges, equalization pulses, or Macrovision signals.

After the trailing edge of HSYNC, the DC restore clamp is turned on after the number of pixels specified in the DC Restore and ABLC™ Starting Pixel registers (0x24 and 0x25) has been reached. The clamp is applied for the number of pixels specified by the DC Restore Clamp Width Register (0x26). The clamp can be applied to the back porch of the video, or to the front porch (by increasing the DC Restore and ABLC™ Starting Pixel registers so all the active video pixels are skipped).

Note: The TriLevel detect for Sync on Green (SOG) utilizes the digitized data from the selected Green video channel. If TriLevel Sync is present, the default DC Clamp start position will clamp at the top of the TriLevel Sync pulse giving a false negative for TriLevel detect and clamping off the bottom half of the green video. If you have an indication of active SOG you must move the clamp start to a value greater than 0x30 to check to see if the Tri-level Sync is present.

If DC-coupled operation is desired, the input to the ADC will be the difference between the input signal ($R_{IN}1$, for example) and that channel's ground reference ($RGB_{GND}1$ in that example).

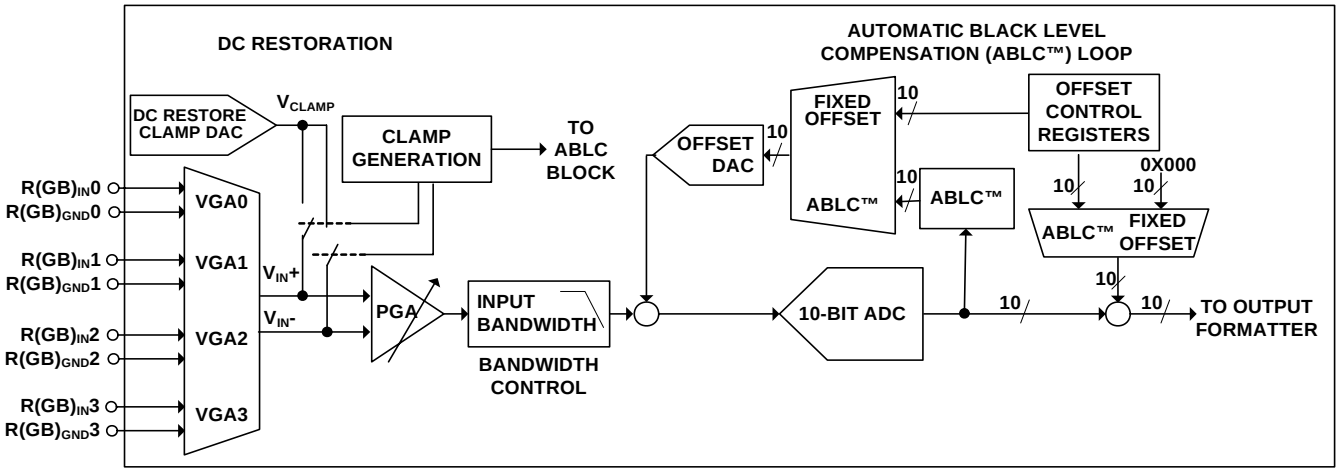


FIGURE 1. VIDEO FLOW (INCLUDING ABLC™)

SOG

For component YPbPr signals, the sync signal is embedded on the Y channel's video, which is connected to the green input, hence the name SOG (Sync on Green). The horizontal sync information is encoded onto the video input by adding the sync tip during the blanking interval. The sync tip level is typically 0.3V below the video black level.

To minimize the loading on the green channel, the SOG input for each of the green channels should be AC-coupled to the ISL51002 through a series combination of a 10nF capacitor and a 500Ω resistor.

SOG Slicer (Figure 2)

The SOG input has programmable threshold, 40mV of hysteresis, and an optional low pass filter than can be used to remove high frequency video spikes (generated by overzealous video peaking in a DVD player, for example) that can cause false SOG triggers. The SOG threshold sets the comparator threshold relative to the sync tip (the bottom of the SOG pulse).

Inside the ISL51002, a 1µA pulldown ensures that each sync tip triggersthe clamp circuit causing the tip to be clamped to a 600mV level. A comparator compares the SOG signal with an internal 4-bit programmable threshold level reference ranging from 0mV to 300mV above the sync clamp level. The SOG threshold level, hysteresis, and low-pass filter is programmed via registers 0x30and 0x31. If the Sync-On-Green function is not needed, the SOG_{IN} pin(s) may be left unconnected.

SYNC Processing

The ISL51002 can process sync signals from 3 different sources: discrete HSYNC and VSYNC, composite sync on the HSYNC input, or composite sync from a Sync-On-Green (SOG) signal embedded on the Green video input. The ISL51002 has SYNC activity detect functions to help the firmware determine which sync source is available.

Macrovision

The ISL51002 automatically detects the presense of Macrovision-encoded video. When Macrovision is detected, it generates a mask signal that is ANDed with the incoming SOG CSYNC signal to remove the Macrovision before the HSYNC goes to the PLL. No additional programming is required to support Macrovision.

The mask signal is also applied to the $HSYNC_{OUT}$ signal. When Sync Mask Disable = 0, any Macrovision present on the incoming sync will not be visible on $HSYNC_{OUT}$. If the application requires the Macrovision pulses to be visible on $HSYNC_{OUT}$, set the HSYNCOUT Mask Disable bit (register 0x7A bit 4).

Headswitching from Analog Videotape Signals

Occasionally this AFE may be used to digitize signals coming from analog videotape sources. The most common example of this is a Digital VCR (which for best signal quality would be connected to this AFE with a component YPbPr connection). If the digital VCR is playing an older analog VHS tape, the sync signals from the VCR may contain the worst of the traditional analog tape artifacts: headswitching. Headswitching is traditionally the enemy of PLLs with large capture ranges, because a headswitch can cause the HSYNC period to change by as much as ±90%. To the PLL, this can look like a frequency change of -50% to +900%, causing errors in the output frequency (and obviously the phase) to change. Subsequent HSYNCs have the correct, original period, but most analog PLLs will take dozens of lines to settle back to the correct frequency and phase after a headswitch disturbance. This causes the top of the image to "tear" during normal playback. In "trick modes" (fast forward and rewind), the HSYNC signal has multiple headswitch-like discontinuities, and many PLLs never settle to the correct value before the next headswitch, rendering the image completely unintelligible.

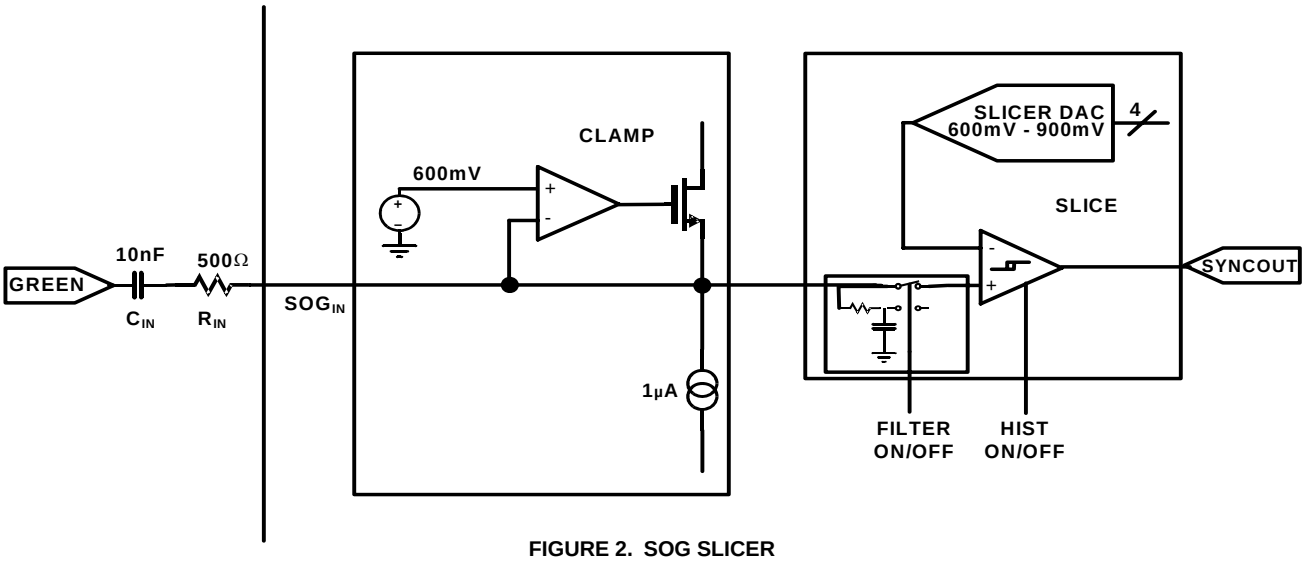


FIGURE 2. SOG SLICER

Intersil's DPLL has the capability to correct large phase changes almost instantly by maximizing the phase error gain while keeping the frequency gain relatively low. This is done by changing the contents of register 0x74 to 0x4C. This increases the phase error gain to 100%. Because a phase setting this high will slightly increase jitter, the default setting (0x49) for register 0x74 is recommended for all other sync sources.

SYNC TIMING MEASUREMENT

The ISL51002 analyzes the timing characteristics of the sysnc signals for the currently selected input channel and presents the results in registers 0x40 through 0x0x46.

The Hsync period and pulse width values are 16-bit numbers representing the number of crystal clocks in 16 consecutive periods or pulse widths giving a measurment resolution of 1/16th of a crystal clock.

The Vsync period is a 12-bit number representing the number of either Hsyncs or units of 512 crystal clocks that occure in one video frame. The default is to count Hsync pulses but setting register 0x4F[0] = 1 changes to the units to crystal clock / 512.

The Vsync pulse width is a 12-bit number representing the number of either Hsyncs or units of 512 crystal clocks that occure in one Vsync. The default is to count Hsync pulses but setting register 0x4F[0] = 1 changes to the units to crystal clock/512.

PGA

The ISL51002's Programmable Gain Amplifier (PGA) has a nominal gain range from 0.5V/V (-6dB) to 2.0V/V (+6dB). The transfer function is:

$$\text{Gain}\left(\frac{V}{V}\right) = 0.5 + \frac{\text{GainCode}}{170} \qquad \text{(EQ. 1)}$$

where GainCode is the value in the Gain register for that particular color. Note that for a gain of 1V/V, the GainCode should be 85 (0x55). This is a different center value than the 128 (0x80) value used by some other AFEs, so the firmware should take this into account when adjusting gains.

The PGAs are updated by the internal clamp signal once per line. In normal operation this means that there is a maximum delay of one HSYNC period between a write to a Gain register for a particular color and the corresponding change in that channel's actual PGA gain. If there is no regular HSYNC/SOG source, or if the external clamp option is enabled (register 0x10[7:6]) but there is no external clamp signal being generated, it may take up to 100ms for a write to the Gain register to update the PGA. This is not an issue in normal operation with RGB and YPbPr signals.

Offset DAC

The ISL51002 features a 10-bit Digital-to-Analog Converter (DAC) to provide extremely fine control over the full channel offset. The DAC is placed after the PGA to eliminate interaction between the PGA (controlling "contrast") and the Offset DAC (controlling "brightness").

In normal operation, the Offset DAC is controlled by the ABLC™ circuit, ensuring that the offset is always reduced to sub-LSB levels (See the following ABLC™ section for more information). When ABLC™ is enabled, the Offset register pairs (0x18 & 0x19 - 0x1C & 0x1D) control a digital offset added to or subtracted from the output of the ADC. This mode provides the best image quality and eliminates the need for any offset calibration.

If desired, ABLC™ can be disabled (0x27[0] = 1) and the Offset DAC programmed manually, with the 8 most significant bits in registers 0x18, 0x1A,10x1C, and the 2 least significant bits in registers 0x19[7:6], 0x1B[7:6] and 0x1D[7:6].

The default Offset DAC range is ±127 ADC LSBs. Setting 0x27[1] = 1 reduces the swing of the Offset DAC by 50%, making 1 Offset DAC LSB the weight of 1/2 of an ADC LSB. This provides the finest offset control and applies to both ABLC™ and manual modes.

Automatic Black Level Compensation (ABLC™)

ABLC is a function that continuously removes all offset errors from the incoming video signal by monitoring the offset at the output of the ADC and servoing the 10-bit analog DAC to force those errors to zero. When ABLC is enabled, the user offset control is a digital adder, with 10-bit resolution.

When the ABLC function is enabled (0x27[0] = 0), the ABLC function is executed every line after the trailing edge of HSYNC. If register 0x60[2] = 0 (the default), the ABLC function will be not be triggered while the DPLL is coasting, preventing any composite sync edges, equalization pulses, or Macrovision signals from corrupting the black data and potentially adding a small error in the ABLC accumulator.

After the trailing edge of HSYNC, the start of ABLC is delayed by the number of pixels specified in registers 0x24 and 0x25. After that delay, the number of pixels specified by register 0x27[3:2] are averaged together and added to the ABLC's accumulator. The accumulator stores the average black levels for the number of lines specified by register 0x27[6:4], which is then used to generate a 10-bit DAC value.

The ABLC can be set to allow the capture of signals below black by setting registers 0x65, 0x66 and 0x67 to a number that will controll the target for the ABLC servo loop. If you set register 0x65 to 0x04 then the ABLC will adjust the offset dac to produce an average output code on the Red channel of 0x10 during the back porch. Effectivly, the black level for a given channel will be set to the value of its ABLC offset target register times four. (output = register 0x65, 0x66 or 0x67 times 4).

ADC

The ISL51002 features 3 fully differential, high-speed 10-bit ADCs.

Clock Generation

A Digital Phase Lock Loop (DPLL) is employed to generate the pixel clock frequency. The HSYNC input and the external XTAL provide a reference frequency to the PLL. The PLL then generates the pixel clock frequency that equal to the incoming HSYNC frequency times the HTOTAL value programmed into registers 0x1E and 0x1F.

The stability of the clock is very important and correlates directly with the quality of the image. During each pixel time transition, there is a small window where the signal is slewing from the old pixel amplitude and settling to the new pixel value. At higher frequencies, the pixel time transitions at a faster rate, which makes the stable pixel time even smaller. Any jitter in the pixel clock reduces the effective stable pixel time and thus the sample window in which pixel sampling can be made accurately.

Sampling Phase

The ISL51002 provides 64 low-jitter phase choices per pixel period, allowing the firmware to precisely select the optimum sampling point. The sampling phase register is 0x20.

Auto Phase Adjust

The ISL51002 provides the ability to automatically adjust the Sampling Phase to the best setting. Set register 0x50 to 0x03 to activate the auto phase adjust function.

Data Enable (DE) Generator

The ISL51002 provides a signal that is high during the active video time when properly configured. This signal is used by devices such as DVI/HDMI transmitters to gate the active portion of the video and ignore the H and V sync times.

Auto DE Adjust

The ISL51002 provides the ability to automatically adjust the DE to the settings that are very close to ideal. The determination of exactly where on a line the active video starts and ends depends heavily on the video content being analyzed making the DE settings difficult to automate. The customer will be required to fine tune the DE settings after the Auto Adjust routine has completed. Set register 0x50 to 0x04 to activate the auto DE adjust function

HSYNC Slicer

To further minimize jitter, the HSYNC inputs are treated as analog signals, and brought into a precision slicer block with thresholds programmable in 400mV steps with 240mV of hysteresis, and a subsequent digital glitch filter that ignores any HSYNC transitions within 100ns of the initial transition. This processing greatly increases the AFE's rejection of ringing and reflections on the HSYNC line and allows the AFE to perform well even with pathological HSYNC signals.

Voltages given above and in the HSYNC Slicer register description are with respect to a 3.3V sync signal at the $HSYNC_{IN}$ input pin. To achieve 5V compatibility, a 680Ω series resistor should be placed between the HSYNC source and the $HSYNC_{IN}$ input pin. Relative to a 5V input, the hysteresis will be 240mV*5V/3.3V = 360mV, and the slicer step size will be 400mV*5V/3.3V = 600mV per step.

SYNC Status and Polarity Detection

The CH0 and CH1 Activity Status register (0x02) and the CH2 and CH3 Activity Status register (0x03) continuously monitor all 12sync inputs ($VSYNC_{IN}$, $HSYNC_{IN}$, and SOG_{IN} for each of 4 channels) and report their status, while the Selected Input Channel Characteristics register (0x01) gives more detailed information on the curently selected input channel.

However, accurate sync activity detection is always a challenge. Noise and repetitive video patterns on the Green

channel may look like SOG activity when there actually is no SOG signal, while non-standard SOG signals and TriLevel sync signals may have amplitudes below the default SOG slicer levels and not be easily detected. As a consequence, not all of the activity detect bits in the ISL51002 are correct under all conditions.

For best SOG operation, the SOG low pass filter (register 0x04[4] should always be enabled to reject the high frequency peaking often seen on video signals.

HSYNC and VSYNC Activity Detect

Activity on these bits always indicates valid sync pulses, so they should have the highest priority and be used even if the SOG activity bit is also set.

SOG Activity Detect

The SOG activity detect bit monitors the output of the SOG slicer, looking for 64 consecutive pulses with the same period and duty cycle. If there is no signal on the Green (or Y) channel, the SOG slicer will clamp the video to a DC level and will reject any sporadic noise. There should be no false positive SOG detects if there is no video on Green (or Y).

If there is video on Green (or Y) with no valid SOG signal, the SOG activity detect bit may sometimes report false positives (it will detect SOG when no SOG is actually present). This is due to the presence of video with a repetitive pattern that creates a waveform similar to SOG. For example, the desktop of a PC operating system is black during the front porch, horizontal sync, and back porch, then increases to a larger value for the video portion of the screen. This creates a repetitive video waveform very similar to SOG that may falsely trigger the SOG Activity detect bit. However, in these cases where there is active video without SOG, the SYNC information will be provided either as separate H and V sync on $HSYNC_{IN}$ and $VSYNC_{IN}$, or composite sync on $HSYNC_{IN}$. $HSYNC_{IN}$ and $VSYNC_{IN}$ should therefore be used to qualify SOG. The SOG Active bit should only be considered valid if HSYNC Activity Detect = 0. Note: Some pattern generators can output HSYNC and SOG simultaneously, in which case both the HSYNC and the SOG activity bits will be set, and valid. Even in this case, however, the monitor should still choose HSYNC over SOG.

TriLevel Sync Detect

The TriLevel detect for Sync on Green (SOG) utilizes the digitized data from the selected Green video channel. If TriLevel Sync is present, the default DC Clamp start position will clamp at the top of the TriLevel Sync pulse giving a false negative for TriLevel detect and clamping off the bottom half of the green video. If you have an indication of active SOG you must move the clamp start to a value greater than 0x30 to check to see if the TriLevel Sync is present.

SYNC Output Signals

The ISL51002 has a pair of HSYNC output signals, $HSYNC_{OUT}$ and $VSYNC_{OUT}$, and HS_{OUT}.

$HSYNC_{OUT}$ and $VSYNC_{OUT}$ are buffered versions of the incoming sync signals; no synchronization is done. These signals are used for mode detection

HS_{OUT} is generated by the ISL51002's logic and is synchronized to the output DATACLK and the digital pixel data on the output databus. HS_{OUT} is used to signal the start of a new line of digital data.

Both $HSYNC_{OUT}$ and $VSYNC_{OUT}$ (including the sync separator function) remain active in power-down mode. This allows them to be used in conjunction with the Sync Status registers to detect valid video without powering up the ISL51002.

$HSYNC_{OUT}$

$HSYNC_{OUT}$ is an unmodified, buffered version of the incoming $HSYNC_{IN}$ or SOG_{IN} signal of the selected channel, with the incoming signal's period, polarity, and width to aid in mode detection. $HSYNC_{OUT}$ will be the same format as the incoming sync signal: either horizontal or composite sync. If a SOG input is selected, $HSYNC_{OUT}$ will output the entire SOG signal, including the VSYNC portion, pre-/post-equalization pulses if present, and Macrovision pulses if present. $HSYNC_{OUT}$ remains active when the ISL51002 is in power-down mode. $HSYNC_{OUT}$ is generally used for mode detection.

$VSYNC_{OUT}$

$VSYNC_{OUT}$ is an unmodified, buffered version of the incoming $VSYNC_{IN}$ signal of the selected channel, with the original VSYNC period, polarity, and width to aid in mode detection. If a SOG input is selected, this signal will output the VSYNC signal extracted by the ISL51002's sync slicer. Extracted VSYNC will be the width of the embedded VSYNC pulse plus pre- and post-equalization pulses (if present). Macrovision pulses from an NTSC DVD source will lengthen the width of the VSYNC pulse. Macrovision pulses from other sources (PAL DVD or videotape) may appear as a second VSYNC pulse encompassing the width of the Macrovision. See the Macrovision section for more information. $VSYNC_{OUT}$ (including the sync separator function) remains active in power-down mode. $VSYNC_{OUT}$ is generally used for mode detection, start of field detection, and even/odd field detection.

HS_{OUT}

HS_{OUT} is generated by the ISL51002's control logic and is synchronized to the output DATACLK and the digital pixel data on the output databus. Its trailing edge is aligned with pixel 0. Its width, in units of pixels, is determined by register 0x2A, and its polarity is determined by register 0x29[3]. As the width is increased, the trailing edge stays aligned with pixel 0, while the leading edge is moved backwards in time relative to pixel 0. HS_{OUT} is used by the scaler to signal the start of a new line of pixels.

Crystal Oscillator

An external 12MHz to 27MHz crystal supplies the low-jitter reference clock to the DPLL. The absolute frequency of this crystal within this range is unimportant, as is the crystal's temperature coefficient, allowing use of less expensive, lower-grade crystals.

As an alternative to a crystal, the $XTAL_{IN}$ pin can be driven with a 3.3V CMOS-level external clock source at any frequency between 12MHz and 27MHz. The ISL51002's jitter specification assumes a low-jitter crystal source. If the external clock source has increased jitter, the sample clock generated by the DPLL may exhibit increased jitter as well.

EMI Considerations

There are two possible sources of EMI on the ISL51002:

Crystal oscillator.

The EMI from the crystal oscillator is negligible. This is due to an amplitude-regulated, low voltage sine wave oscillator circuit, instead of the typical high-gain square wave inverter-type oscillator, so there are no harmonics. *The crystal oscillator is not a significant source of EMI.*

Digital output switching.

This is the largest potential source of EMI. However, the EMI is determined by the PCB layout and the loading on the databus. The way to control this is to put series resistors on the output of all the digital pins (as our demo board and reference circuits show). These resistors should be as large as possible, while still meeting the setup and hold timing requirements of the scaler. We recommend starting with 22Ω. If the databus is heavily loaded (long traces, many other part on the same bus), this value may need to be reduced. If the databus is lightly loaded, it may be increased.

Intersil's recommendations to minimize EMI are:

- Minimize the databus trace length
- Minimize the databus capacitive loading.

If EMI is a problem in the final design, increase the value of the digital output series resistors to reduce slew rates on the bus. This can only be done as long as the scaler's setup and hold timing requirements continue to be met.

Standby Mode

The ISL51002 can be placed into a low power standby mode by writing a 0x0F to register 0x2C, powering down the triple ADCs, the DPLL, and most of the internal clocks.

To allow input monitoring and mode detection during power-down, the following blocks remain active:

- Serial interface (including the crystal oscillator) to enable register read/write activity
- Activity and polarity detect functions (registers 0x01 and 0x02)
- The $HSYNC_{OUT}$ and $VSYNC_{OUT}$ pins (for mode detection)

Initialization

The ISL51002 initializes with default register settings for an AC-coupled, RGB input on the VGA1 channel, with a 30-bit output.

Reset

The ISL51002 has a Power On Reset (POR) function that resets the chip to its default state when power is initially applied, including resetting all the registers to their default settings as described in the Register Listing. The POR function takes 512k Crystal clocks (~21ms at 25MHz) to complete. The external $\overline{\text{RESET}}$ pin duplicates the reset function of the POR without having to cycle the power supplies. The $\overline{\text{RESET}}$ pin does not need to be used in normal operation and can be tied high.

ISL51002 Serial Communication

Overview

The ISL51002 uses a 2-wire serial bus for communication with its host. SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by all devices on the bus. SDA is open drain to allow multiple devices to share the same bus simultaneously.

Communication is accomplished in three steps:

1) The Host selects the ISL51002 it wishes to communicate with.
2) The Host writes the initial ISL51002 Configuration Register address it wishes to write to or read from.
3) The Host writes to or reads from the ISL51002's Configuration Register. The ISL51002's internal address pointer auto increments, so to read registers 0x00 through 0x1B, for example, one would write 0x00 in step 2, then repeat step three 28 times, with each read returning the next register value.

The ISL51002 has a 7-bit address on the serial bus. The upper 6-bits are permanently set to 100110, with the lower bit determined by the state of pin 67. This allows two ISL51002s to be independently controlled while sharing the same bus.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 3). The ISL51002 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit serial address plus a R/$\overline{\text{W}}$ bit, indicating if the next transaction will be a Read (R/$\overline{\text{W}}$ = 1) or a Write (R/$\overline{\text{W}}$ = 0). If the address transmitted matches that of any device on the bus, that device must respond with an ACKNOWLEDGE (Figure 4).

Once the serial address has been transmitted and acknowledged, one or more bytes of information can be written to or read from the slave. Communication with the selected device in the selected direction (read or write) is ended by a STOP command, where SDA rises while SCL is high (Figure 3), or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

Data on the serial bus must be valid for the entire time SCL is high (Figure 5). To achieve this, data being written to the ISL51002 is latched on a delayed version of the rising edge of SCL. SCL is delayed and deglitched inside the ISL51002 for three crystal clock periods (120ns for a 25MHz crystal) to eliminate spurious clock pulses that could disrupt serial communication.

When the contents of the ISL51002 are being read, the SDA line is updated after the falling edge of SCL, delayed and deglitched in the same manner.

Configuration Register Write

Figure 6 shows two views of the steps necessary to write one or more words to the Configuration Register.

Configuration Register Read

Figure 7 shows two views of the steps necessary to read one or more words from the Configuration Register.

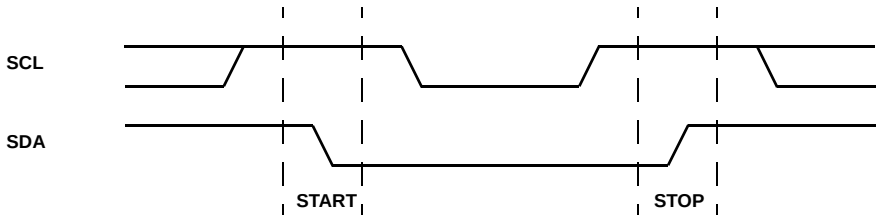


FIGURE 3. VALID START AND STOP CONDITIONS

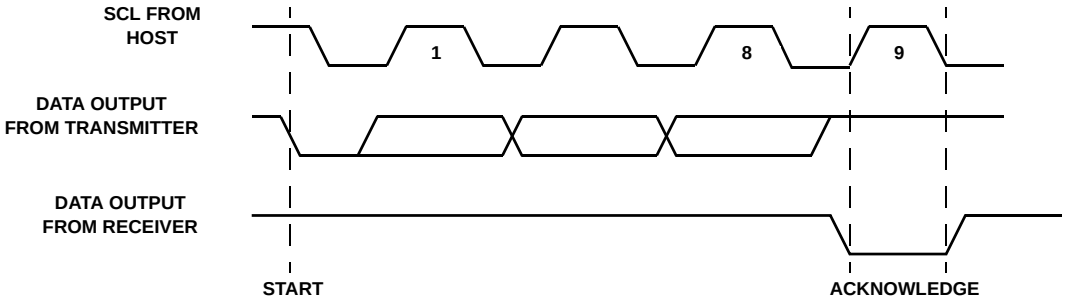


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

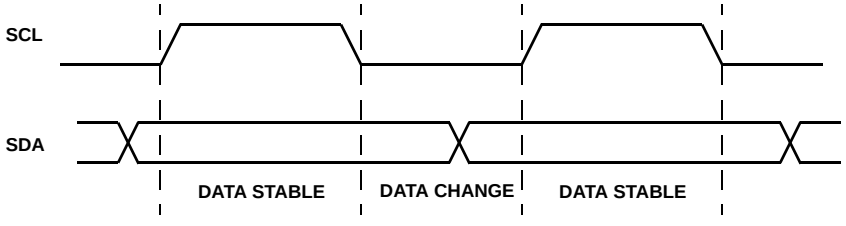
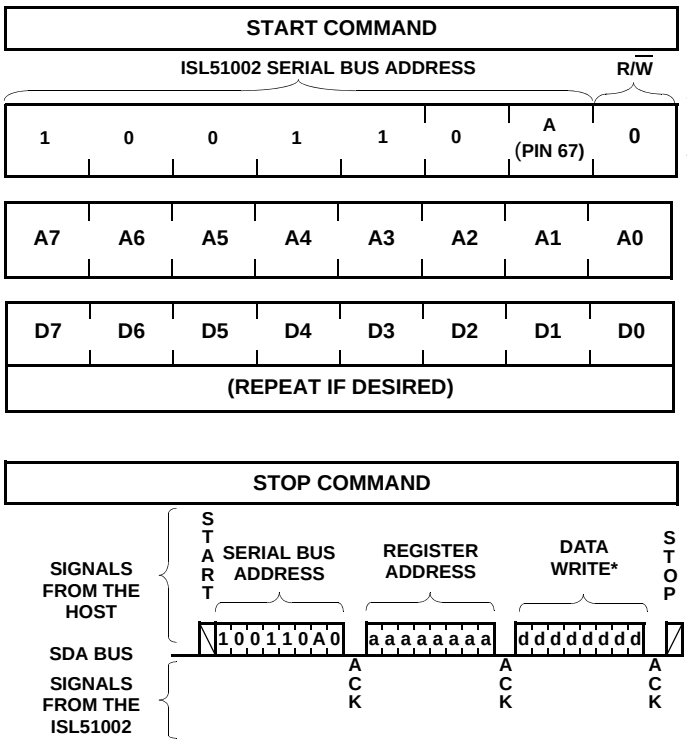


FIGURE 5. VALID DATA CHANGES ON THE SDA BUS



Signals the beginning of serial I/O

ISL51002 Serial Bus Address Write

This is the 7-bit address of the ISL51002 on the 2-wire bus. The address is 0x98 if pin 67 is low, 0x9A if pin 67 is high. Shift this value left to when adding the R/W bit.

ISL51002 Register Address Write

This is the address of the ISL51002's configuration register that the following byte will be written to.

ISL51002 Register Data Write(s)

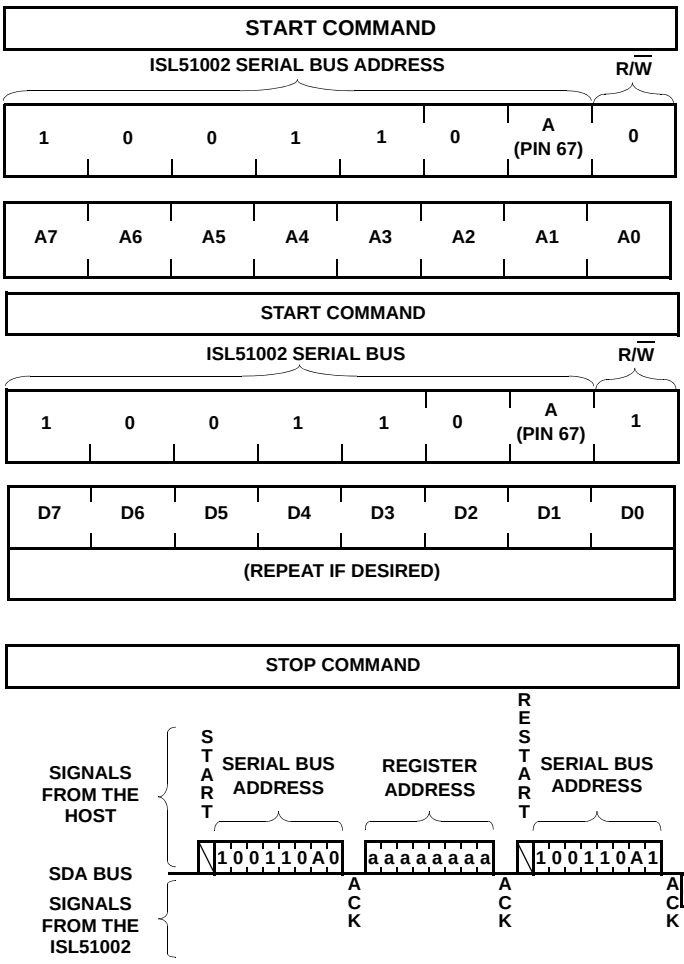
This is the data to be written to the ISL51002's configuration register.

Note: The ISL51002's Configuration Register's address pointer auto increments after each data write: repeat this step to write multiple sequential bytes of data to the Configuration Register.

Signals the ending of serial I/O

* The data write step may be repeated to write to the ISL51002's Configuration Register sequentially, beginning at the Register Address written in the previous step.

FIGURE 6. CONFIGURATION REGISTER WRITE



Signals the beginning of serial I/O

ISL51002 Serial Bus Address Write

This is the 7-bit address of the ISL51002 on the 2-wire bus. The address is 0x98 if pin 67 is low, 0x9A if pin 67 is high. R/$\overline{W}$ = 0, indicating next transaction will be a write.

ISL51002 Register Address Write

This sets the initial address of the ISL51002's configuration register for subsequent reading.

Ends the previous transaction and starts a new one

ISL51002 Serial Bus Address Write

This is the 7-bit address of the ISL51002 on the 2-wire bus. The address is 0x98 if pin 67 is low, 0x9A if pin 67 is high. R/$\overline{W}$ = 1, indicating next transaction(s) will be a read.

ISL51002 Register Data Read(s)

This is the data read from the ISL51002's configuration register.

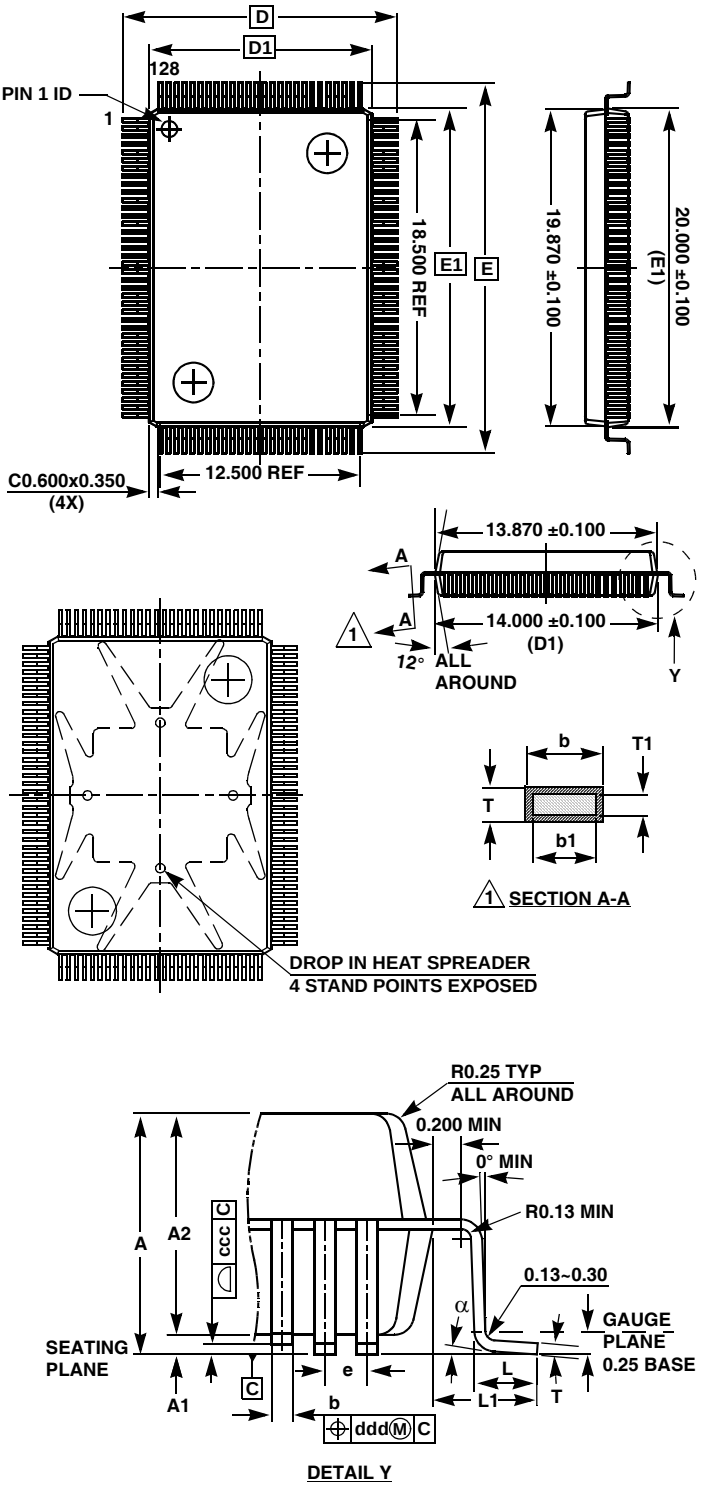
Note: The ISL51002's Configuration Register's address pointer auto increments after each data read: repeat this step to read multiple sequential bytes of data from the Configuration Register.

Signals the ending of serial I/O

* The data read step may be repeated to read from the ISL51002's Configuration Register sequentially, beginning at the Register Address written in the two steps previous.

FIGURE 7. CONFIGURATION REGISTER READ

Metric Plastic Quad Flatpack Packages (MQFP)



MDP0055

14x20mm 128 LEAD MQFP (WITH AND WITHOUT HEAT SPREADER) 3.2mm FOOTPRINT

SYMBOL	DIMENSIONS	REMARKS
A	Max 3.40	Overall height
A1	0.250~0.500	Standoff
A2	2.750±0.250	Package thickness
α	0°~7°	Foot angle
b	0.220±0.050	Lead width (1)
b1	0.200±0.030	Lead base metal width (1)
D	17.200±0.250	Lead tip to tip
D1	14.000±0.100	Package length
E	23.200±0.250	Lead tip to tip
E1	20.000±0.100	Package width
e	0.500 Base	Lead pitch
L	0.880±0.150	Foot length
L1	1.600 Ref.	Lead length
T	0.170±0.060	Frame thickness (1)
T1	0.152±0.040	Frame base metal thickness (1)
ccc	0.100	Foot coplanarity
ddd	0.100	Foot position

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NOTES:

1. General tolerance: Distance ±0.100, Angle +2.5°.
2. (1) Matte finish on package body surface except ejection and pin 1 marking (Ra 0.8~2.0um).
3. All molded body sharp corner RADII unless otherwise specified (Max RO.200).
4. Package/Leadframe misalignment (X, Y): Max. 0.127
5. Top/Bottom misalignment (X, Y): Max. 0.127
6. Drawing does not include plastic or metal protrusion or cutting burr.
7. (2) Compliant to JEDEC MS-022.