PA41/PA42 • PA41A/PA42A

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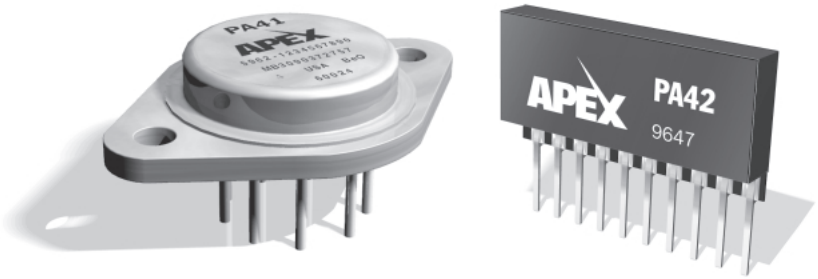
FEATURES

- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT—2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK
- AVAILABLE IN DIE FORM—PA41DIE



APPLICATIONS

- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

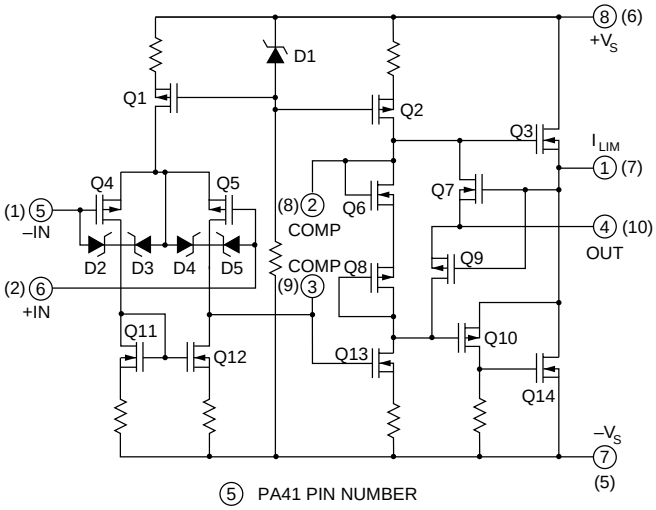
DESCRIPTION

The PA41/42 are high voltage monolithic MOSFET operational amplifiers achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA41 is packaged in a hermetically sealed TO-3 and all circuitry is isolated from the case by an aluminum nitride (AlN) substrate.

The PA42 is packaged in APEX's hermetic ceramic SIP10 package.

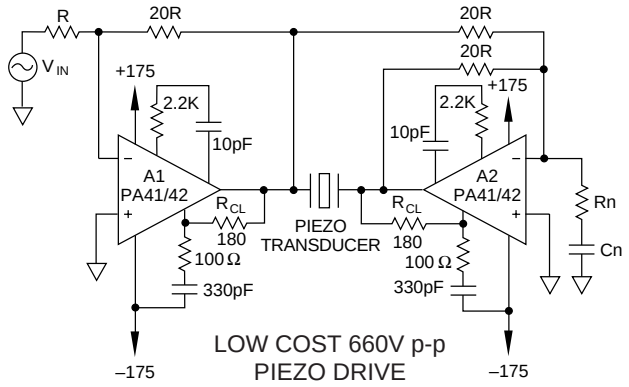
EQUIVALENT SCHEMATIC



(5) PA41 PIN NUMBER

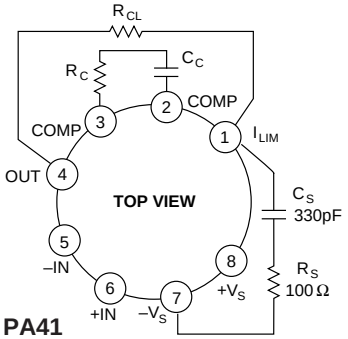
(1) PA42 PIN NUMBER

TYPICAL APPLICATION



Two PA41/42 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 volt total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

EXTERNAL CONNECTIONS



PA41

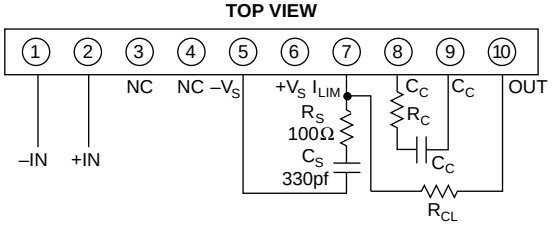
PHASE COMPENSATION

Gain	C_C	R_C
1	18pF	2.2KΩ
≥10	10pF	2.2KΩ
≥30	3.3pF	2.2KΩ

C_S, C_C ARE NPO RATED FOR FULL SUPPLY VOLTAGE.

$$R_{CL} = \frac{3}{I_{LIM}}$$

PA42



NOTE: PA41 Recommended mounting torque is 4-7 in•lbs (.45 -.79 N•m)

CAUTION: The use of compressible, thermally conductive insulators may void warranty.

ABSOLUTE MAXIMUM RATINGS

	PA41/PA41A	PA42/PA42A
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V	350V
OUTPUT CURRENT, continuous within SOA	60 mA	60 mA
OUTPUT CURRENT, peak	120 mA	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	12W	9W
INPUT VOLTAGE, differential	±16 V	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	300°C	220°C
TEMPERATURE, junction[2]	150°C	150°C
TEMPERATURE, storage	–65 to +150°C	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C	–40 to +125°C

SPECIFICATIONS

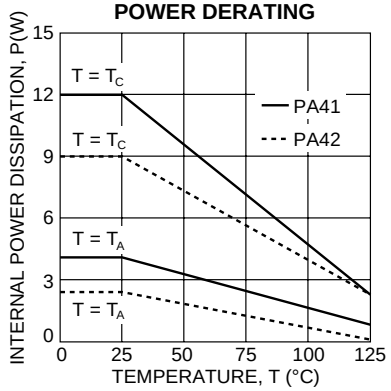
PARAMETER	TEST CONDITIONS[1]	PA41/PA42 MIN	PA41/PA42 TYP	PA41/PA42 MAX	PA41A/PA42A MIN	PA41A/PA42A TYP	PA41A/PA42A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			25	40		15	30	mV
OFFSET VOLTAGE, vs. temperature[4, 7]	Full temperature range		70	130		40/*	65/*	µV/°C
OFFSET VOLTAGE, vs supply			20	32		*	*	µV/V
OFFSET VOLTAGE, vs time			75			*		µV √kh
BIAS CURRENT, initial[7]			5/100	50/2000		*	*	pA
BIAS CURRENT, vs supply			.2/.5	.5/50		*	*	pA/V
OFFSET CURRENT, initial[7]			2.5/100	50/400		*	*	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			5			*		pF
COMMON MODE, voltage range		$\pm V_S$–12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		*	*		dB
NOISE, broad band	10kHz BW, R_S = 1KΩ		50			*		µV RMS
NOISE, low frequency	1-10 Hz		110			*		µV p-p
GAIN								
OPEN LOOP at 15Hz	R_L = 5KΩ	94	106		*	*		dB
BANDWIDTH, open loop			1.6			*		MHz
POWER BANDWIDTH	C_C = 10pf, 280V p-p		26			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		$\pm V_S$–10	$\pm V_S$–8.5		V
CURRENT, peak[5]		120			*			mA
CURRENT, continuous		60			*			mA
SETTLING TIME to .1%	C_C = 10pF, 10V step, A_V = –10		12			*		µs
SLEW RATE	C_C = OPEN		40			*		V/µs
CAPACITIVE LOAD	A_V = +1	10			*			nF
RESISTANCE[6], no load	R_{CL} = 0		150			*		Ω
RESISTANCE[6], 20mA load	R_{CL} = 0		25			*		Ω
POWER SUPPLY								
VOLTAGE[3]	See Note 3	±50	±150	±175	*	*	*	V
CURRENT, quiescent			1.6	2.0	.9	1.4	1.8	mA
THERMAL								
PA41 RESISTANCE, AC junction to case	F > 60Hz		5.4	6.5		*	*	°C/W
PA42 RESISTANCE, AC junction to case	F > 60Hz		7	10		*	*	°C/W
PA41 RESISTANCE, DC junction to case	F < 60Hz		9	10.4		*	*	°C/W
PA42 RESISTANCE, DC junction to case	F < 60Hz		12	14		*	*	°C/W
PA41 RESISTANCE, junction to air	Full temperature range		30			*		°C/W
PA42 RESISTANCE, junction to air	Full temperature range		55			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification for PA41A/PA42A is identical to the specification for PA41/PA42 in applicable column to the left.

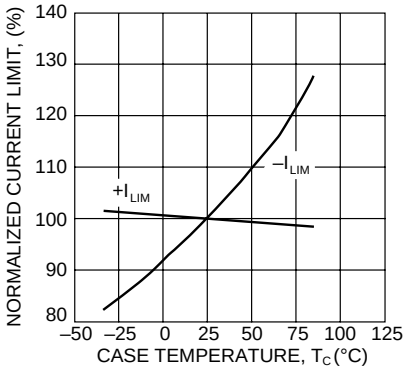
1. Unless otherwise noted T_C = 25°C, C_C = 18pF, R_C = 2.2KΩ. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above T_C = 25°C.
4. Sample tested by wafer to 95%.
5. Guaranteed but not tested.
6. The selected value of R_{CL} must be added to the values given for total output resistance.
7. Specifications separated by / indicate values for the PA41 and PA42 respectively.

CAUTION The PA41/PA42 is constructed from MOSFET transistors. ESD handling procedures must be observed.

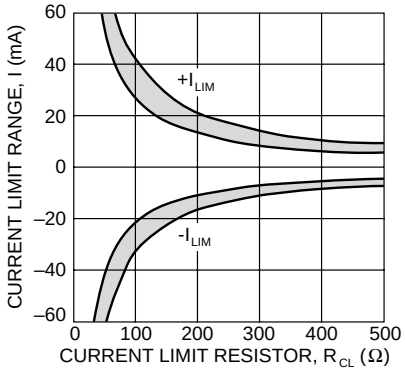
POWER DERATING



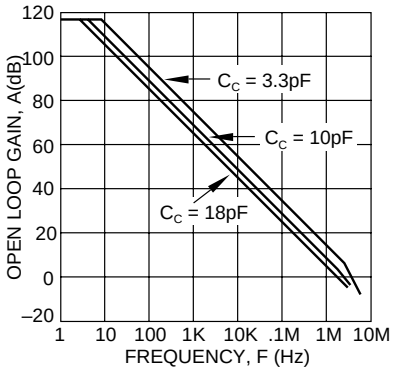
CURRENT LIMIT



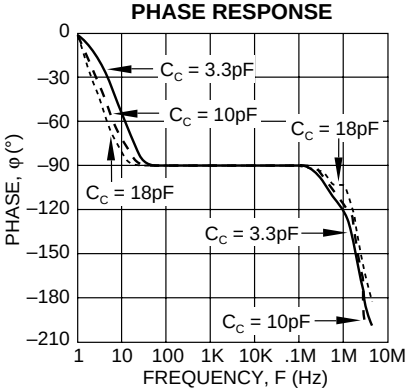
CURRENT LIMIT



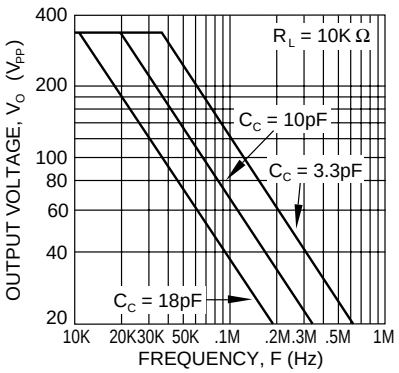
SMALL SIGNAL RESPONSE



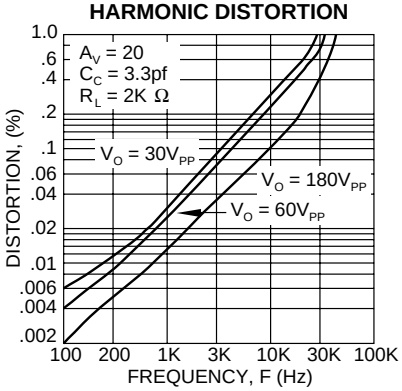
PHASE RESPONSE



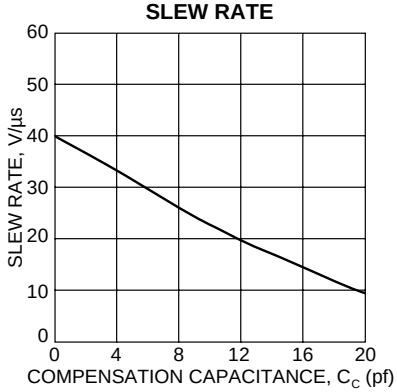
POWER RESPONSE



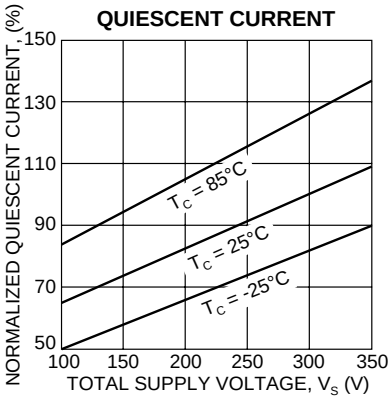
HARMONIC DISTORTION



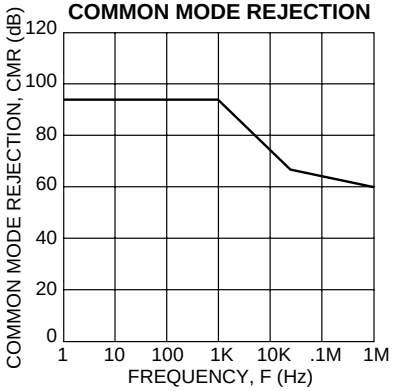
SLEW RATE



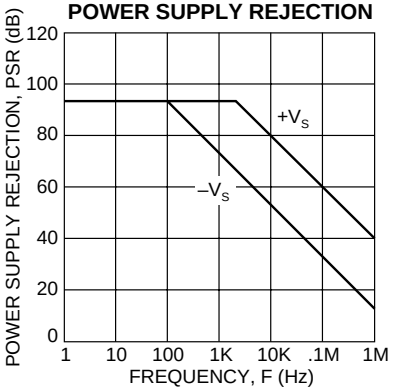
QUIESCENT CURRENT



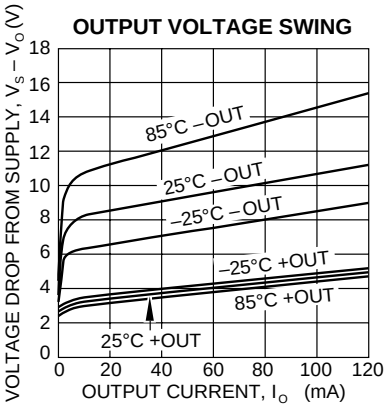
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation the current limit resistor, R_{CL}, must be connected as shown in the external connection diagram. The minimum value is 18 ohms, however for optimum reliability the resistor value should be set as high as possible. The value can be estimated as follows with the maximum practical value of 500 ohms.

$$R_{CL} = \frac{3}{I_{LIM}}$$

Use the typical performance graphs as a guide for expected variations in current limit value with a given R_{CL} and variations over temperature. The selected value of R_{CL} must be added to the specified typical value of output resistance to calculate the total output resistance. Since the load current passes through R_{CL} the value selected also affects the output voltage swing according to:

$$V_R = I_O * R_{CL}$$

where V_R is the voltage swing reduction.

When the amplifier is current limiting, there may be small signal spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, and load. The oscillation will cease as the amplifier comes out of current limit.

INPUT PROTECTION

The PA41/42 inputs are protected against common mode voltages up the supply rails and differential voltages up to ±16 volts as well as static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input, but this may be insufficient for severe overloads. It may be necessary to add external resistors to the application circuit where severe overload conditions are expected. Limiting input current to 1mA will prevent damage.

STABILITY

The PA41/42 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10 nF. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 5K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

The PA41/42 is externally compensated and performance can be tailored to the application. Use the graphs of small signal gain and phase response as well as the graphs for slew rate and power response as a guide. The compensation capacitor C_C must be rated at 350V working voltage. The compensation capacitor and associated resistor R_C must be mounted closely to the amplifier pins to avoid spurious oscillation. An NPO capacitor is recommended for compensation.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.