Data Sheet December 13, 2006 FN6345.0

Micropower, Single Supply, Rail-to-Rail Input-Output Instrumentation Amplifier and Precision Operational Amplifier

The ISL28274 is a combination of a micropower instrumentation amplifier (Amp A) with a low power precision amplifier (Amp B) in a single package. The ISL28474 consist of two micropower instrumentation amplifiers (Amp A) and two low power precision amplifiers (Amp B) in a single package. The amplifiers are optimized for operation at 2.4V to 5V single supplies. Inputs and outputs can operate rail-to-rail. As with all instrumentation amplifiers, a pair of inputs provide a high common-mode rejection and are completely independent from a pair of feedback terminals. The feedback terminals allow zero input to be translated to any output offset, including ground. A feedback divider controls the overall gain of the amplifier. The additional precision amplifier can be used to generate higher gain, with smaller feedback resistors or used to generate a reference voltage.

The instrumentation amp (Amp A) is compensated for a gain of 100 or more and the precision amp (Amp B) is unity gain stable. Both amplifiers have PMOS inputs that provide less than 30pA input bias currents.

The amplifiers can be operated from one lithium cell or two Ni-Cd batteries. The amplifiers input range goes from below ground to slightly above positive rail. The output stage swings completely to ground or positive supply - no pull-up or pull-down resistors are needed.

Ordering Information

PART NUMBER (Note)	PART MARKING	QTY. PER TUBE/REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28274FAZ	28274FAZ	97/Tube	16 Ld QSOP	MDP0040
ISL28274FAZ-T7	28274FAZ	7” (1000 pcs)	16 Ld QSOP Tape & Reel	MDP0040
Coming Soon ISL28474FAZ	ISL28474FAZ	55 /Tube	24 Ld QSOP	MDP0040
Coming Soon ISL28474FAZ-T7	ISL28474FAZ	7” (1000 pcs)	24 Ld QSOP Tape & Reel	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

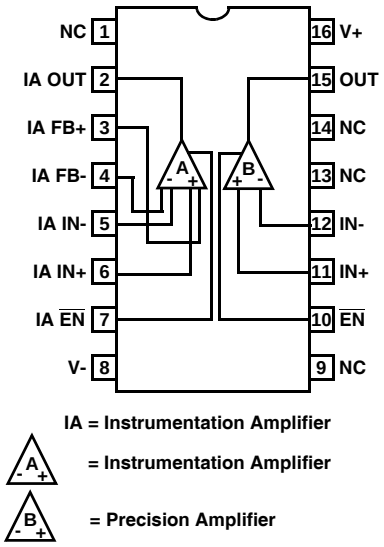
- Combination of IN-AMP and OP-AMP in a single package
- 120µA supply current for ISL28274
- Input Offset Voltage IN-AMP 400µV max
- Input Offset Voltage OP-AMP 225µV max
- 30pA max input bias current
- 100dB CMRR and PSRR
- Single supply operation of 2.4V to 5.0V
- Ground Sensing
- Input voltage range is rail-to-rail and output swings rail-to-rail
- Pb-free plus anneal available (RoHS compliant)

Applications

- 4-20mA loops
- Industrial Process Control
- Medical Instrumentations

Pinout

ISL28274
(16 LD QSOP)
TOP VIEW

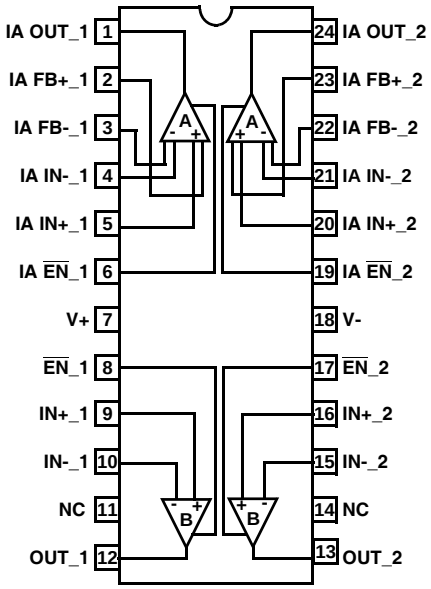


IA = Instrumentation Amplifier

= Instrumentation Amplifier

= Precision Amplifier

ISL28474
(16 LD QSOP)
TOP VIEW



IA = Instrumentation Amplifier

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Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Input Current (IN, FB) 5mA
Differential Input Voltage (IN, FB) 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD tolerance, Human Body Model 3kV
ESD tolerance, Machine Model 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
16 Ld QSOP Package	112
24 Ld QSOP Package	88

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

INSTRUMENTATION AMPLIFIER "A" V+ = +5V, V_S- = GND, VCM = 1/2V_S+ T_A = +25°C, unless otherwise specified. For ISL28274 ONLY. **Boldface limits apply over the operating temperature range, -40°C to +125°C**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage		400 **-750**	35	400 **750**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	Temperature = -40°C to +125°C		0.7		µV/°C
I_{OS}	Input Offset Current between IN+ and IN-, and between FB+ and FB-	(see Figure 44 for extended temperature range) -40°C to +85°C	-30 **-80**	±5	30 **80**	pA
I_B	Input Bias Current (IN+, IN-, FB+, and FB- terminals)	(see Figure 36 and 37 for extended temperature range) -40°C to +85°C	-30 **-80**	±10	30 **80**	pA
e_N	Input Noise Voltage	f = 0.1Hz to 10Hz		0.75		μV_{P-P}
	Input Noise Voltage Density	f_0 = 1kHz		210		nV/√Hz
i_N	Input Noise Current Density	f_0 = 1kHz		0.65		pA/√Hz
R_{IN}	Input Resistance			1		GΩ
V_{IN}	Input Voltage Range	V_+ = 2.4V to 5.0V	0		V_+	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 5V	80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5V	80 **75**	100		dB
E_G	Gain Error	R_L = 100kΩ to 2.5V		-0.2		%
SR	Slew Rate	R_L = 1kΩ to GND	0.40 **0.35**	0.5	0.65 **0.70**	V/µs
GBWP	Gain Bandwidth Product			2.5		MHz

Electrical Specifications

OPERATIONAL AMPLIFIER "B" V_S+ = +5V, V_S- = GND, VCM = 1/2V_S+ T_A = +25°C, unless otherwise specified. For ISL28274 ONLY. **Boldface limits apply over the operating temperature range, -40°C to +125°C**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage		-225 **-450**	±20	225 **450**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			1.2		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			2.2		µV/°C
I_{OS}	Input Offset Current	(see Figure 46 for extended temperature range) -40°C to +85°C	-30 **-80**	±5	30 **80**	pA

Electrical Specifications OPERATIONAL AMPLIFIER "B" V_S+ = +5V, V_S- = GND, VCM = 1/2V_S+ T_A = +25°C, unless otherwise specified. For ISL28274 ONLY. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_B	Input Bias Current	(see Figure 40 and 41for extended temperature range) -40°C to +85°C	-30 **-80**	±10	30 **80**	pA
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		5.4		μV_{PP}
	Input Noise Voltage Density	f_O = 1kHz		50		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.14		pA/√Hz
CMIR	Input Voltage Range	Guaranteed by CMRR test	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5V	85 **80**	105		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	200 **190**	300		V/mV
SR	Slew Rate		0.12 **0.09**	±0.14	0.16 **0.21**	V/µs
GBW	Gain Bandwidth Product			300		kHz

Electrical Specifications COMMON ELECTRICAL SPECIFICATIONS V+ = 5V, V- = GND, VCM = 1/2V_S+ T_A = 25°C, unless otherwise specified.For ISL28274 ONLY. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ		3	6 **30**	mV
		Output low, R_L = 1kΩ		130	175 **225**	mV
		Output high, R_L = 100kΩ	4.990 **4.97**	4.996		V
		Output high, R_L = 1kΩ	4.800 **4.750**	4.880		V
$I_{S,ON}$	Supply Current, Enabled	ISL28274 All channels enabled		120	156 **175**	µA
		ISL28474 All channels enabled		240		µA
$I_{S,OFF}$	Supply Current, Disabled	ISL28274 All channels enabled		4	7 **9**	µA
		ISL28474 All channels enabled		8		µA
I_{SC}+	Short Circuit Sourcing Capability	R_L = 10Ω	28 **25**	31		mA
I_{SC}-	Short Circuit Sinking Capability	R_L = 10Ω	24 **20**	26		mA
V_S	Minimum Supply Voltage		**2.4**			V
V_{INH}	Enable Pin High Level		**2**			V
V_{INL}	Enable Pin Low Level				**0.8**	V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V		0.8	1 **1.3**	µA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V		0 **26**	50 **100**	µA

Typical Performance Curves

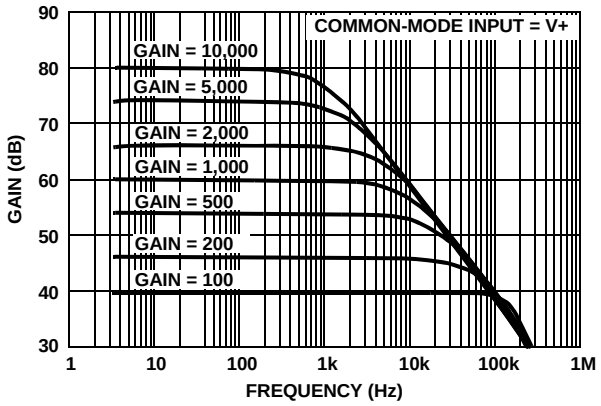


FIGURE 1. AMPLIFIER "A"(INAMP) FREQUENCY RESPONSE vs CLOSED LOOP GAIN

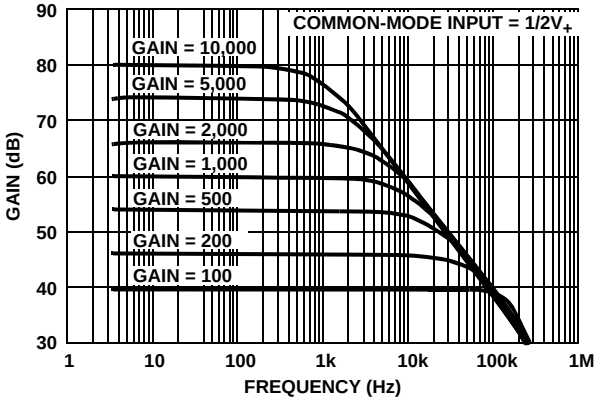


FIGURE 2. AMPLIFIER "A"(INAMP) FREQUENCY RESPONSE vs CLOSED LOOP GAIN. V_{CM} = 1/2V+

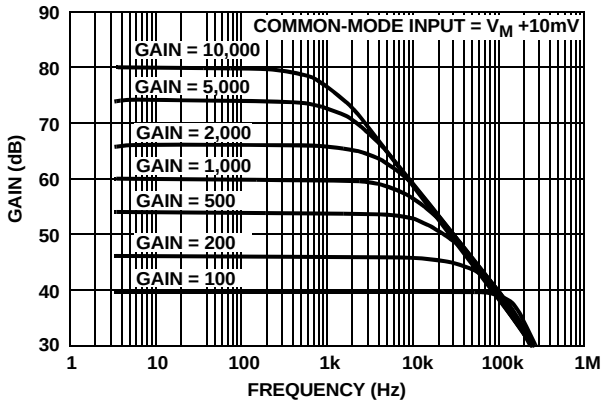


FIGURE 3. AMPLIFIER "A"(INAMP) FREQUENCY RESPONSE vs CLOSED LOOP GAIN

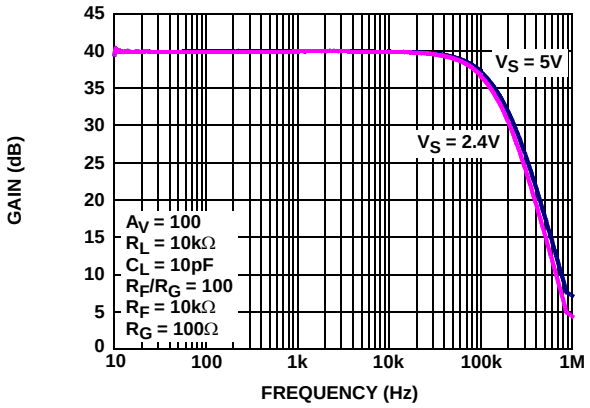


FIGURE 4. AMPLIFIER "A"(INAMP) FREQUENCY RESPONSE vs SUPPLY VOLTAGE

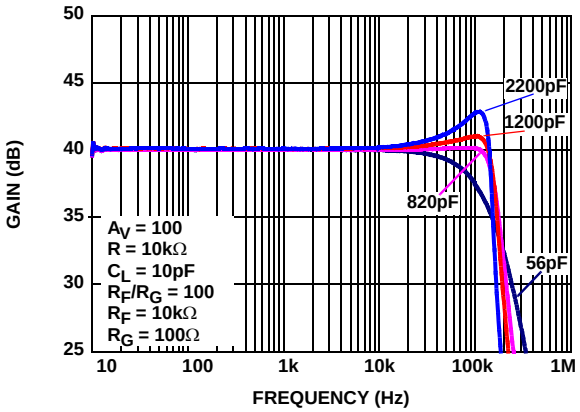


FIGURE 5. AMPLIFIER "A"(INAMP) FREQUENCY RESPONSE vs C_{LOAD}

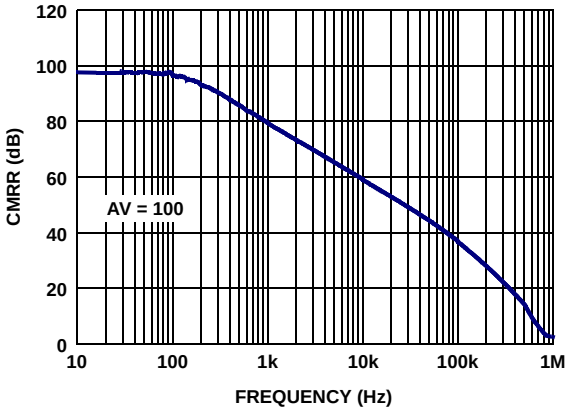


FIGURE 6. AMPLIFIER "A"(INAMP) CMRR vs FREQUENCY

Typical Performance Curves (Continued)

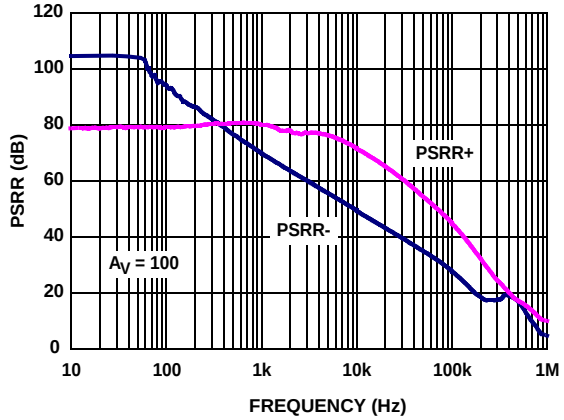


FIGURE 7. AMPLIFIER "A"(INAMP) PSRR vs FREQUENCY

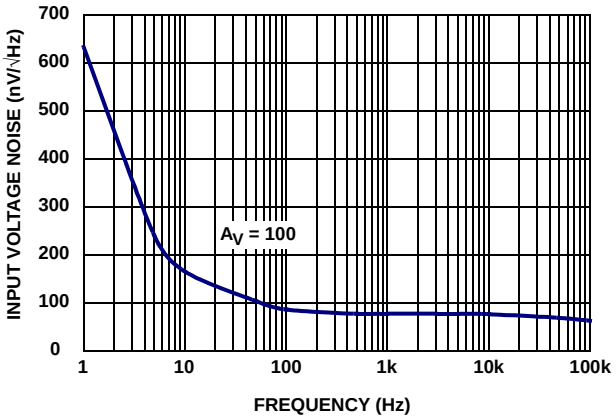


FIGURE 8. AMPLIFIER "A"(INAMP) INPUT VOLTAGE NOISE SPECTRAL DENSITY

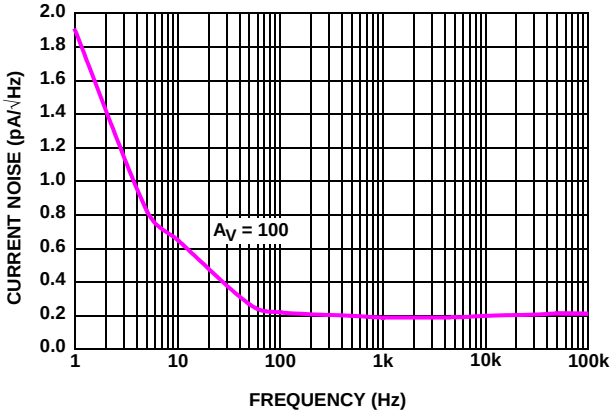


FIGURE 9. AMPLIFIER "A"(INAMP) INPUT CURRENT NOISE SPECTRAL DENSITY

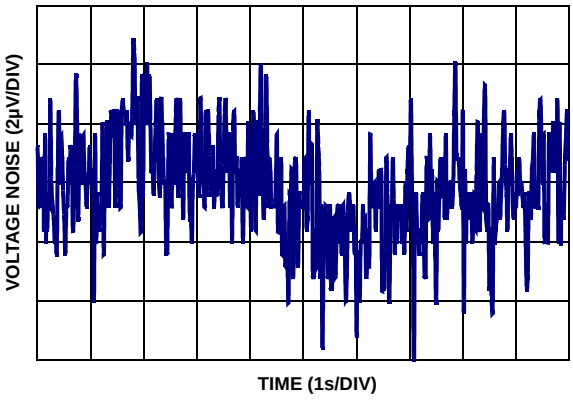


FIGURE 10. AMPLIFIER "A"(INAMP) 0.1 Hz TO 10Hz INPUT VOLTAGE NOISE

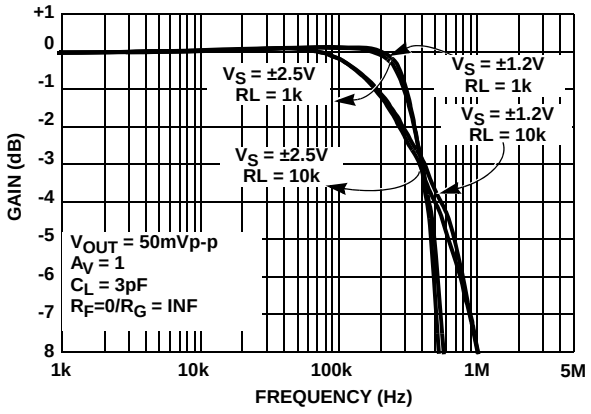


FIGURE 11. AMPLIFIER "B" (OP-AMP) FREQUENCY RESPONSE vs SUPPLY VOLTAGE

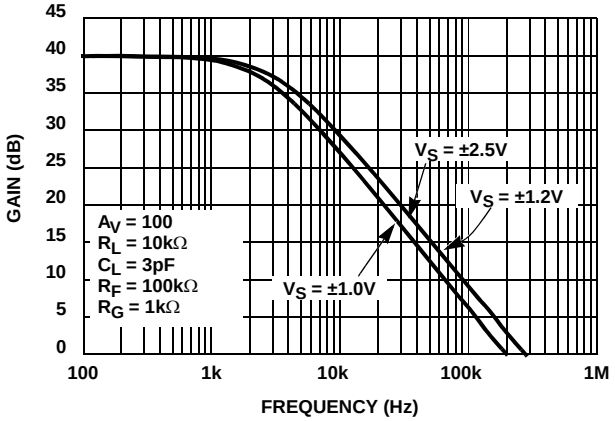


FIGURE 12. AMPLIFIER "B" (OP-AMP) FREQUENCY RESPONSE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

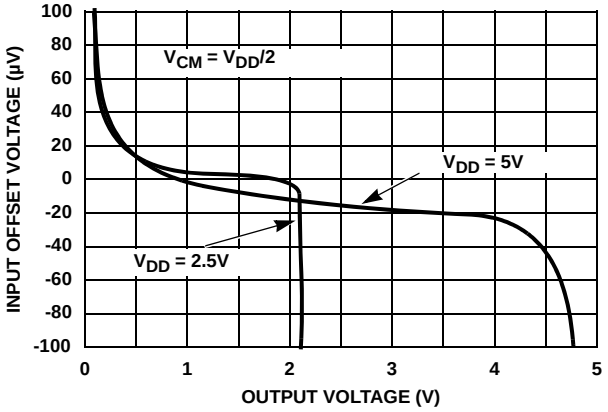


FIGURE 13. AMPLIFIER "B" (OP-AMP) INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

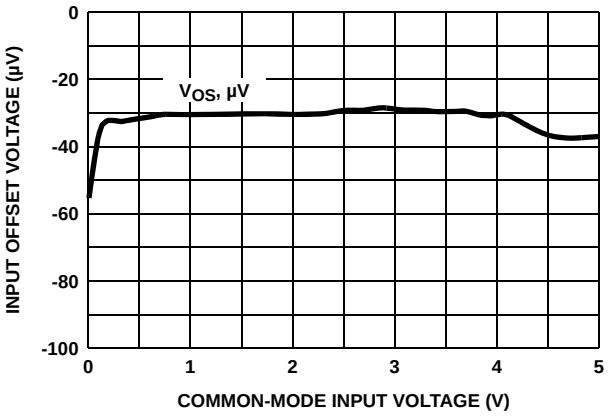


FIGURE 14. AMPLIFIER "B" (OP-AMP) INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

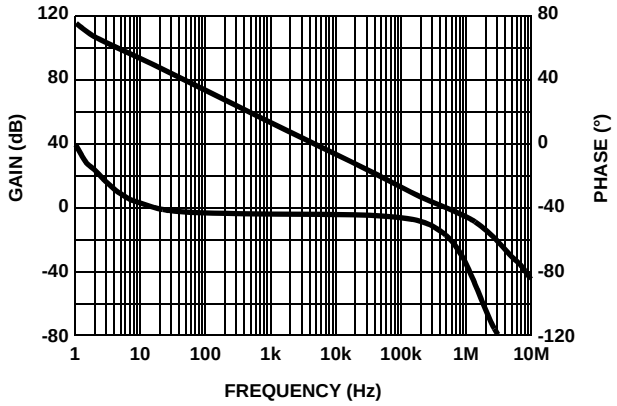


FIGURE 15. AMPLIFIER "B" (OP-AMP) A_{VOL} vs FREQUENCY @ 100kΩ LOAD

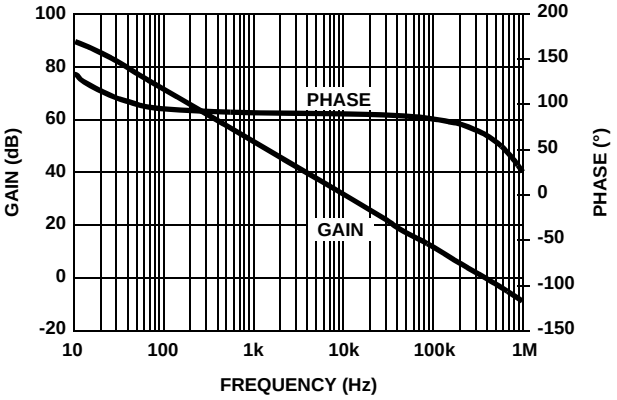


FIGURE 16. AMPLIFIER "B" (OP-AMP) A_{VOL} vs FREQUENCY @ 1kΩ LOAD

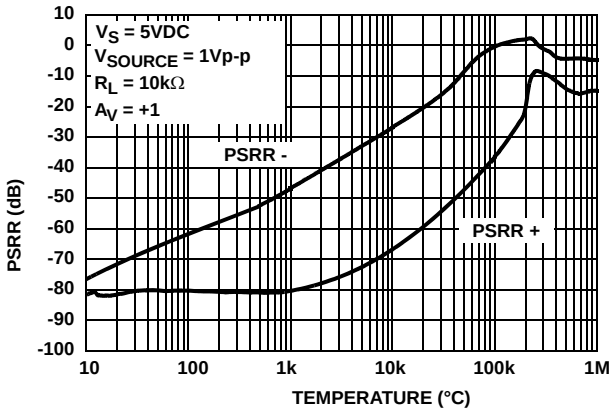


FIGURE 17. AMPLIFIER "B" (OP-AMP) PSRR vs FREQUENCY

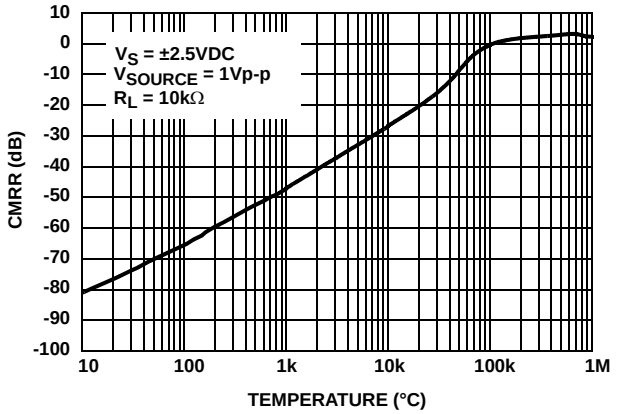


FIGURE 18. AMPLIFIER "B" (OP-AMP) CMRR vs FREQUENCY

Typical Performance Curves (Continued)

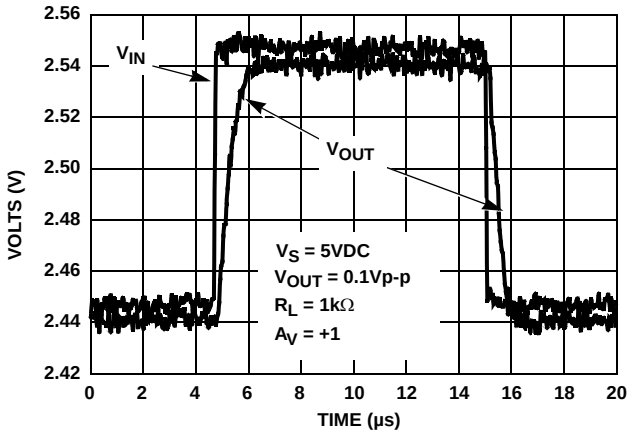


FIGURE 19. AMPLIFIER "B" (OP-AMP) SMALL SIGNAL TRANSIENT RESPONSE

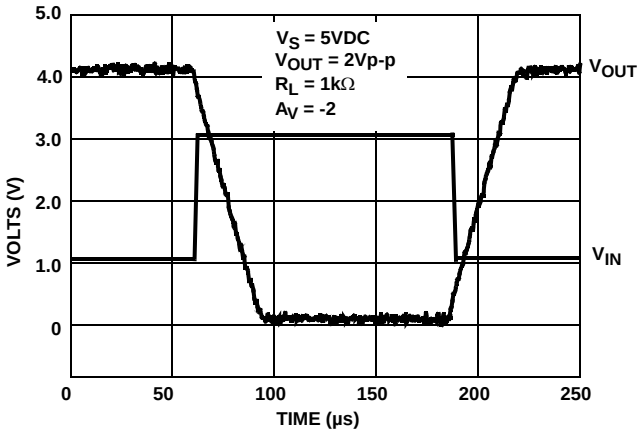


FIGURE 20. AMPLIFIER "B" (OP-AMP) LARGE SIGNAL TRANSIENT RESPONSE

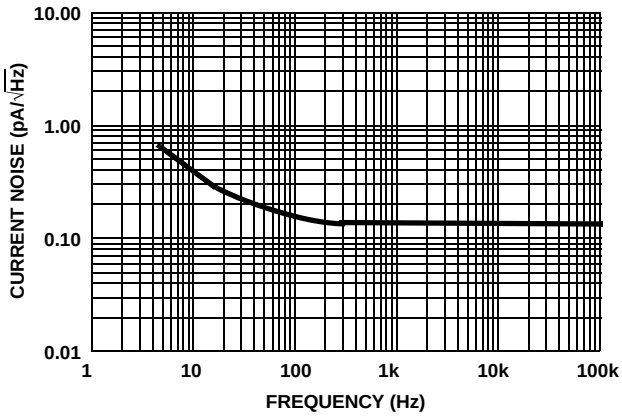


FIGURE 21. AMPLIFIER "B" (OP-AMP) CURRENT NOISE vs FREQUENCY

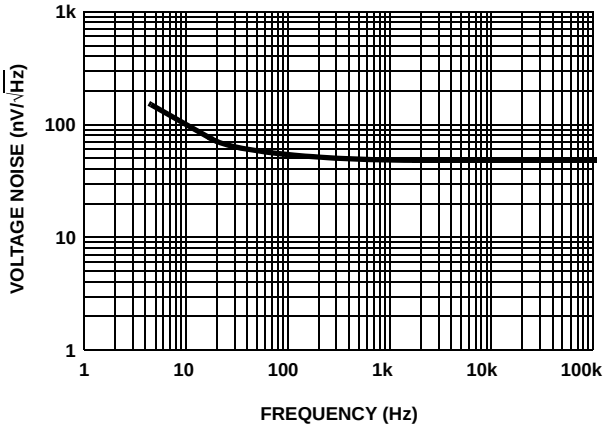


FIGURE 22. AMPLIFIER "B" (OP-AMP) VOLTAGE NOISE vs FREQUENCY

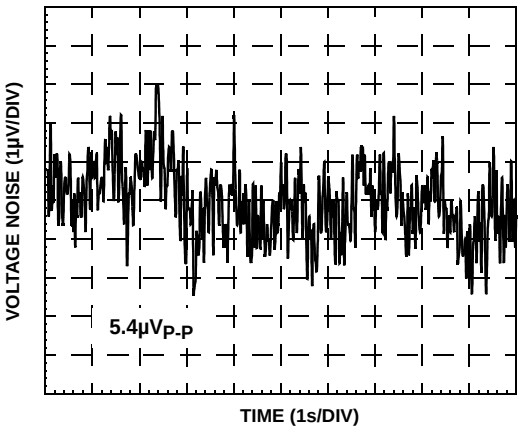


FIGURE 23. AMPLIFIER "B" (OP-AMP) 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

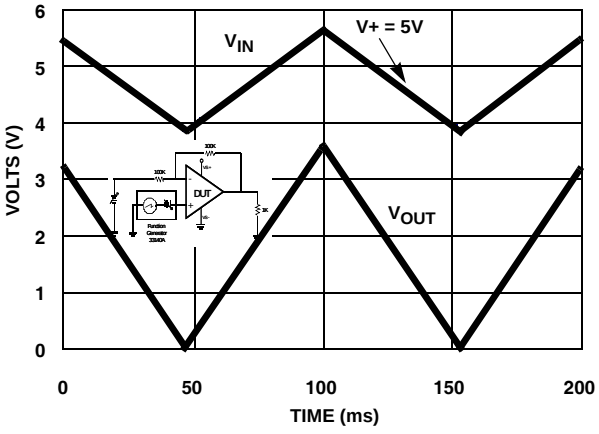


FIGURE 24. AMPLIFIER "B" (OP-AMP) INPUT VOLTAGE SWING ABOVE THE V+ SUPPLY

Typical Performance Curves (Continued)

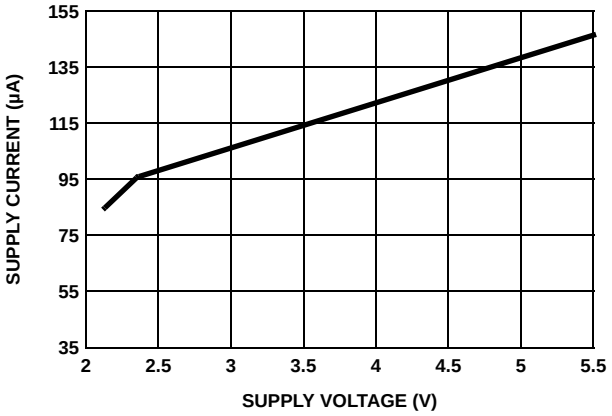


FIGURE 25. SUPPLY CURRENT vs SUPPLY VOLTAGE

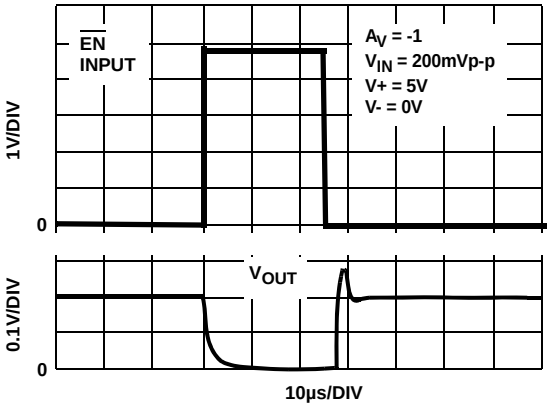


FIGURE 26. AMPLIFIER "B" (OP-AMP) ENABLE TO OUTPUT DELAY TIME

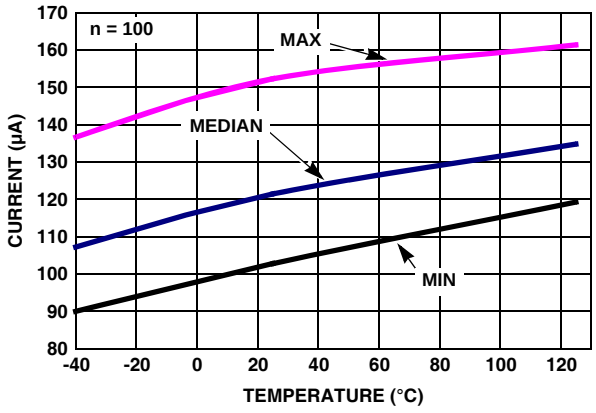


FIGURE 27. TOTAL SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

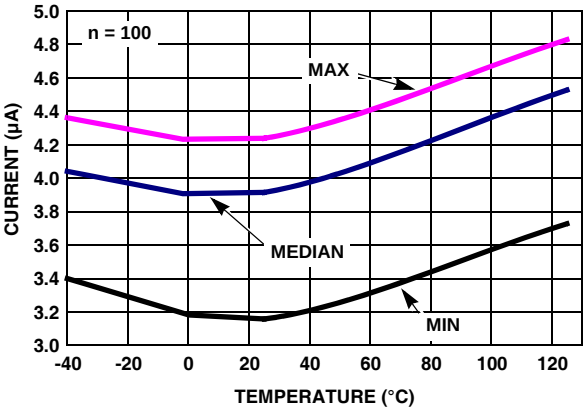


FIGURE 28. DISABLED POSITIVE SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V. R_L = INF

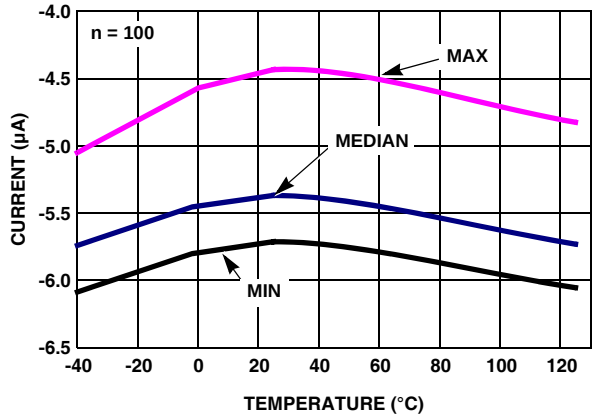


FIGURE 29. DISABLED NEGATIVE SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V. R_L = INF

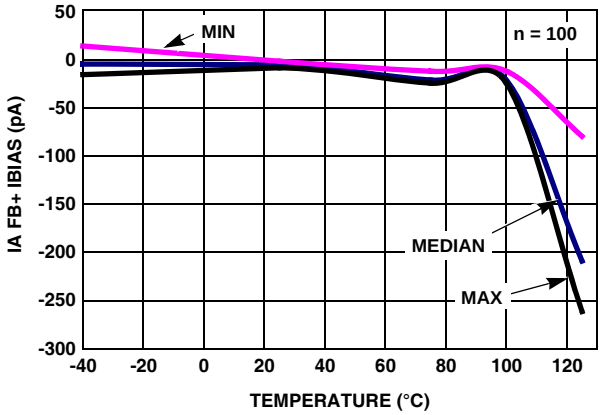


FIGURE 30. I BIAS (IA FB+) vs TEMPERATURE V_S = ±2.5V.

Typical Performance Curves (Continued)

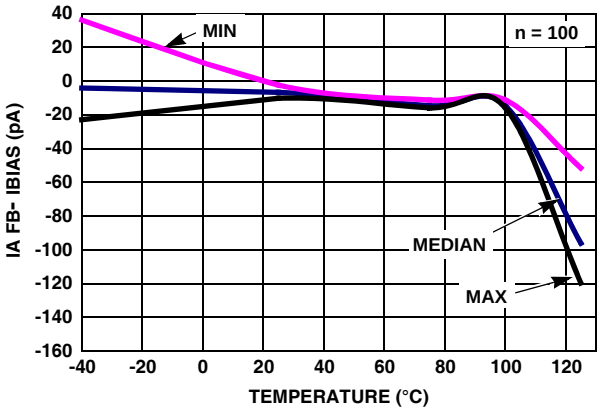


FIGURE 31. I BIAS (IA FB-) vs TEMPERATURE V_S = ±2.5V.

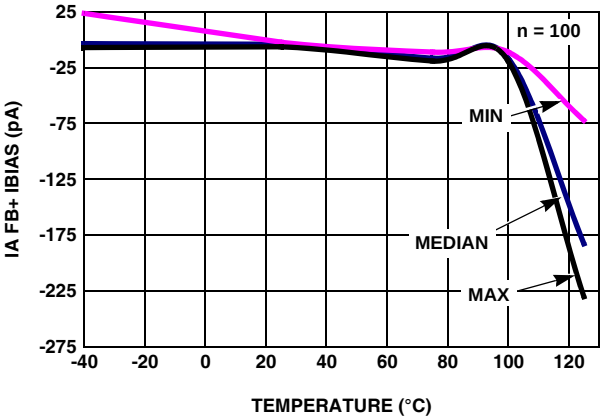


FIGURE 32. I BIAS (IA FB+) vs TEMPERATURE V_S = ±1.2V

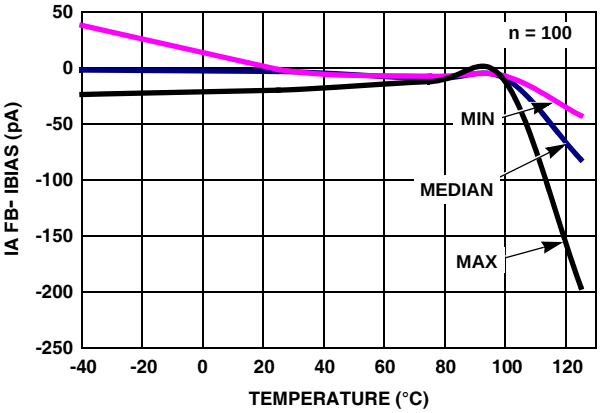


FIGURE 33. I BIAS (IA FB-) vs TEMPERATURE V_S = ±1.2V

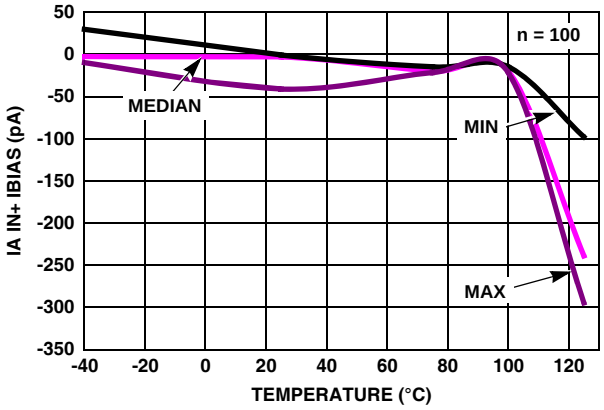


FIGURE 34. I BIAS (IA IN+) vs TEMPERATURE V_S = ±2.5V

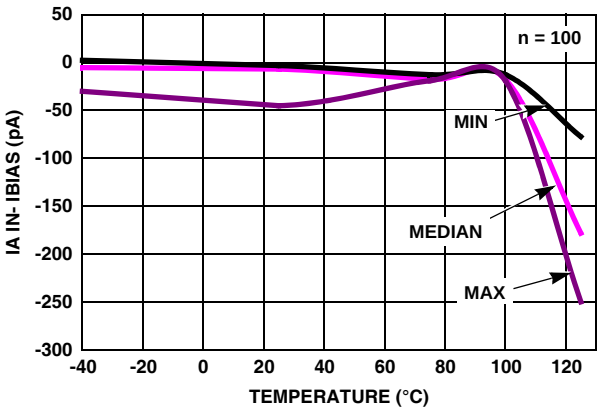


FIGURE 35. I BIAS (IA IN-) vs TEMPERATURE V_S = ±2.5V

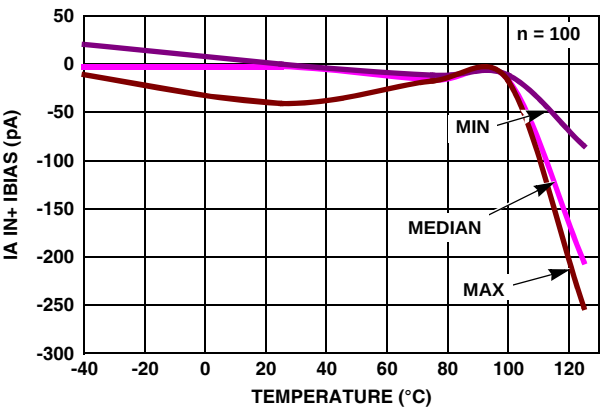


FIGURE 36. I BIAS (IA IN+) vs TEMPERATURE V_S = ±1.2V

Typical Performance Curves (Continued)

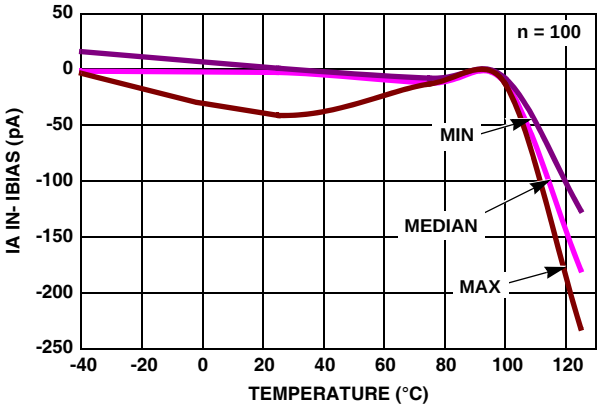


FIGURE 37. I BIAS (IA IN-) vs TEMPERATURE V_S = ±1.2V

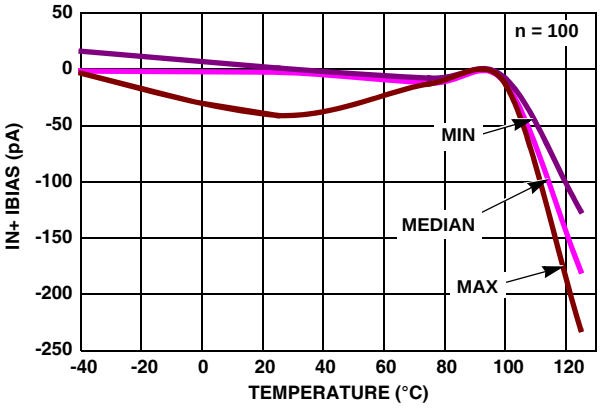


FIGURE 38. I BIAS(IN+) vs TEMPERATURE V_S = ±2.5V

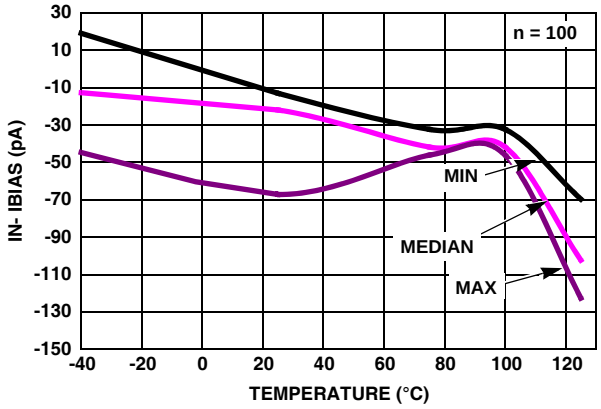


FIGURE 39. I BIAS(IN-) vs TEMPERATURE V_S = ±2.5V

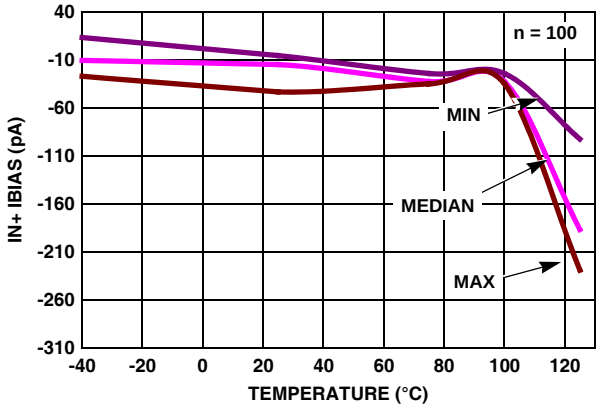


FIGURE 40. I BIAS(IN+) vs TEMPERATURE V_S = ±1.2V

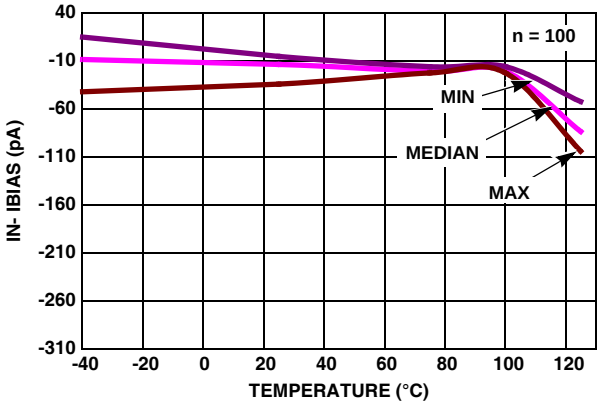


FIGURE 41. I BIAS(IN-) vs TEMPERATURE V_S = ±1.2V

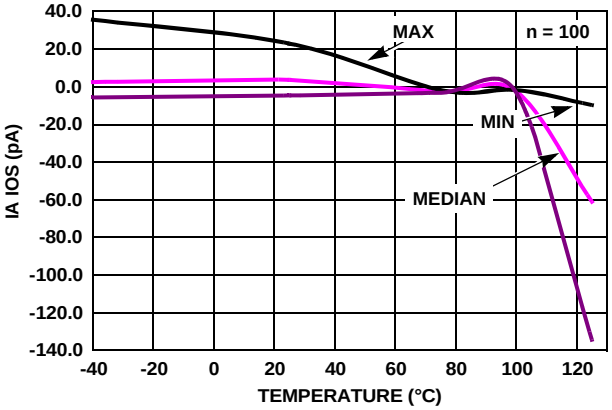


FIGURE 42. IA INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±2.5V

Typical Performance Curves (Continued)

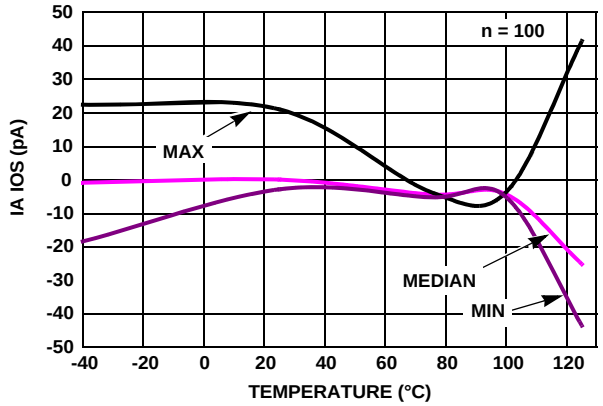


FIGURE 43. IA INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±1.2V

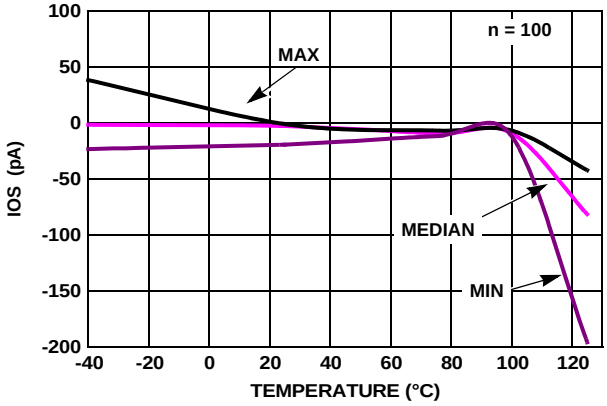


FIGURE 44. INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±2.5V

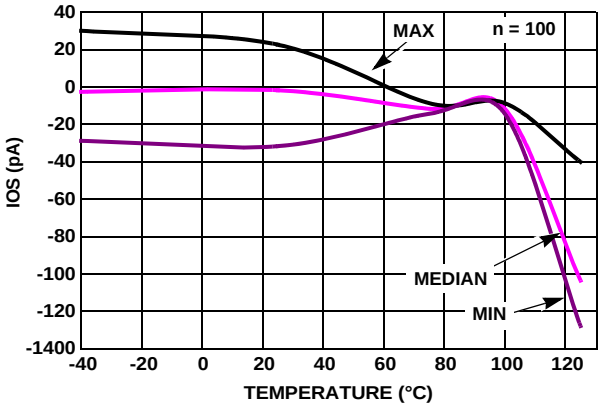


FIGURE 45. INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±1.2V

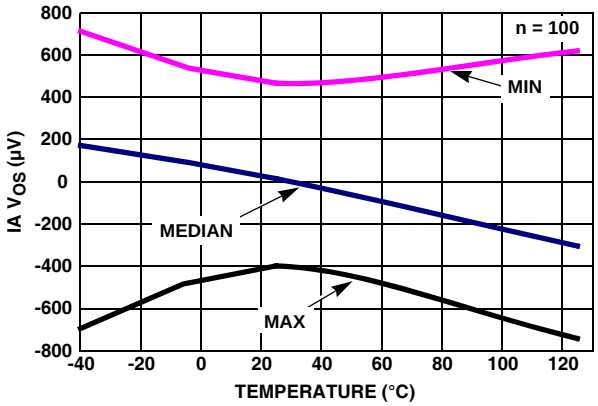


FIGURE 46. IA INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

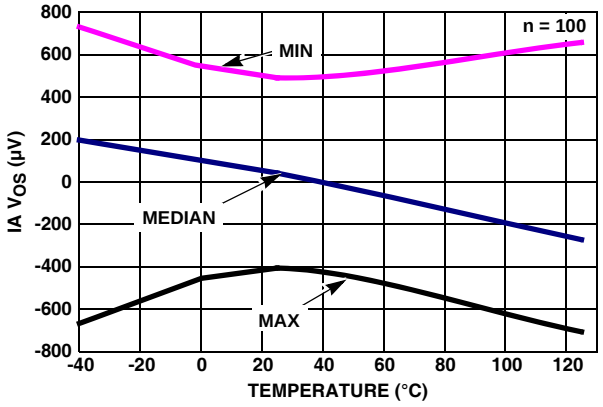


FIGURE 47. IA INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

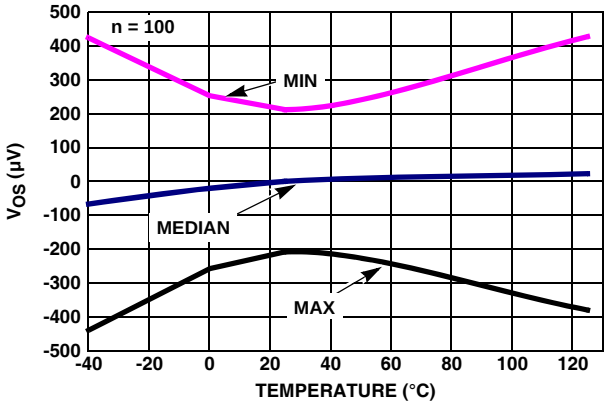


FIGURE 48. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

Typical Performance Curves (Continued)

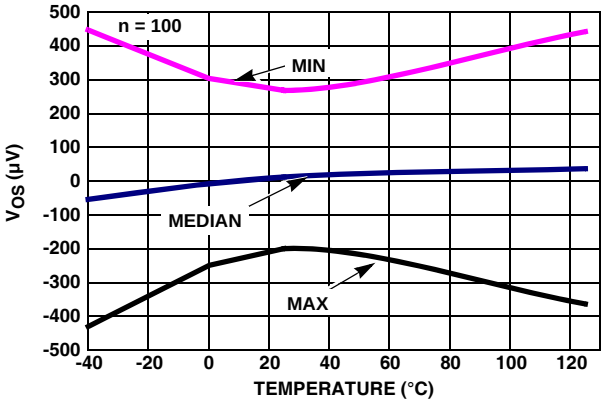


FIGURE 49. INPUT OFFSET VOLTAGE vs TEMPERATURE V_S = ±1.2V

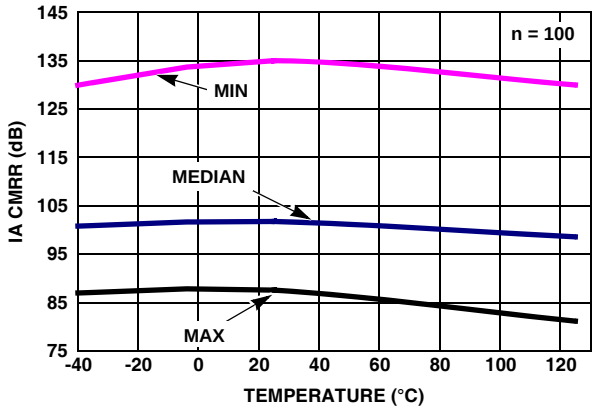


FIGURE 50. IA CMRR vs TEMPERATURE VCM = +2.5V TO -2.5V

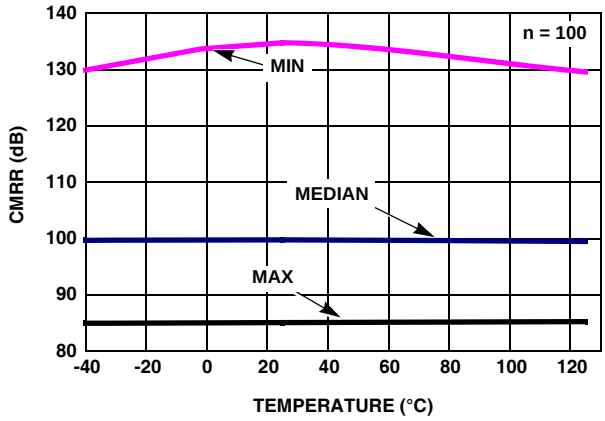


FIGURE 51. CMRR vs TEMPERATURE VCM = +2.5V TO -2.5V

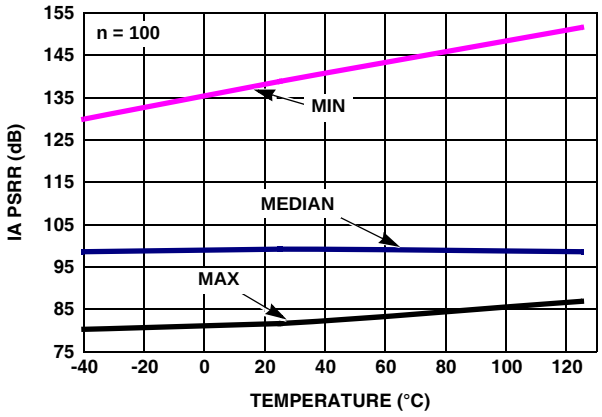


FIGURE 52. IA PSRR vs TEMPERATURE V_S = ±2.5V

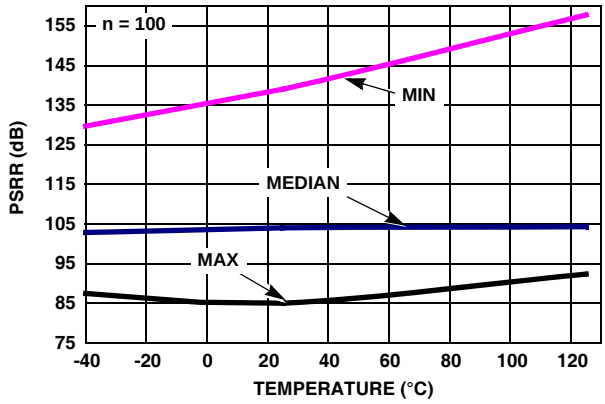


FIGURE 53. PSRR vs TEMPERATURE V_S = ±2.5V

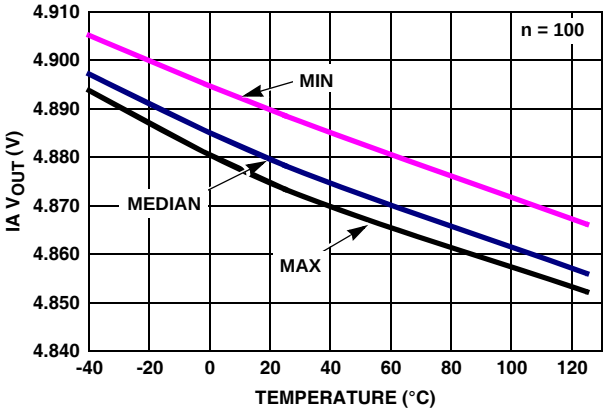


FIGURE 54. IA V_{OUT} HIGH vs TEMPERATURE R_L = 1k. V_S = ±2.5V

Typical Performance Curves (Continued)

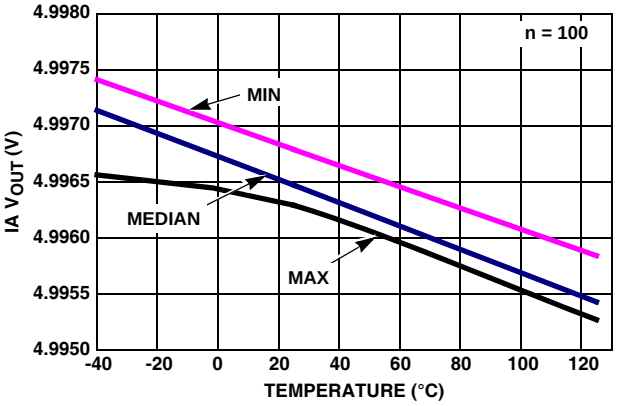


FIGURE 55. IA V_{OUT} HIGH vs TEMPERATURE R_L = 100k. V_S = ±2.5V

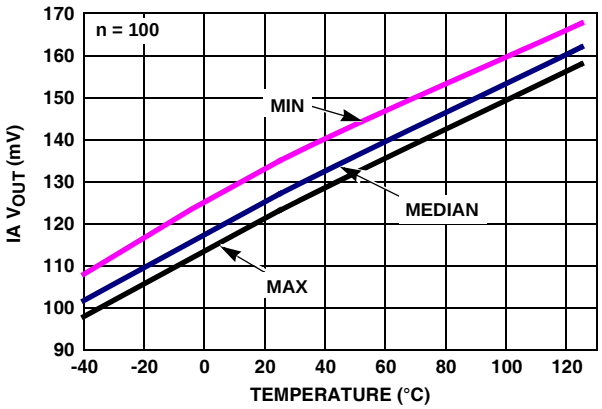


FIGURE 56. IA VOUT LOW vs TEMPERATURE R_L = 1k. V_S = ±2.5V

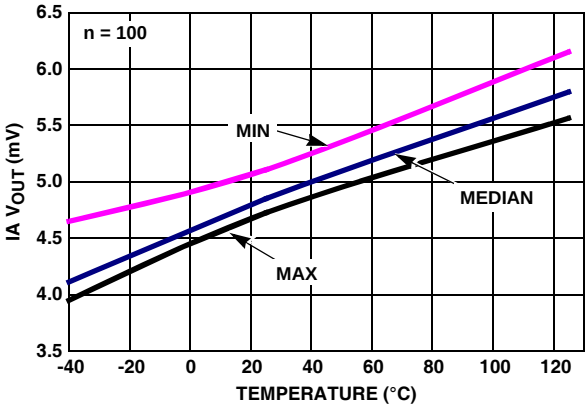


FIGURE 57. IA V_{OUT} LOW vs TEMPERATURE R_L = 100k. V_S = ±2.5V

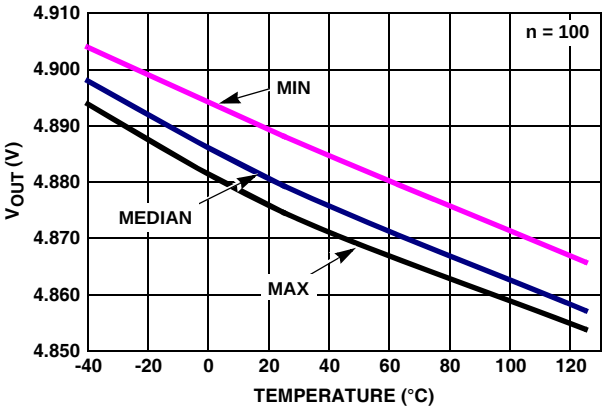


FIGURE 58. V_{OUT} HIGH vs TEMPERATURE R_L = 1k. V_S = ±2.5V

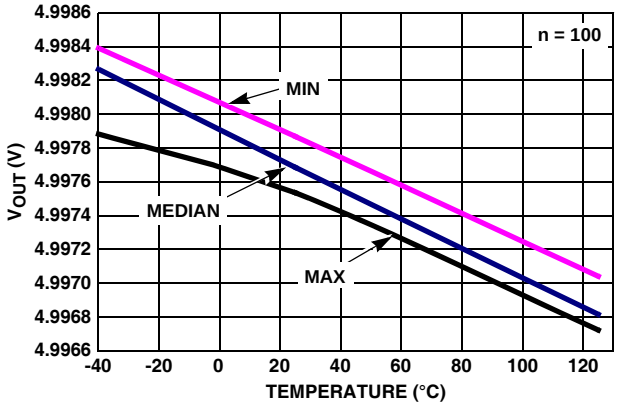


FIGURE 59. V_{OUT} HIGH vs TEMPERATURE R_L = 100k. V_S = ±2.5V

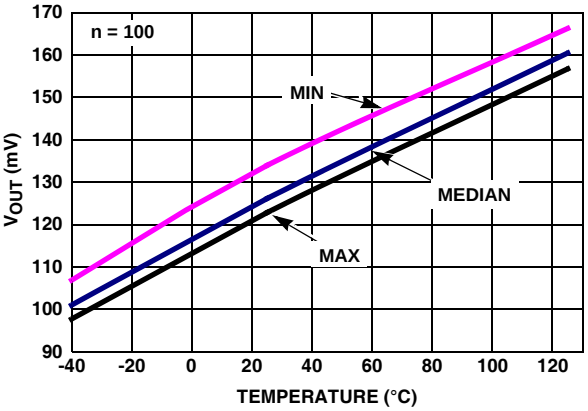


FIGURE 60. V_{OUT} LOW vs TEMPERATURE R_L = 1k. V_S = ±2.5V

Typical Performance Curves (Continued)

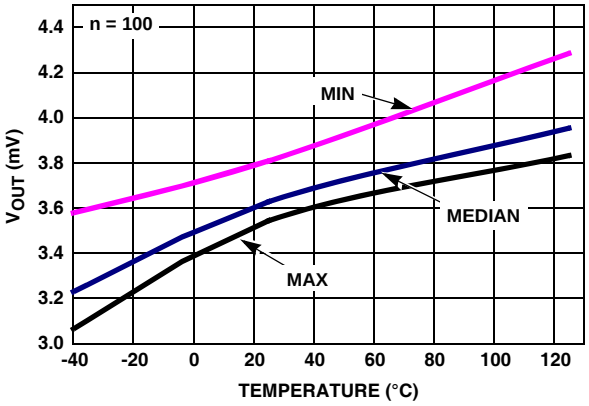
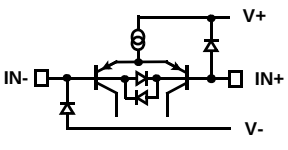


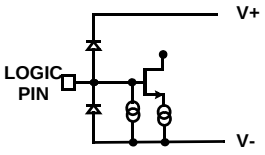
FIGURE 61. V_{OUT} LOW vs TEMPERATURE R_L = 100k. V_S = ±2.5V

Pin Descriptions

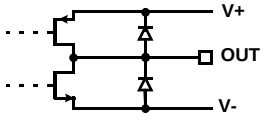
ISL28274 (16 LD QSOP)	ISL28474 (24 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1, 9, 13, 14	11, 14	NC		No internal connection
2	1, 24	IA OUT IA OUT_1/2	Circuit 3	Instrumentation Amplifier output
3	2, 23	IA FB+ IA FB+_1/2	Circuit 1	Instrumentation Amplifier Feedback from non-inverting output
4	3, 22	IA FB- IA FB-_1/2	Circuit 1	Instrumentation Amplifier Feedback from inverting output
5	4, 21	IA IN- IA IN-_1/2	Circuit 1	Instrumentation Amplifier inverting input
6	5, 20	IA IN+ IA IN+_1/2	Circuit 1	Instrumentation Amplifier non-inverting input
7	6, 19	IA $\overline{EN}$ IA $\overline{EN}$_1/2	Circuit 2	Instrumentation Amplifier enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
8	18	V-	Circuit 4	Negative power supply
10	8, 17	$\overline{EN}$ $\overline{EN}$ 1/2	Circuit 2	Amplifier enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
11	9, 16	IN+ IN+ 1/2	Circuit 1	Amplifier non-inverting input
12	10, 15	IN- IN- 1/2	Circuit 1	Amplifier inverting input
15	12, 13	OUT OUT 1/2	Circuit 3	Amplifier output
16	7	V+	Circuit 4	Positive power supply
IA = Instrumentation Amplifier				



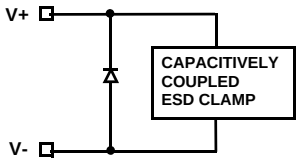
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Description of Operation and Application Information

Product Description

The ISL28274 and ISL28474 provide both a micropower instrumentation amplifier (Amp A) and a low power precision amplifier (Amp B) in the same package. The amplifiers deliver rail-to-rail input amplification and rail-to-rail output swing on a single 2.4V to 5V supply. They also deliver excellent DC and AC specifications while consuming only 60µA typical supply current per amplifier. Because the instrumentation amplifiers provide an independent pair of feedback terminals to set the gain and to adjust the output level, the in-amp achieve high common-mode rejection ratio regardless of the tolerance of the gain setting resistors. The instrumentation amplifier is internally compensated for a minimum closed loop gain of 100 or greater. An $\overline{EN}$ pin is used to reduce power consumption, typically 4µA for the ISL28274 and 8µA for the ISL28474, while both amplifiers are disabled. The user has independent control of each amplifier via separate $\overline{EN}$ pins.

Input Protection

The input and feedback terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode drop beyond the supply rails. If overdriving the inputs is necessary, the external input current must never exceed 5mA. External series resistor may be used as a protection to limit excessive external voltage and current from damaging the inputs.

Input Stage and Input Voltage Range

The input terminals (IN+ and IN-) of both amplifiers “A” and amp “B” are single differential pair P-MOSFET devices aided by an Input Range Enhancement Circuit to increase the headroom of operation of the common-mode input voltage. The feedback terminals (FB+ and FB-) of amplifier “A” also have a similar topology. As a result, the input common-mode voltage range is rail-to-rail. These amps are able to handle input voltages that are at or slightly beyond the supply and ground making them well suited for single 5V or 3.3V low voltage supply systems. There is no need then to move the common-mode input to achieve symmetrical input voltage.

Output Stage and Output Voltage Range

A pair of complementary MOSFET devices drives the output VOUT to within a few mV of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply, while the NMOS sinks current and pulls the output down to 3mV above the negative supply, or ground in the case of a single supply operation. The current sinking and sourcing capability of the ISL28274 are internally limited to 31mA.

Gain Setting of Instrumentation amp “A”

VIN, the potential difference across IN+ and IN-, is replicated (less the input offset voltage) across FB+ and FB-. The goal of the ISL28274 in-amp is to maintain the differential voltage across FB+ and FB- equal to IN+ and IN-; (FB+ - FB-) = (IN+ - IN-). Consequently, the transfer function can be derived. The gain is set by two external resistors, the feedback resistor RF, and the gain resistor RG.

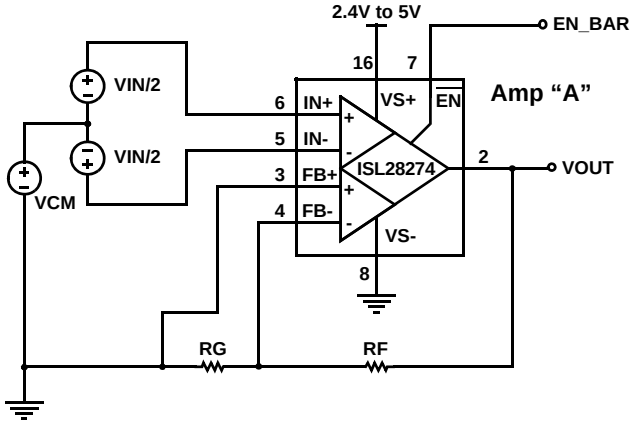


FIGURE 62. GAIN IS BY EXTERNAL RESISTORS R_F AND R_G

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)VIN$$

In Figure 62, the FB+ pin and one end of resistor RG are connected to GND. With this configuration, the above gain equation is only true for a positive swing in VIN; negative input swings will be ignored and the output will be at ground.

Reference Connection

Unlike a three-opamp instrumentation amplifier, a finite series resistance seen at the REF terminal does not degrade the high CMRR performance eliminating the need for an additional external buffer amplifier. Figure 63 uses the FB+ pin to provide a high impedance REF terminal.

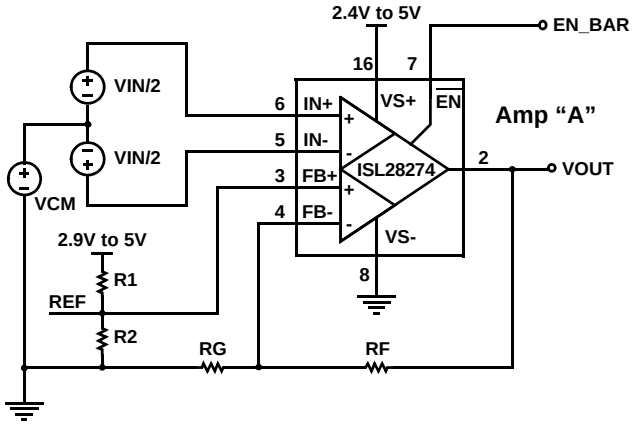


FIGURE 63. GAIN SETTING AND REFERENCE CONNECTION

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + \left(1 + \frac{R_F}{R_G}\right)(VREF)$$

The FB+ pin is used as a REF terminal to center or to adjust the output. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal without degrading or affecting the CMRR performance. Any voltage applied to the REF terminal will shift VOUT by VREF times the closed loop gain, which is set by resistors RF and RG as shown in Figure 63.

The FB+ pin can also be connected to the other end of resistor, RG. See Figure 64. Keeping the basic concept that the in-amps maintain constant differential voltage across the input terminals and feedback terminals (IN+ - IN- = FB+ - FB-), the transfer function of Figure 64 can be derived.

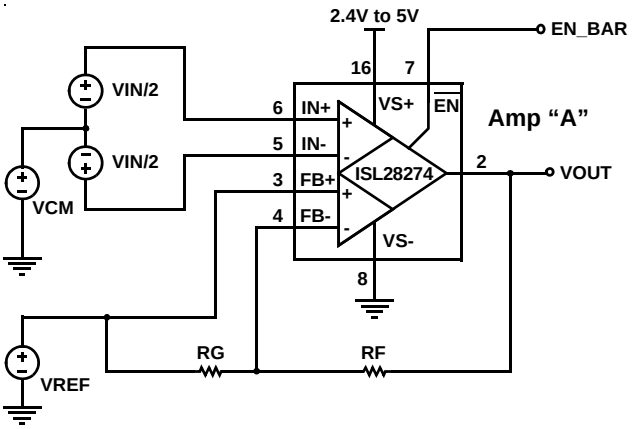


FIGURE 64. REFERENCE CONNECTION WITH AN AVAILABLE VREF

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + (VREF)$$

A finite resistance Rs in series with the VREF source, adds an output offset of VIN*(RS/RG). As the series resistance Rs approaches zero, the gain equation is simplified to the above equation for Figure 64. VOUT is simply shifted by an amount VREF.

External Resistor Mismatches

Because of the independent pair of feedback terminals provided by the ISL28274, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three opamp and especially a two opamp in-amp, the ISL28274 reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The ISL28274 CMRR will be 100dB regardless of the tolerance of the resistors used.

Disable/Power-Down

The ISL28274 Amplifiers “A” and “B” can be powered down reducing the supply current to typically 4µA. When disabled, the output is in a high impedance state. The active low $\overline{EN}$ bar pin has an internal pull down and hence can be left floating and the in-amp and Opamp enabled by default. When the $\overline{EN}$ bar is connected to an external logic, the amplifiers will power down when $\overline{EN}$ bar is pulled above 2V, and will power on when $\overline{EN}$ bar is pulled below 0.8V.

Using Only the Instrumentation Amplifier

If the application only requires the instrumentation amp, the user must configure the unused Opamp to prevent it from oscillating. The unused Opamp will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the in-amp. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 65).

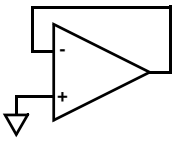


FIGURE 65. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 66 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

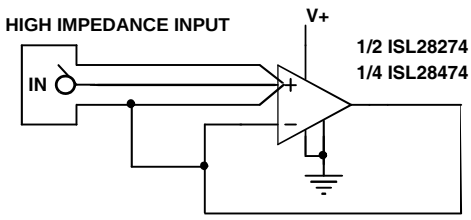


FIGURE 66. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Current Limiting

The ISL28274 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

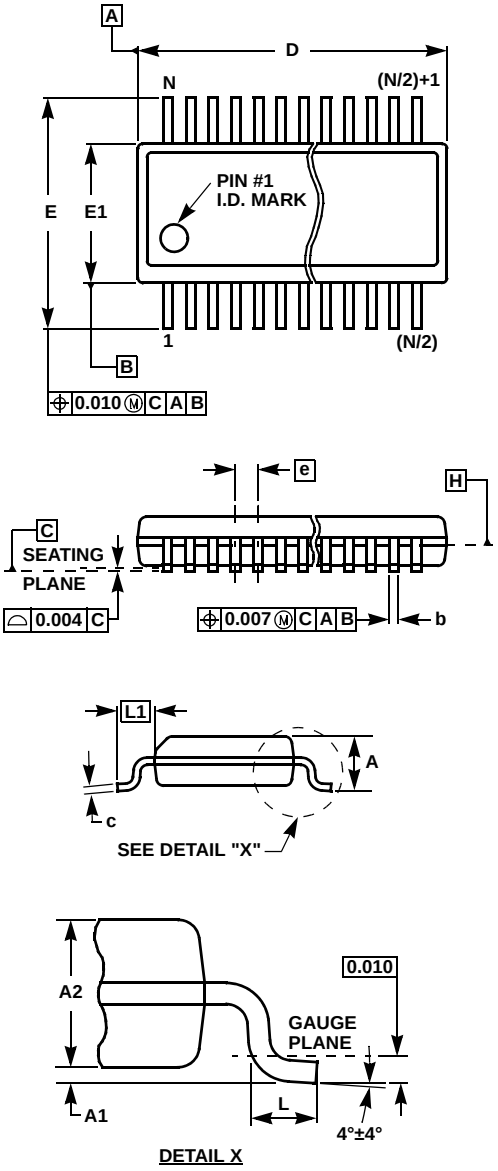
- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as shown in Equation 2:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	QSOP16	QSOP24	QSOP28	TOLERANCE	NOTES
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.