

40V Precision Low Power Operational Amplifiers

ISL28117, ISL28217

The ISL28117 and ISL28217 are a family of very high precision amplifiers featuring low noise vs power consumption, low offset voltage, low I_BI_AS current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28117 single and ISL28217 dual are offered in an 8 Ld SOIC package. Both devices are offered in standard pin configurations and operate over the extended temperature range to -40°C to +125°C.

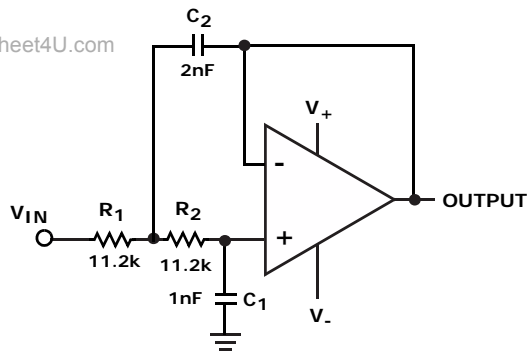
Features

- Low Input Offset ±50μV, Max.
- Superb Offset TC 0.6μV/°C, Max.
- Input Bias Current ±1nA, Max.
- Input Bias Current TC ±5pA/°C, Max.
- Low Current Consumption 440μA
- Voltage Noise 8nV/Hz
- Wide Supply Range 4.5V to 40V
- Operating Temperature Range . . -40°C to +125°C
- Small Package Offerings in Single and Dual
- Pb-Free (RoHS Compliant)

Applications* (see page 17)

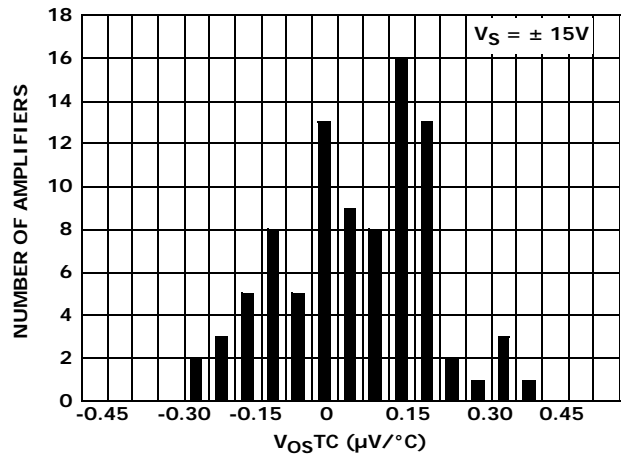
- Precision Instruments
- Medical Instrumentation
- Spectral Analysis Equipment
- Active Filter Blocks
- Thermocouples and RTD Reference Buffers
- Data Acquisition
- Power Supply Control

Typical Application



Sallen-Key Low Pass Filter (10kHz)

V_{os} Temperature Coefficient (V_{os}TC)



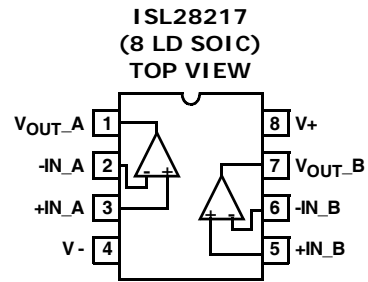
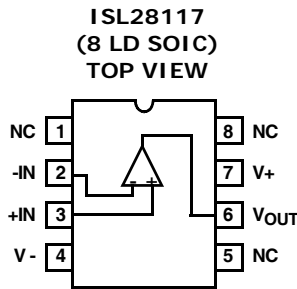
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V _{OS} (MAX) (μ V)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28117FBBZ	28117 -B FBZ	50 (B Grade)	8 Ld SOIC	M8.15E
ISL28117FBZ	28117 FBZ	100 (C Grade)	8 Ld SOIC	M8.15E
ISL28217FBBZ	28217-B FBZ	50 (B Grade)	8 Ld SOIC	M8.15E
ISL28217FBZ	28217 FBZ	100 (C Grade)	8 Ld SOIC	M8.15E

NOTES:

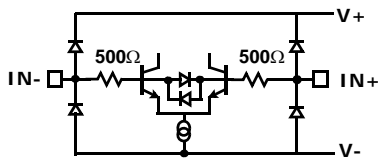
1. Add "-T7" or "-T13" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL28117](#), [ISL28217](#). For more information on MSL please see techbrief [TB363](#).

Pin Configurations

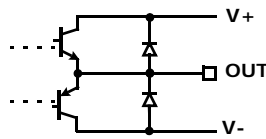


Pin Descriptions

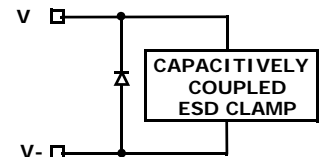
ISL28117 (8 LD SOIC)	ISL28217 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	+IN +IN_A	Circuit 1	Amplifier A non-inverting input
	4	V-	Circuit 3	Negative power supply
	5	+IN_B	Circuit 1	Amplifier B non-inverting input
	6	-IN_B	Circuit 1	Amplifier B inverting input
	7	V _{OUT_B}	Circuit 2	Amplifier B output
7	8	V+	Circuit 3	Positive power supply
6	1	V _{OUT} V _{OUT_A}	Circuit 2	Amplifier A output
2	2	-IN -IN_A	Circuit 1	Amplifier A inverting input
1, 5, 8		NC	-	No internal connection



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage	42V
Maximum Differential Input Current	20mA
Maximum Differential Input Voltage	42V
Min/Max Input Voltage	V- - 0.5V to V+ + 0.5V
Max/Min Input current for Input Voltage >V+ or <V-	±20mA
Output Short-Circuit Duration (1 output at a time)	Indefinite
ESD Rating	
Human Body Model	4.5kV
Machine Model	500V
Charged Device Model	1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
8 Ld SOIC ISL28117 (Note 4)	120
8 Ld SOIC ISL28217 (Note 4)	115
Maximum Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature (T_{JMAX})	+150°C
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range (T_A)	-40°C to +125°C
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CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OS}	Input Offset Voltage	ISL28x17 B Grade	-50	13	50	μV
			-110		110	μV
		ISL28x17 C Grade	-100	19	100	μV
			-190		190	μV
V_{OSTC}	Input Offset Voltage Temperature Coefficient	ISL28x17 B Grade	-0.6	0.14	0.6	$\mu V/C$
		ISL28x17 C Grade	-0.9	0.14	0.9	$\mu V/C$
I_B	Input Bias Current		-1	0.18	1	nA
			-1.5		1.5	nA
I_{BTC}	Input Bias Current Temperature Coefficient		-5	1	5	$\mu A/C$
I_{OS}	Input Offset Current		-1.5	0.3	1.5	nA
			-1.85		1.85	nA
I_{OSTC}	Input Offset Current Temperature Coefficient		-3	0.42	3	$\mu A/C$
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	-13		13	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -13V$ to $+13V$	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25V$ to $\pm 20V$	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	$V_O = -13V$ to $+13V$, $R_L = 10k\Omega$ to ground	3,000	18,000		V/mV
V_{OH}	Output Voltage High	$R_L = 10k\Omega$ to ground	13.5	13.7		V
			13.2			V
		$R_L = 2k\Omega$ to ground	13.3	13.55		V
			13.1			V

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OL}	Output Voltage Low	$R_L = 10k\Omega$ to ground		-13.7	-13.5	V
					-13.2	V
		$R_L = 2k\Omega$ to ground		-13.55	-13.3	V
					-13.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	± 2.25		± 20	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	$A_V = 1k$, $R_L = 2k\Omega$		1.5		MHz
e_{nVp-p}	Voltage Noise V_{p-p}	0.1Hz to 10Hz		0.25		μV_{p-p}
e_n	Voltage Noise Density	$f = 10Hz$		10		nV/\sqrt{Hz}
e_n	Voltage Noise Density	$f = 100Hz$		8.2		nV/\sqrt{Hz}
e_n	Voltage Noise Density	$f = 1kHz$		8		nV/\sqrt{Hz}
e_n	Voltage Noise Density	$f = 10kHz$		8		nV/\sqrt{Hz}
i_n	Current Noise Density	$f = 1kHz$		0.1		pA/\sqrt{Hz}
THD + N	Total Harmonic Distortion	1kHz, $G = 1$, $V_O = 3.5V_{RMS}$, $R_L = 2k\Omega$		0.0009		%
		1kHz, $G = 1$, $V_O = 3.5V_{RMS}$, $R_L = 10k\Omega$		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	$A_V = 11$, $R_L = 2k\Omega$, $V_O = 4V_{p-p}$		0.5		$V/\mu s$
t_r , t_f Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{p-p}$, $R_L = 10k\Omega$ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{p-p}$, $R_L = 10k\Omega$ to V_{CM}		120		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{p-p}$, $R_L = 5k\Omega$ to V_{CM}		21		μs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{p-p}$, $R_L = 5k\Omega$ to V_{CM}		24		μs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{p-p}$, $R_L = 5k\Omega$ to V_{CM}		13		μs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{p-p}$, $R_L = 5k\Omega$ to V_{CM}		18		μs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{p-p}$, $R_L = 2k\Omega$ to V_{CM}		5.6		μs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{p-p}$, $R_L = 2k\Omega$ to V_{CM}		10.6		μs

Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OS}	Input Offset Voltage	ISL28x17 B Grade	-50	13	50	μV
			-110		110	μV
		ISL28x17 C Grade	-100	19	100	μV
			-190		190	μV
V_{OSTC}	Input Offset Voltage Temperature Coefficient	ISL28x17 B Grade	-0.6	0.14	0.6	$\mu V/C$
		ISL28x17 C Grade	-0.9	0.14	0.9	$\mu V/C$
I_B	Input Bias Current		-1	0.18	1	nA
			-1.5		1.5	nA
I_{BTC}	Input Bias Current Temperature Coefficient		-5	1	5	pA/C
I_{OS}	Input Offset Current		-1.5	0.3	1.5	nA
			-1.85		1.85	nA
I_{OSTC}	Input Offset Current Temperature Coefficient		-3	0.42	3	pA/C
V_{CM}	Input Voltage Range		-3		3	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -3V$ to $+3V$	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25V$ to $\pm 5V$	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	$V_O = -3.0V$ to $+3.0V$ $R_L = 10k\Omega$ to ground	3,000	18,000		V/mV
V_{OH}	Output Voltage High	$R_L = 10k\Omega$ to ground	3.5	3.7		V
			3.2			V
		$R_L = 2k\Omega$ to ground	3.3	3.55		V
			3.1			V
V_{OL}	Output Voltage Low	$R_L = 10k\Omega$ to ground		-3.7	-3.5	V
					-3.2	V
		$R_L = 2k\Omega$ to ground		-3.55	-3.3	V
					-3.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	$A_V = 1k$, $R_L = 2k\Omega$		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		μV_{p-p}
e_n	Voltage Noise Density	$f = 10Hz$		12		nV/ \sqrt{Hz}
e_n	Voltage Noise Density	$f = 100Hz$		8.6		nV/ \sqrt{Hz}
e_n	Voltage Noise Density	$f = 1kHz$		8		nV/ \sqrt{Hz}

Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0V$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
e_n	Voltage Noise Density	$f = 10kHz$		8		nV/\sqrt{Hz}
i_n	Current Noise Density	$f = 1kHz$		0.1		pA/\sqrt{Hz}
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	$A_V = 11$, $R_L = 2k\Omega$, $V_O = 4V_{P-P}$		0.5		$V/\mu s$
t_r , t_f , Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$ $R_L = 10k\Omega$ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$ $R_L = 10k\Omega$ to V_{CM}		120		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$ $R_L = 5k\Omega$ to V_{CM}		12		μs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$ $R_L = 5k\Omega$ to V_{CM}		19		μs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$ $R_L = 2k\Omega$ to V_{CM}		7		μs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$ $R_L = 2k\Omega$ to V_{CM}		5.8		μs

NOTE:

- 5. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified.

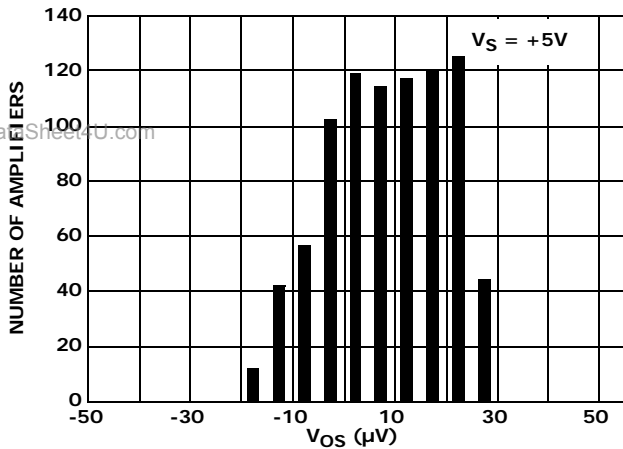


FIGURE 1. V_{OS} DISTRIBUTION for GRADE B

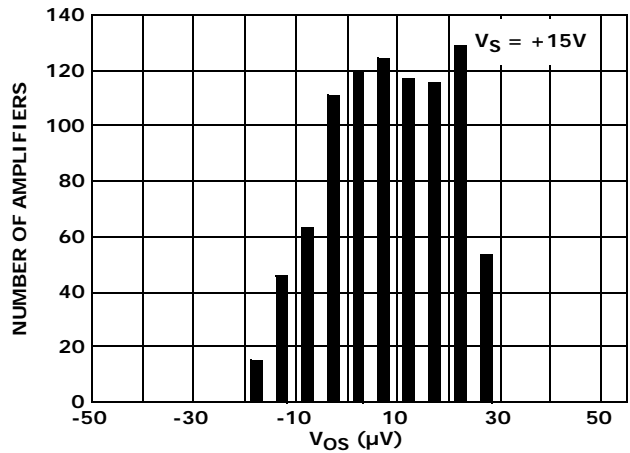


FIGURE 2. V_{OS} DISTRIBUTION FOR GRADE B

Typical Performance Curves

$V_S = \pm 15V, V_{CM} = 0V, R_L = \text{Open}$, unless otherwise specified. (Continued)

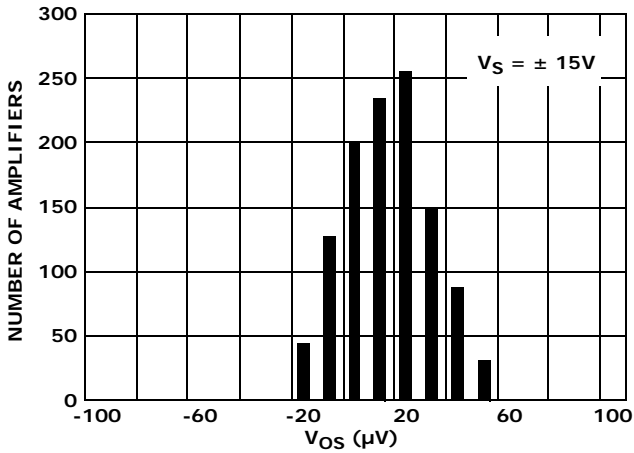


FIGURE 3. V_{OS} DISTRIBUTION FOR GRADE C

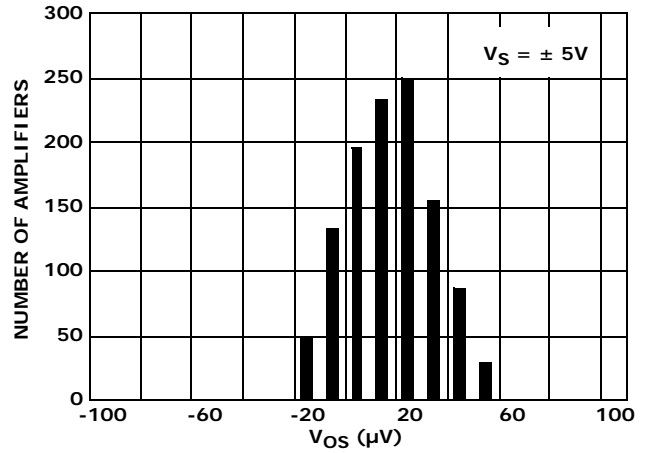


FIGURE 4. V_{OS} DISTRIBUTION FOR GRADE C

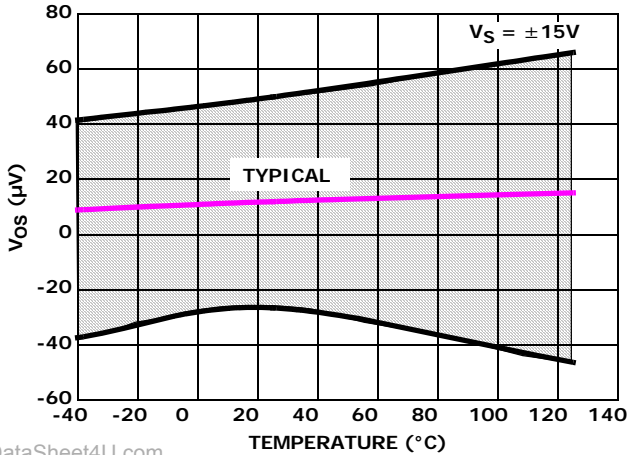


FIGURE 5. V_{OS} RANGE vs TEMPERATURE

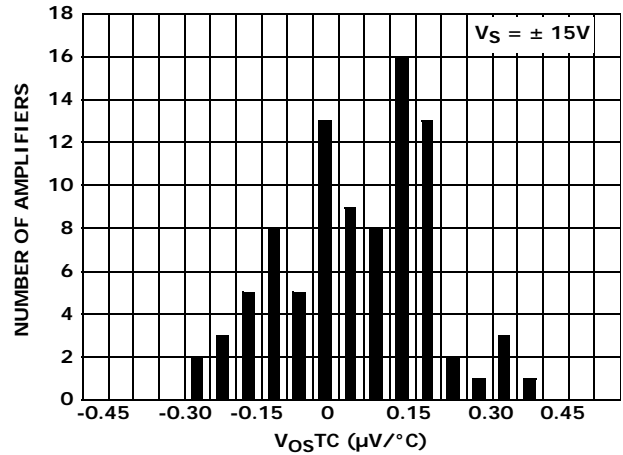


FIGURE 6. TCV_{OS} vs NUMBER OF AMPLIFIERS

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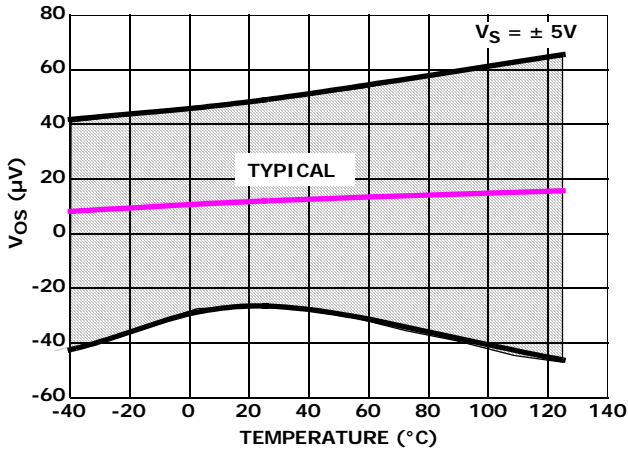


FIGURE 7. V_{OS} RANGE vs TEMPERATURE

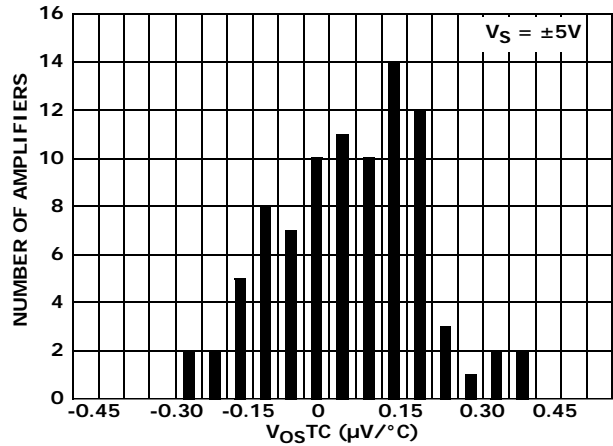


FIGURE 8. TCV_{OS} vs NUMBER OF AMPLIFIERS

Typical Performance Curves $V_S = \pm 15V, V_{CM} = 0V, R_L = \text{Open}$, unless otherwise specified. (Continued)

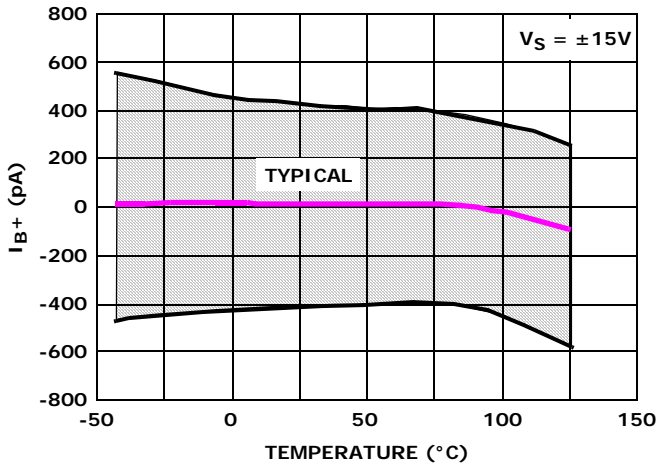


FIGURE 9. I_{B+} RANGE vs TEMPERATURE

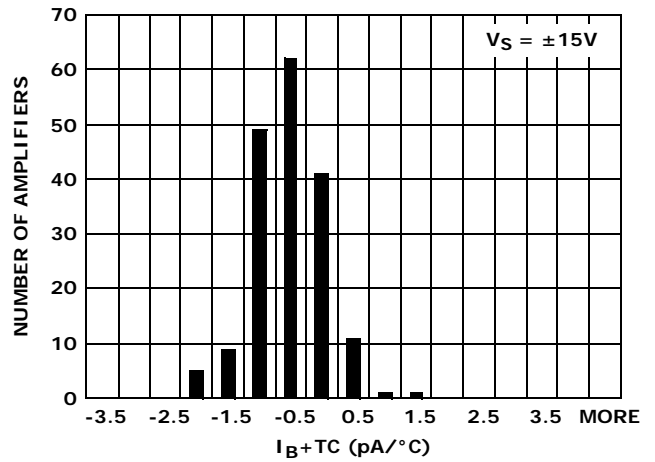


FIGURE 10. TCI_{B+} vs NUMBER OF AMPLIFIERS

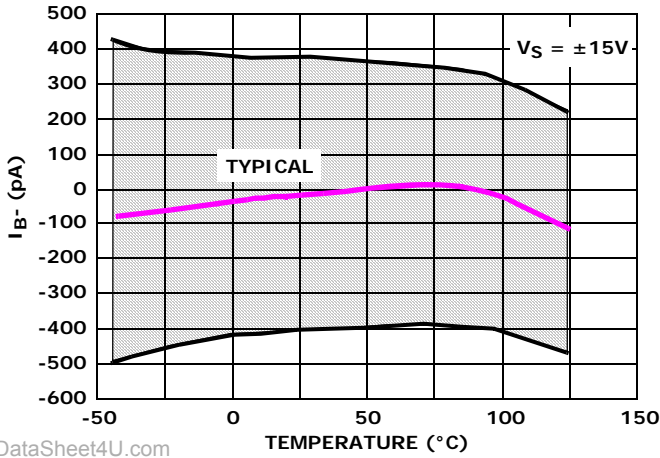


FIGURE 11. I_{B-} RANGE vs TEMPERATURE

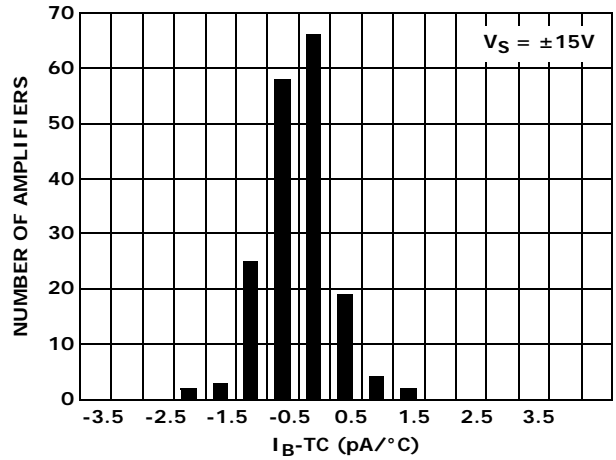


FIGURE 12. TCI_{B-} vs NUMBER OF AMPLIFIERS

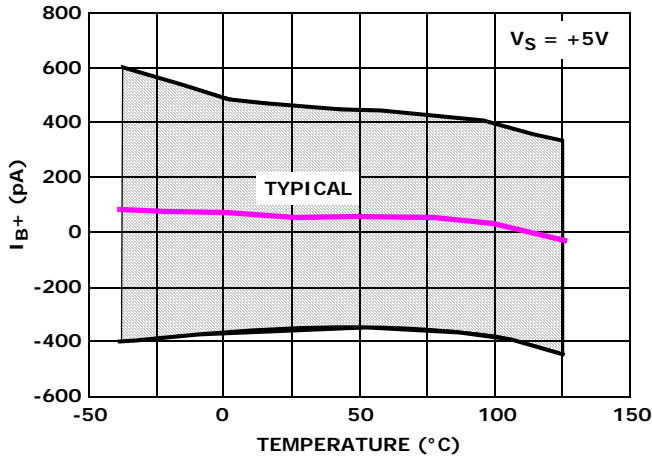


FIGURE 13. I_{B+} RANGE vs TEMPERATURE

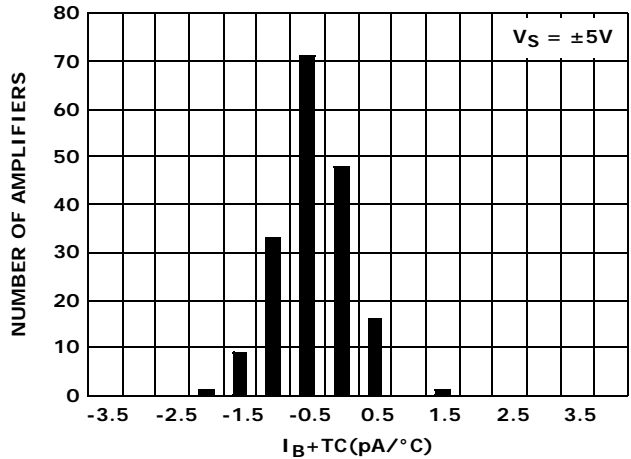


FIGURE 14. I_{BTC+} vs NUMBER OF AMPLIFIERS

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Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

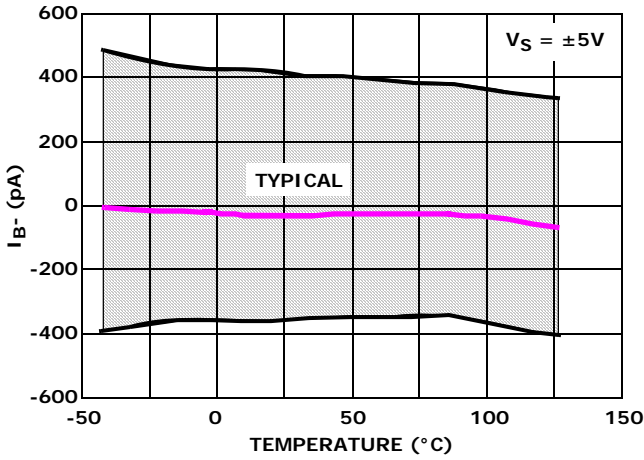


FIGURE 15. I_{B-} RANGE vs TEMPERATURE

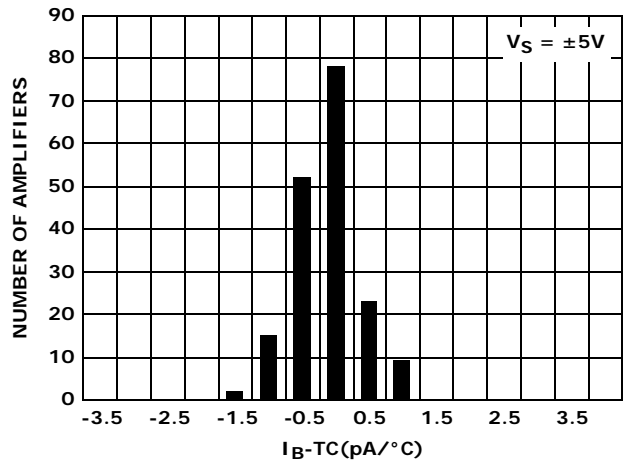


FIGURE 16. I_{BTC-} vs NUMBER OF AMPLIFIERS

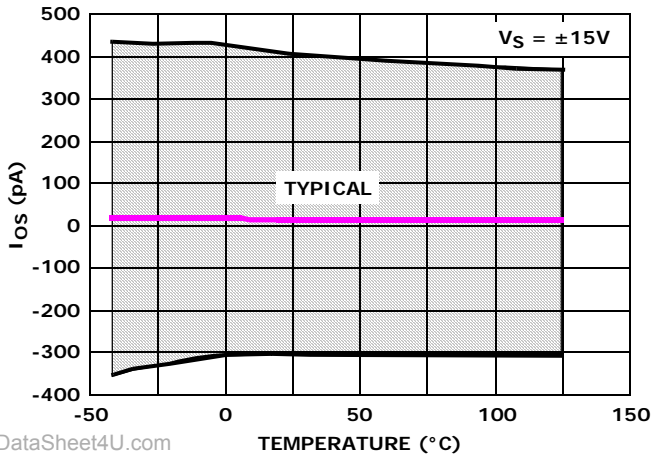


FIGURE 17. I_{OS} RANGE vs TEMPERATURE

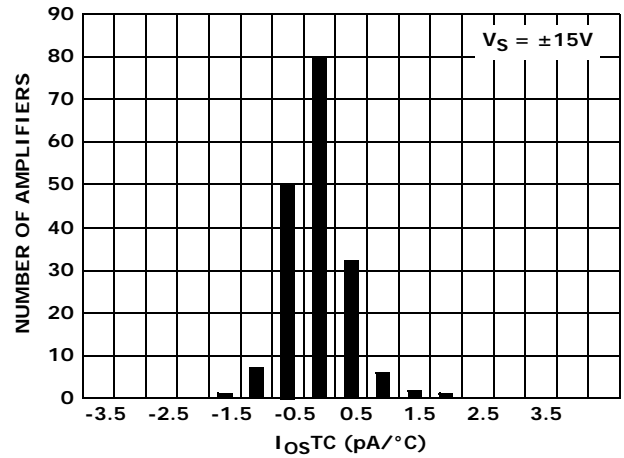


FIGURE 18. I_{OSTC} vs NUMBER OF AMPLIFIERS

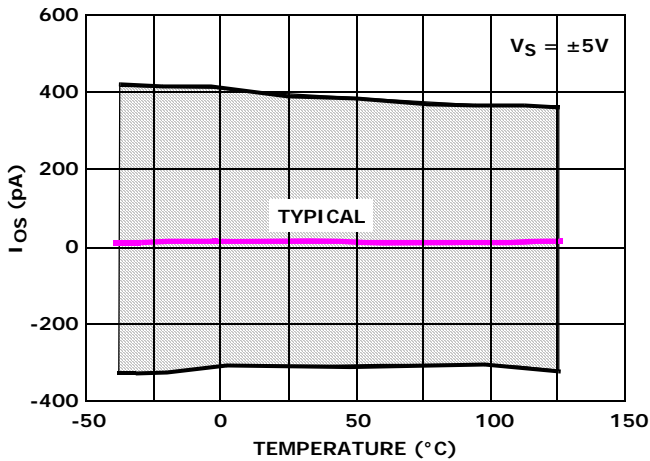


FIGURE 19. I_{OS} RANGE vs TEMPERATURE

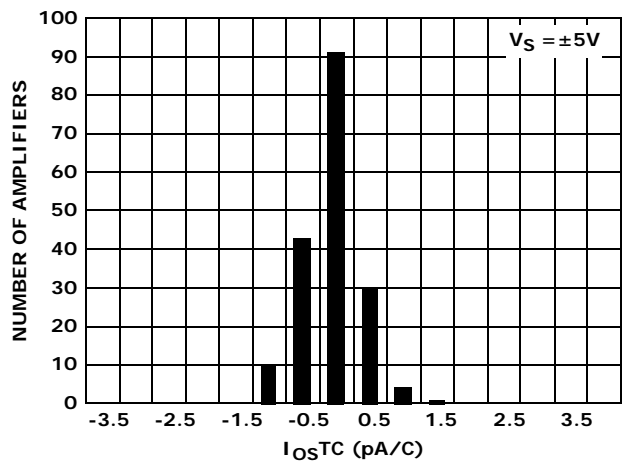


FIGURE 20. I_{OSTC} vs NUMBER OF AMPLIFIERS

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

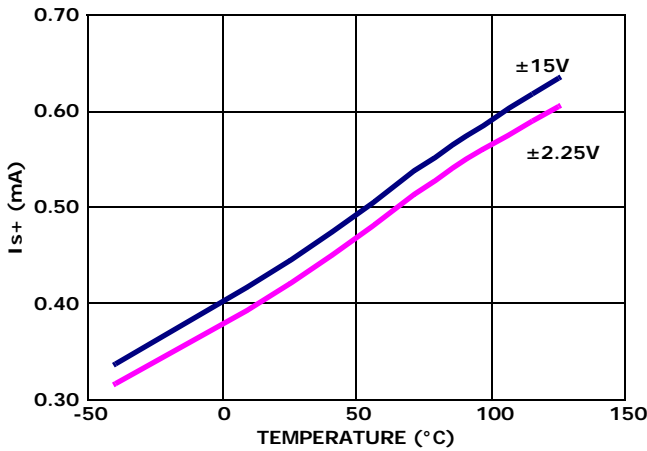


FIGURE 21. SUPPLY CURRENT PER AMP vs TEMPERATURE

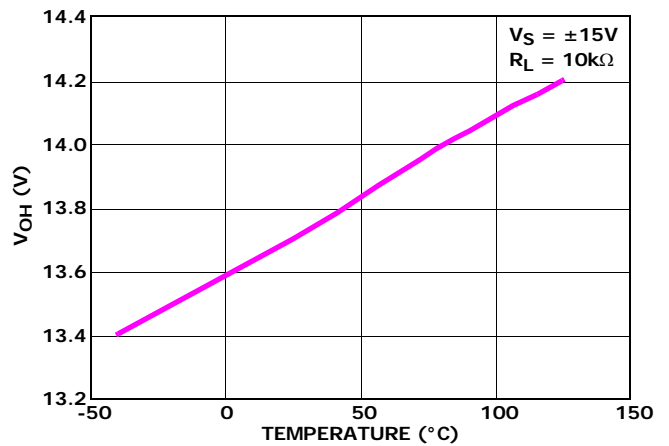


FIGURE 22. $+V_{OH}$ vs TEMPERATURE

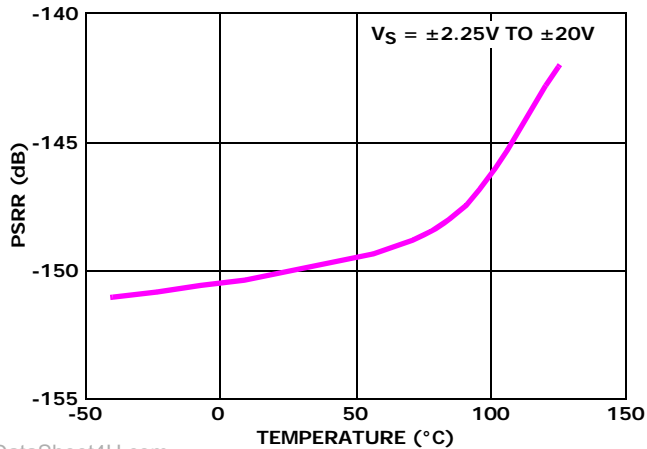


FIGURE 23. PSRR vs TEMPERATURE

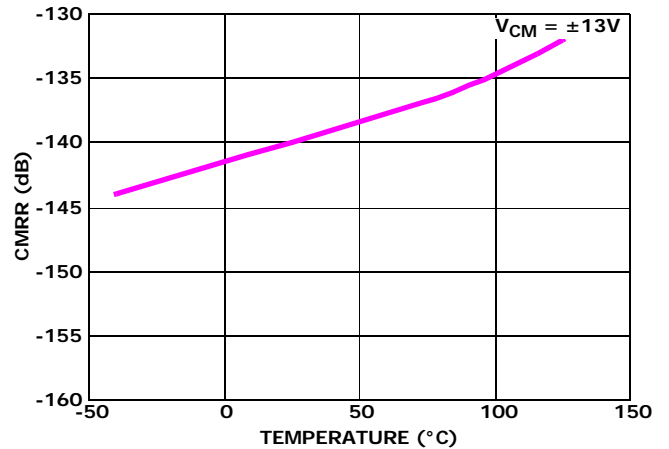


FIGURE 24. CMRR vs TEMPERATURE

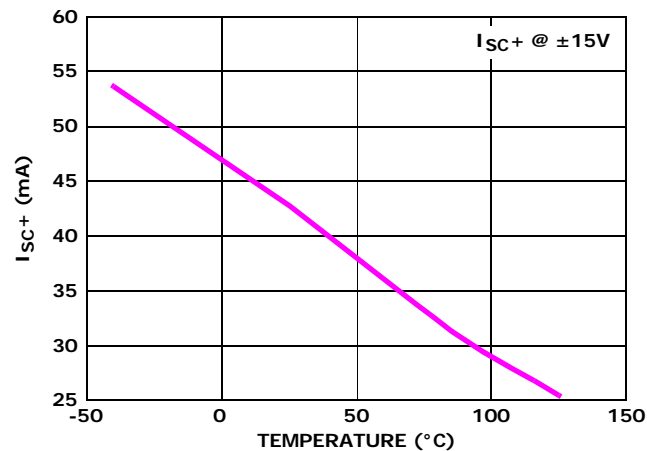


FIGURE 25. SHORT CIRCUIT CURRENT vs TEMPERATURE

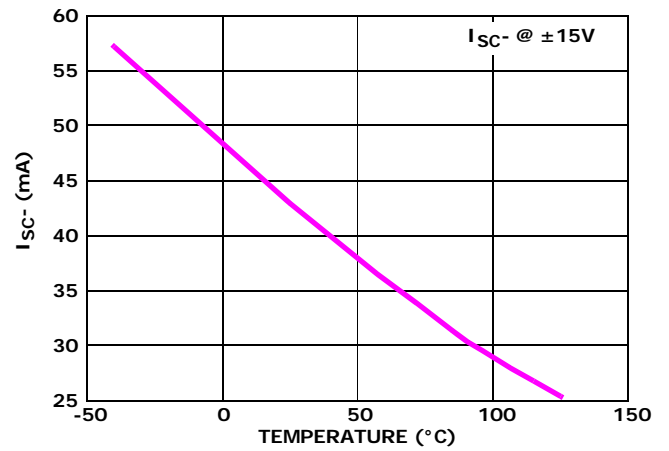


FIGURE 26. SHORT CIRCUIT CURRENT vs TEMPERATURE

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

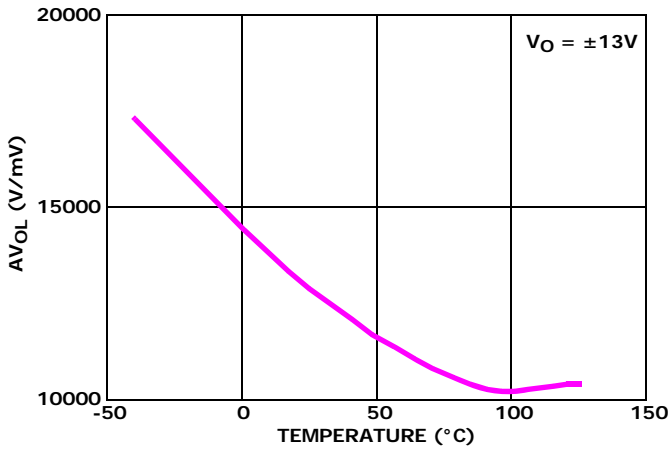


FIGURE 27. A_{VOL} vs TEMPERATURE

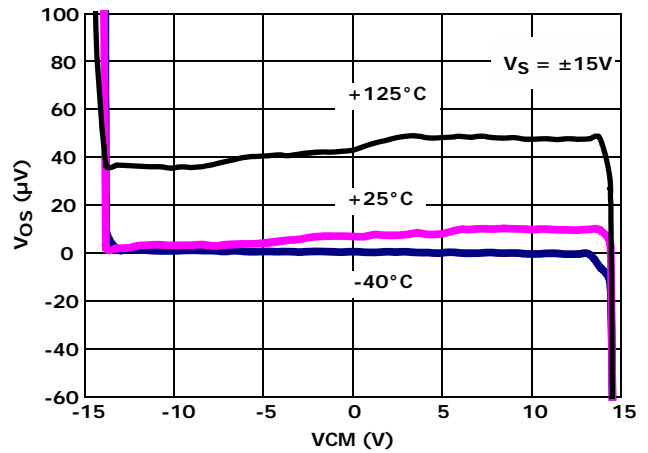


FIGURE 28. INPUT V_{OS} vs INPUT COMMON MODE VOLTAGE, $V_S = \pm 15V$

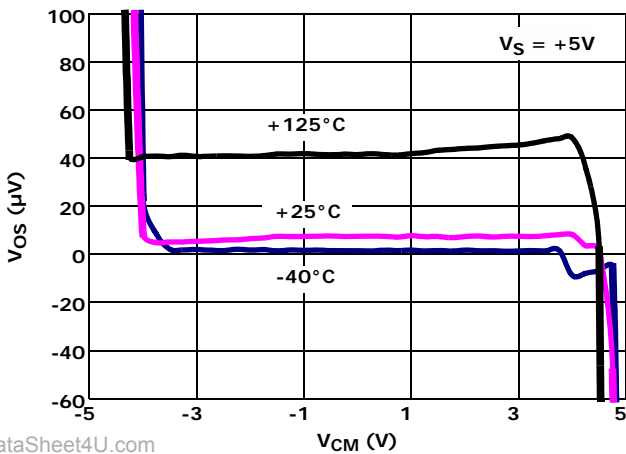


FIGURE 29. V_{OS} vs INPUT COMMON MODE VOLTAGE, $V_S = \pm 5V$

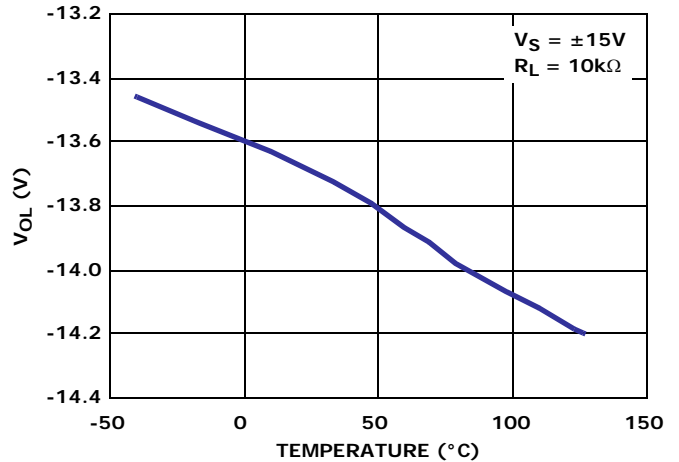


FIGURE 30. V_{OUT} vs TEMPERATURE

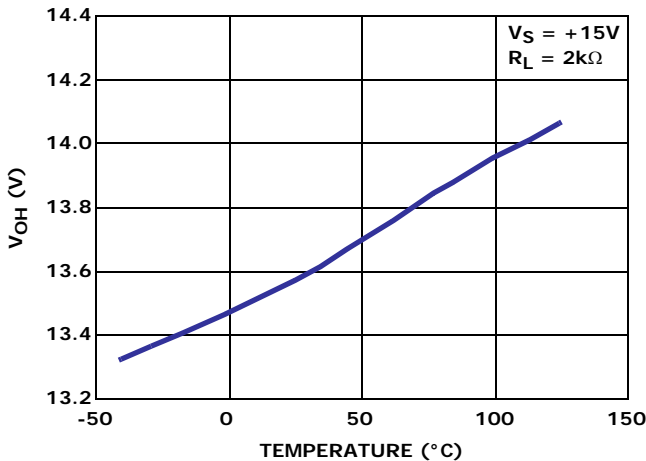


FIGURE 31. V_{OUT} vs TEMPERATURE

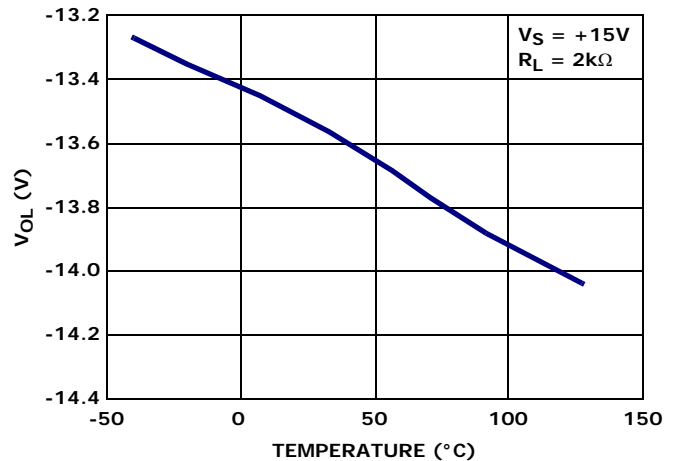


FIGURE 32. V_{OUT} vs TEMPERATURE

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Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

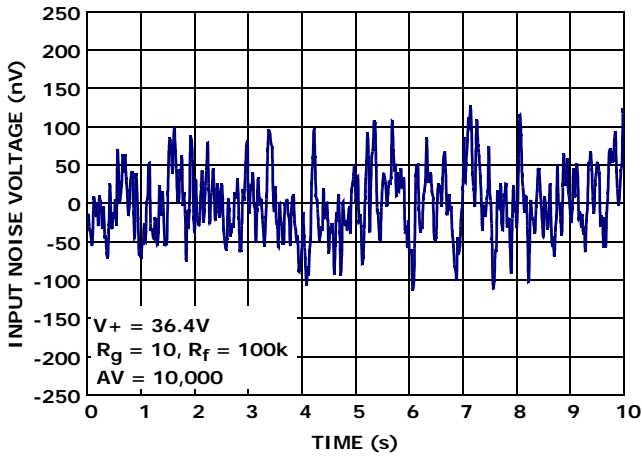


FIGURE 33. INPUT NOISE VOLTAGE 0.1Hz to 10Hz

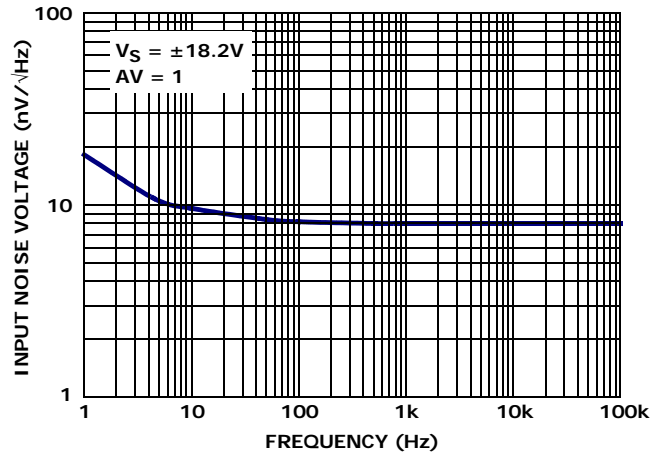
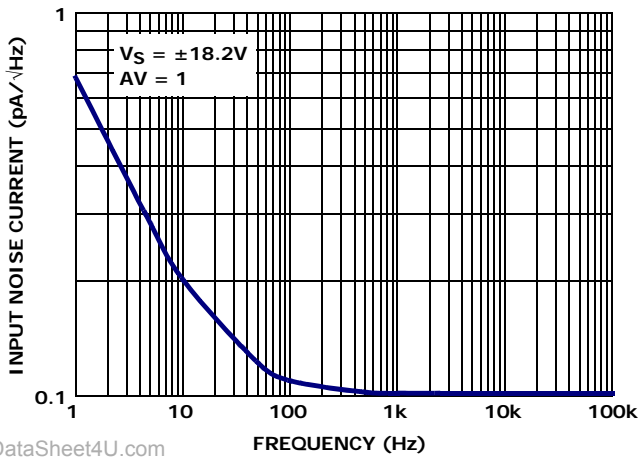


FIGURE 34. INPUT NOISE VOLTAGE SPECTRAL DENSITY



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FIGURE 35. INPUT NOISE CURRENT SPECTRAL DENSITY

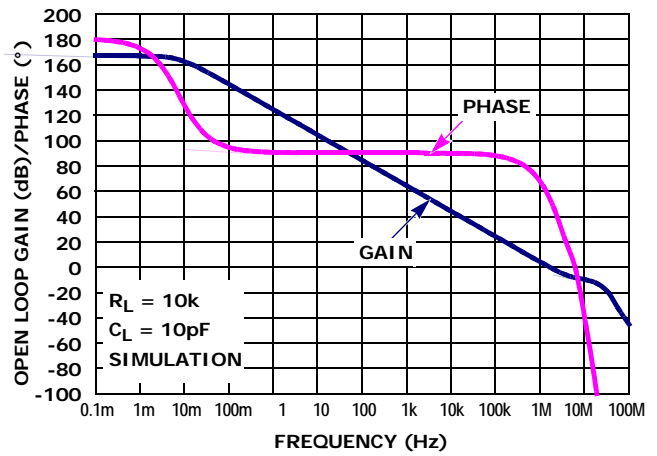


FIGURE 36. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 10k\Omega$, $C_L = 10pF$

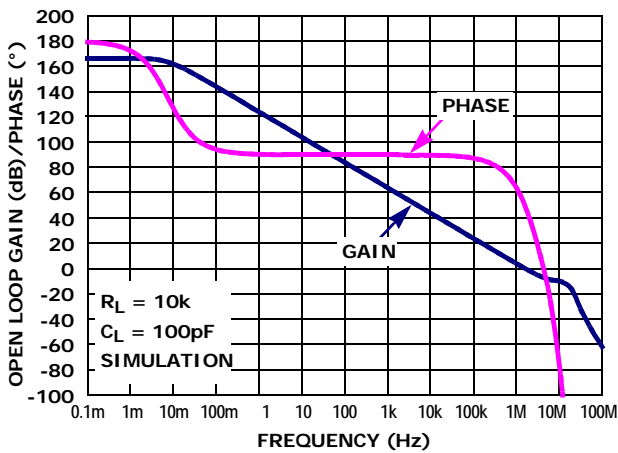


FIGURE 37. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 10k\Omega$, $C_L = 100pF$

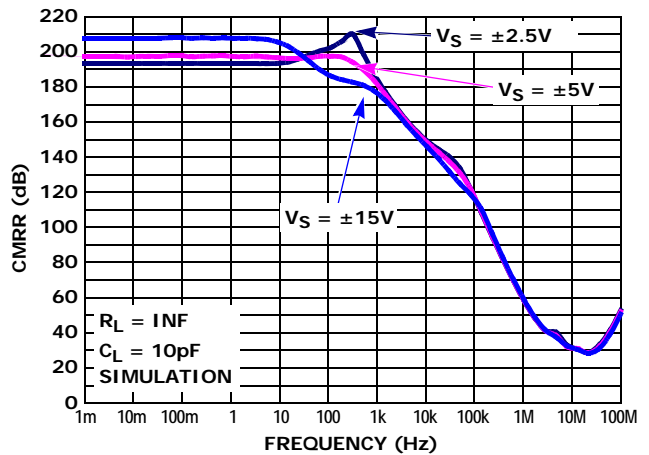


FIGURE 38. CMRR vs FREQUENCY, $V_S = \pm 2.25, \pm 5V, \pm 15V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

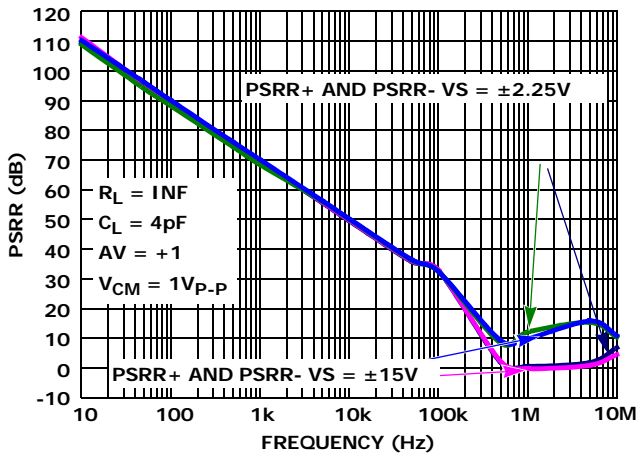


FIGURE 39. PSRR vs FREQUENCY, $V_S = \pm 5V$, $\pm 15V$

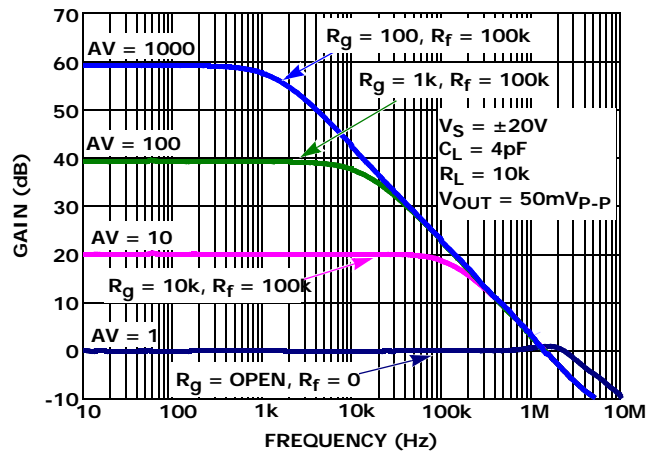


FIGURE 40. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

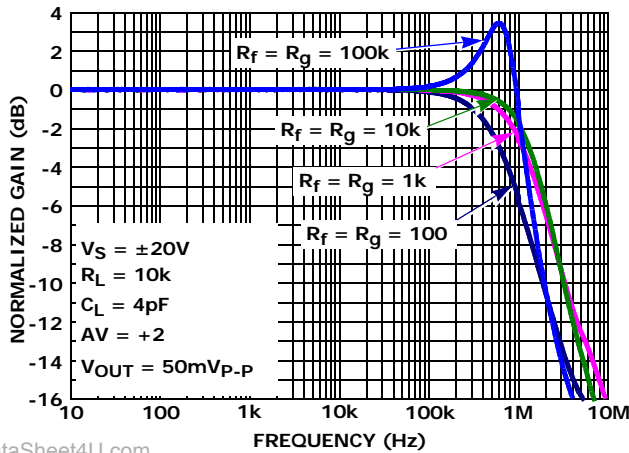


FIGURE 41. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

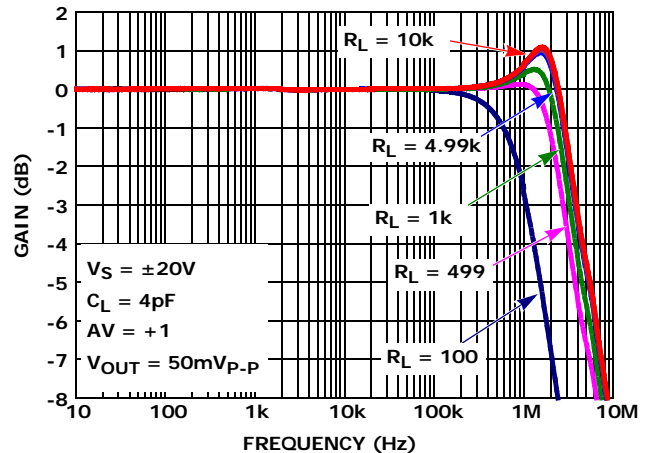


FIGURE 42. GAIN vs FREQUENCY vs R_L

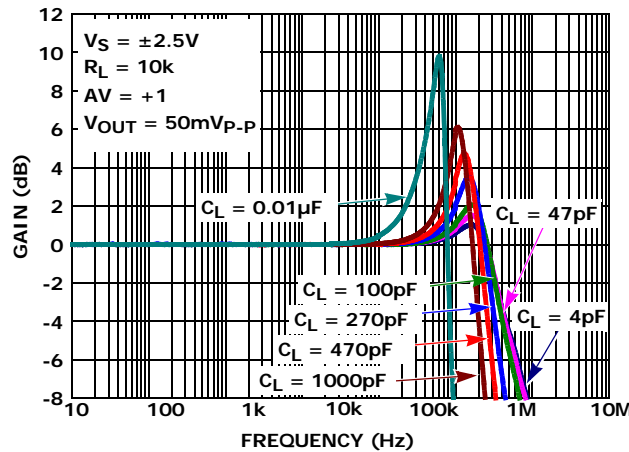


FIGURE 43. GAIN vs FREQUENCY vs C_L

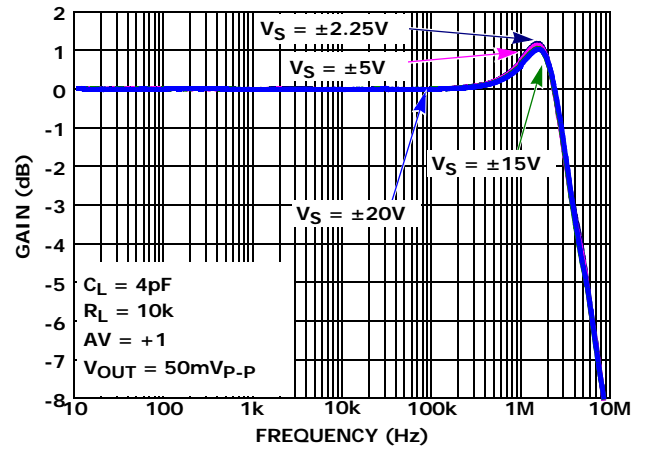


FIGURE 44. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

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Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

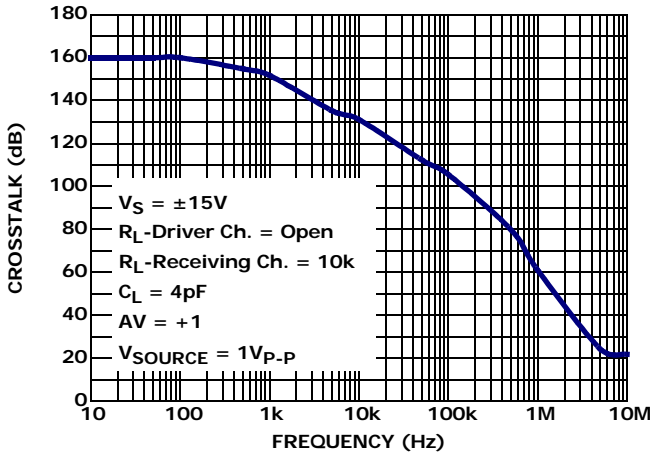


FIGURE 45. CROSSTALK, $V_S = \pm 15V$

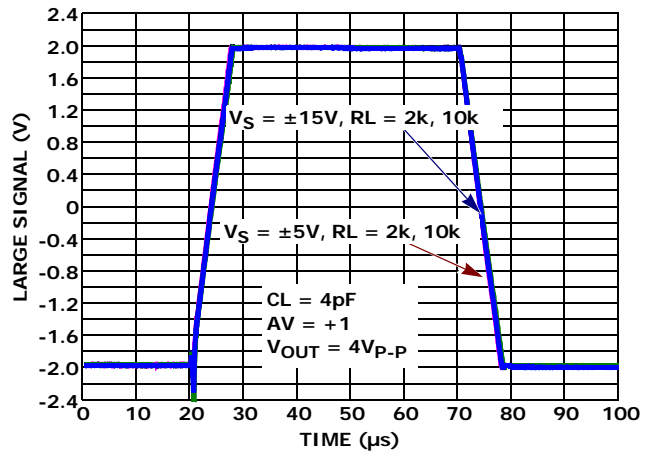


FIGURE 46. LARGE SIGNAL TRANSIENT RESPONSE vs R_L $V_S = \pm 5V, \pm 15V$

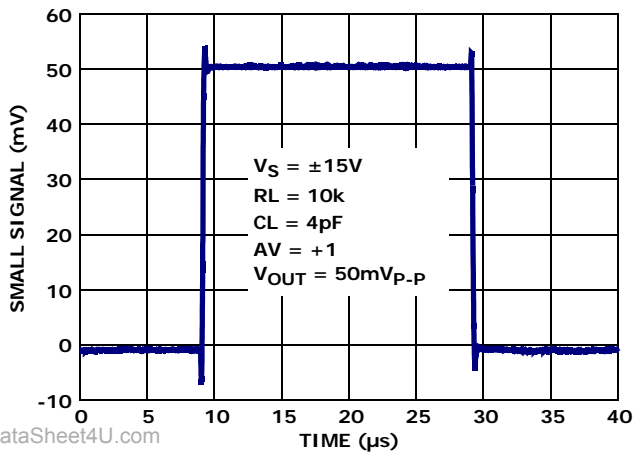


FIGURE 47. SMALL SIGNAL TRANSIENT RESPONSE, $V_S = \pm 5V, \pm 15V$

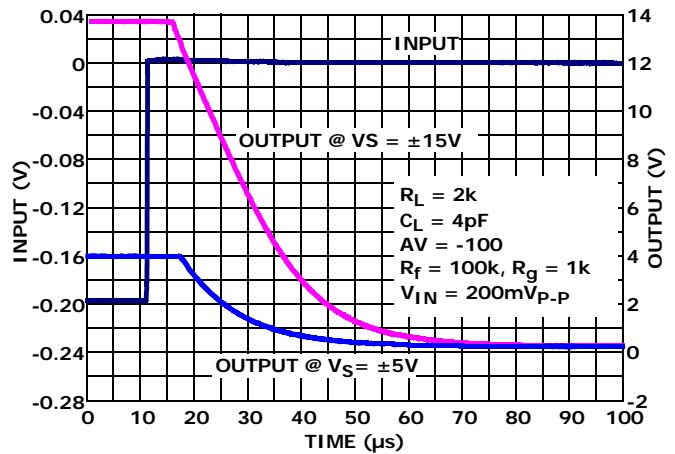


FIGURE 48. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 5V, \pm 15V$

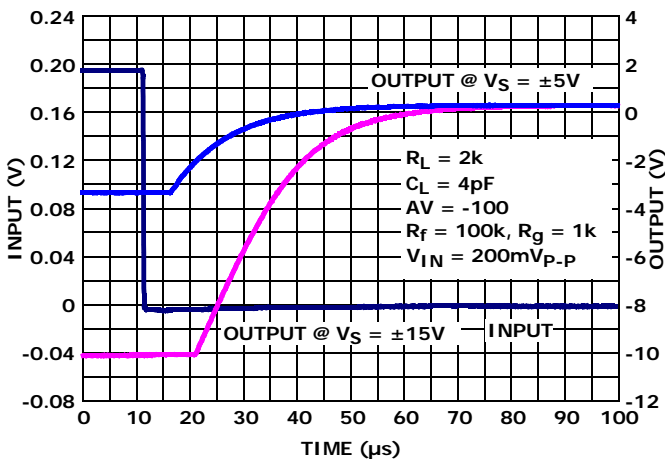


FIGURE 49. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 5V, \pm 15V$

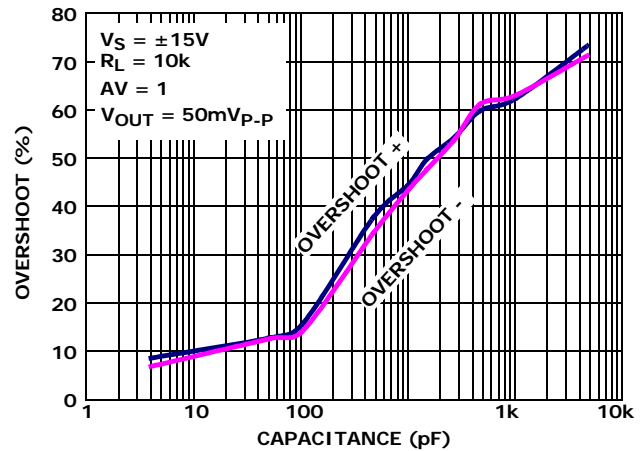


FIGURE 50. % OVERSHOOT vs LOAD CAPACITANCE, $V_S = \pm 15V$

Applications Information

Functional Description

The ISL28117 and ISL28217 are single and dual, low noise precision op amps. Both devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13 μ V typical), low input noise voltage (8nV/ $\sqrt{\text{Hz}}$), and low 1/f noise corner frequency (\sim 8Hz). These amplifiers also feature high open loop gain (18kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% @ 3.5V_{RMS}, 1kHz into 2k Ω). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate over the 4.5V (\pm 2.25V) to 40V (\pm 20V) range and are fully characterized at 10V (\pm 5V) and 30V (\pm 15V). The Power Supply Rejection Ratio typically exceeds 140dB over the full operating voltage range and 120dB minimum over the -40°C to $+125^{\circ}\text{C}$ temperature range. The worst case common mode input voltage range over temperature is 2V to each rail. With \pm 15V supplies, CMRR performance is typically $>$ 130dB over-temperature. The minimum CMRR performance over the -40°C to $+125^{\circ}\text{C}$ temperature range is $>$ 120dB for power supply voltages from \pm 5V (10V) to \pm 15V (30V).

Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta ($>$ 1000) reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to $<$ 1nA, and excellent temperature stabilization. Figures 9 through 16 show the high degree of bias current stability at \pm 5V and \pm 15V supplies that is maintained across the -40°C to $+125^{\circ}\text{C}$ temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision, high impedance amplifiers.

The $+25^{\circ}\text{C}$ maximum input offset voltage (V_{OS}) for the "B" grade is 50 μ V and 100 μ V for the "C" grade. Input offset voltage temperature coefficients ($V_{OS}TC$) are a maximum of \pm 0.6 μ V/ $^{\circ}\text{C}$ for the "B" and \pm 0.9 μ V/ $^{\circ}\text{C}$ for the "C" grade. Figures 1 through 4 show the typical gaussian-like distribution over the \pm 5V to \pm 15V supply range and over the full temperature range. The V_{OS} temperature behavior is smooth (Figures 5 through 8) maintaining constant TC across the entire temperature range.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500 Ω current limiting resistors and an anti-parallel diode pair across the inputs (Figure 51).

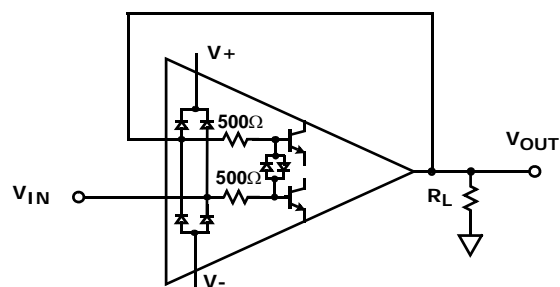


FIGURE 51. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dV/dT exceeds the 0.5V/ μ s slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes causing current to flow to the output resulting in severe distortion and possible diode failure. Figure 46 provides an example of distortion free large signal response using a 4V_{P-P} input pulse with an input rise time of $<$ 1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA max.

Output Current Limiting

The output current is internally limited to approximately \pm 45mA at $+25^{\circ}\text{C}$ and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability. Figures 25 and 26 show the current limit variation with temperature.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28117 and ISL28217 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the $+150^{\circ}\text{C}$ maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times P_{D_{MAXTOTAL}} \quad (\text{EQ. 1})$$

where:

- $P_{\text{DMAXTOTAL}}$ is the sum of the maximum power dissipation of each amplifier in the package (P_{DMAX})
- P_{DMAX} for each amplifier can be calculated using Equation 2:

$$P_{\text{DMAX}} = V_{\text{S}} \times I_{\text{qMAX}} + (V_{\text{S}} - V_{\text{OUTMAX}}) \times \frac{V_{\text{OUTMAX}}}{R_{\text{L}}} \quad (\text{EQ. 2})$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation of 1 amplifier
- V_{S} = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
10/16/09	FN6632.2	On page 2 "Ordering Information", changed the following: a) corrected part marking for ISL28117FBBZ from "28117 -B FBZ" to "28117 FBZ -B". Corrected part marking for ISL28217FBBZ from "28217-B FBZ" to "28217 FBZ -B" B) Updated package outline drawing to most recent revision (no changes were made to package dimensions; land pattern was added and dimensions were moved from table onto drawing) c) Added "Add "-T7" or "-T13" suffix for tape and reel." to the tape and reel Note 1. d) added Note 3 callout to all parts (Note 3 reads: "For Moisture Sensitivity Level (MSL), please see device information page for ISL28117, ISL28217. For more information on MSL please see techbrief TB363.") e) removed "Coming Soon" from ISL28117FBBZ, ISL28117FBZ & ISL28217FBBZ devices
10/8/09	FN6632.1	1. Removed "very" from "...low noise.." 1st sentence, page 1. 2. Removed "Low" from 6th bullet under features, page 1. 3. Modified typical characteristics curves to show conservative performance. Specific channel designations removed. On temperature curves, changed formatting to indicate range from typical value. Changes include: a. Removed former Figures 1, 3, 5, 7, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37 & 38 (all Channel A curves) b. Replaced former Figures 19, 20, 23, 24, 27, 28, 31, 32, 35, 36, 39 & 40 with new Figures 9 thru 20 (all "conservative channels") c. Added Figures 30, 31, 32 4. Updated TCvos histogram on page 1 to match TCvos histogram Figure 6 on page 7 (same graphic) 5. Added temp labels to Figures 28 & 29
9/3/09	FN6632.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL28117](#), [ISL28217](#)

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

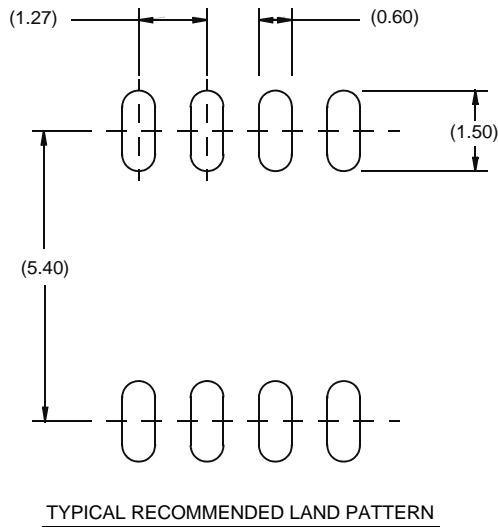
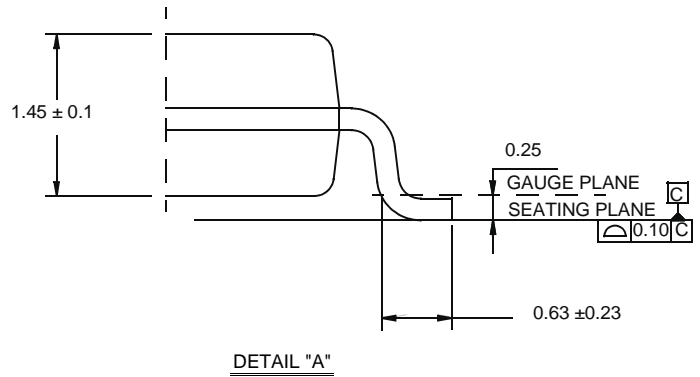
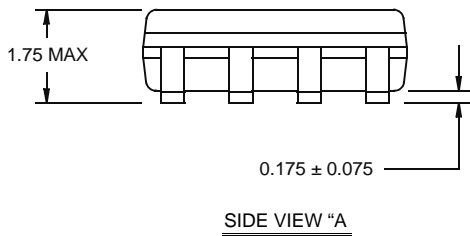
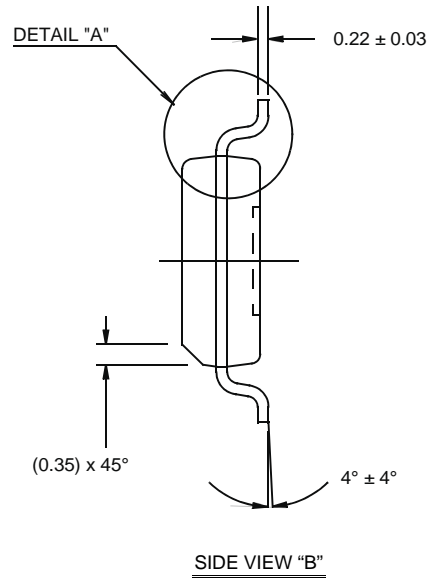
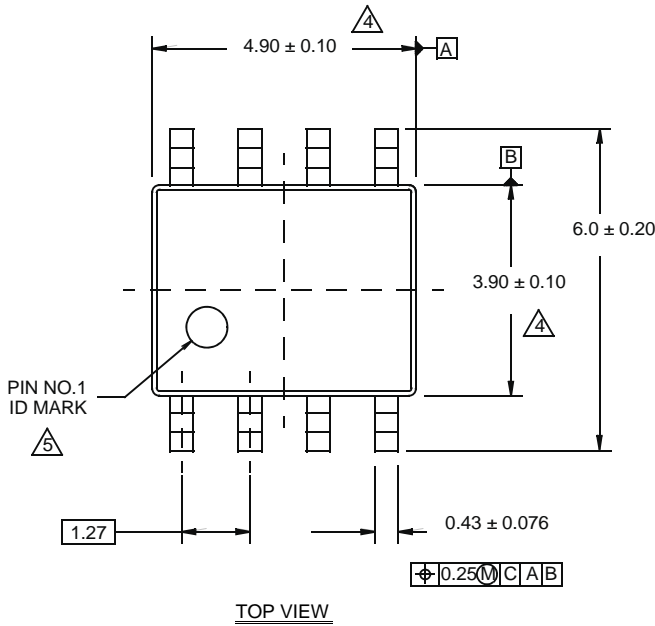
FITs are available from our website at <http://rel.intersil.com/reports/search.php>

Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 0, 08/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.