

Precision Single and Dual Low Noise Operational Amplifiers

The ISL28107 and ISL28207 are single and dual amplifiers featuring low input bias current, low noise, and low offset and temperature drift. This makes them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28107 single is available in an 8 Ld SOIC package. The ISL28207 dual amplifier will be offered in 8 Ld SOIC package. All devices are offered in standard pin configurations and operate over the extended temperature range to -40°C to +125°C.

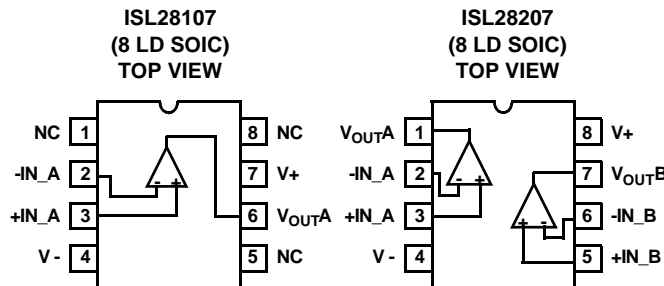
Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28207FBZ*	28207 FBZ	8 Ld SOIC	MDP0027
Coming Soon ISL28107FBZ*	28107 FBZ	8 Ld SOIC	MDP0027

*Add "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts



Features

- Low Input Offset 75µV, Max.
- Input Bias Current 60pA
- Superb Temperature Drift
 - Voltage Offset 0.65µV/°C, Max.
 - Input Current 0.2pA/°C
- Outstanding ESD performance
 - Human Body Model 4.5kV
 - Machine Model 500V
 - Charged Device Model 1.5kV
- Very Low Voltage Noise, 10Hz. 14nV/√Hz
- Low Current Consumption (per amp 0.29mA, Max.
- Gain-bandwidth Product. 1MHz
- Wide Supply Range 4.5V to 40V
- Operating Temperature Range -40°C to +125°C
- No Phase Reversal
- Pb-Free (RoHS Compliant)

Applications

- Precision Instruments
- Medical Instrumentation
- Spectral Analysis Equipment
- Geophysical Analysis Equipment
- Telecom Equipment
- Active Filter Blocks
- Microphone Pre-amplifier
- Thermocouples and RTD Reference Buffers
- Data Acquisition
- Power Supply Control

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Absolute Maximum Ratings

Maximum Supply Voltage	.42V
Maximum Differential Input Current	20mA
Maximum Differential Input Voltage	.42V
Min/Max Input Voltage	V- - 0.5V to V+ + 0.5V
Max/Min Input current for input voltage >V+ or <V-	±20mA
Output Short-Circuit Duration (1 output at a time)	Indefinite
ESD Tolerance	
Human Body Model	4.5kV
Machine Model	.500V
Charged Device Model	1.5kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld SOIC Package (ISL28207)	115
8 Ld SOIC Package (ISL28107)	120
Storage Temperature Range	-65°C to +150°C
Pb-free Reflow Profile	see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Operating Conditions

Ambient Operating Temperature Range	-40°C to +125°C
Maximum Operating Junction Temperature	+150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
V_{OS}	Offset Voltage Magnitude			17	75	μV
					140	μV
V_{OS}/T	Offset Voltage Drift			0.1	0.65	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		60	300	pA
		$T_A = +125^\circ\text{C}$			850	pA
I_B/T	Input Bias Current Drift			0.2		$\text{pA}/^\circ\text{C}$
I_{OS}	Input Offset Current	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		60	300	pA
		$T_A = +125^\circ\text{C}$			850	pA
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	-13		13	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -13\text{V}$ to $+13\text{V}$	115	145		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25\text{V}$ to $\pm 20\text{V}$	115	145		dB
A_{VOL}	Open-Loop Gain	$V_O = -13\text{V}$ to $+13\text{V}$, $R_L = 10\text{k}\Omega$ to ground	3,000	50,000		V/mV
V_{OH}	Output Voltage High	$R_L = 10\text{k}\Omega$ to ground		13.5	13.7	V
				13.2		V
		$R_L = 2\text{k}\Omega$ to ground		13.3	13.55	V
				13.1		V
V_{OL}	Output Voltage Low	$R_L = 10\text{k}\Omega$ to ground		-13.7	-13.5	V
					-13.2	V
		$R_L = 2\text{k}\Omega$ to ground		-13.55	-13.3	V
					-13.1	V
I_S	Supply Current/Amplifier	$R_L = \text{Open}$		0.21	0.29	mA
					0.35	mA
I_{SC}	Short-Circuit	$R_L = 10\Omega$ to ground		±40		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	±2.25		±20	V

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www.intersil.com **Electrical Specifications** $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to $+125^\circ\text{C}$. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			1		MHz
e_{n-p-p}	Voltage Noise	0.1Hz to 10Hz, $V_S = \pm 19V$		340		nV _{P-P}
e_n	Voltage Noise Density	$f = 10\text{Hz}$, $V_S = \pm 19V$		14		nV/ $\sqrt{\text{Hz}}$
e_n	Voltage Noise Density	$f = 100\text{Hz}$, $V_S = \pm 19V$		13		nV/ $\sqrt{\text{Hz}}$
e_n	Voltage Noise Density	$f = 1\text{kHz}$, $V_S = \pm 19V$		13		nV/ $\sqrt{\text{Hz}}$
e_n	Voltage Noise Density	$f = 10\text{kHz}$, $V_S = \pm 19V$		13		nV/ $\sqrt{\text{Hz}}$
i_n	Current Noise Density	$f = 10\text{kHz}$, $V_S = \pm 19V$		53		fA/ $\sqrt{\text{Hz}}$
THD + N	Total Harmonic Distortion + Noise	1kHz, $G = 1$, $V_O = 3.5V_{RMS}$, $R_L = 2k\Omega$		0.0035		%
TRANSIENT RESPONSE						
SR	Slew Rate	$A_V = 10$, $R_L = 10k\Omega$, $V_O = 10V_{P-P}$		± 0.32		V/ μs
t_r , t_f , Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		355		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		365		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_g = R_f = 10k$, $R_L = 2k\Omega$ to V_{CM}		29		μs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_g = R_f = 10k$, $R_L = 2k\Omega$ to V_{CM}		31.2		μs
t_{OL}	Output Overload Recovery Time	$A_V = 100$, $V_{IN} = 0.2V$, $R_L = 2k\Omega$ to V_{CM}		6		μs

Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ\text{C}$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to $+125^\circ\text{C}$. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
V_{OS}	Offset Voltage			10	75	μV
					140	μV
V_{OS}/T	Offset Voltage Drift			0.2	0.65	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		60	300	pA
		$T_A = +125^\circ\text{C}$			850	pA
I_B/T	Input Bias Current Drift			0.2		pA/ $^\circ\text{C}$
I_{OS}	Input Offset Current	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		60	300	pA
		$T_A = +125^\circ\text{C}$			850	pA
V_{CM}	Common Mode Input Voltage Range	Guaranteed by CMRR test	-3		3	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -3V$ to $+3V$	115	145		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25V$ to $\pm 5V$	115	145		dB
A_{VOL}	Open-Loop Gain	$V_O = -3V$ to $+3V$, $R_L = 10k\Omega$ to ground	3,000	50,000		V/mV
V_{OH}	Output Voltage High	$R_L = 10k\Omega$ to ground		3.5	3.7	V
				3.2		V
		$R_L = 2k\Omega$ to ground		3.3	3.55	V
				3.1		V

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www.intersil.com **Electrical Specifications** $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
V_{OL}	Output Voltage Low	$R_L = 10k\Omega$ to ground		-3.7	-3.5	V
					-3.2	V
		$R_L = 2k\Omega$ to ground		-3.55	-3.3	V
					-3.1	V
I_S	Supply Current/Amplifier	$R_L = \text{Open}$		0.21	0.29	mA
					0.35	mA
I_{SC}	Short-Circuit			± 40		mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			1		MHz
THD + N	Total Harmonic Distortion + Noise	1kHz, $G = 1$, $V_O = 2.5V_{RMS}$, $R_L = 2k\Omega$		0.0053		%
TRANSIENT RESPONSE						
SR	Slew Rate	$A_V = 10$, $R_L = 2k\Omega$		0.32		V/ μs
t_r , t_f , Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		355		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		370		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_f = R_g = 2k\Omega$, $R_L = 2k\Omega$ to V_{CM}		12.4		μs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_f = R_g = 2k\Omega$, $R_L = 2k\Omega$ to V_{CM}		22		μs

NOTE:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified.

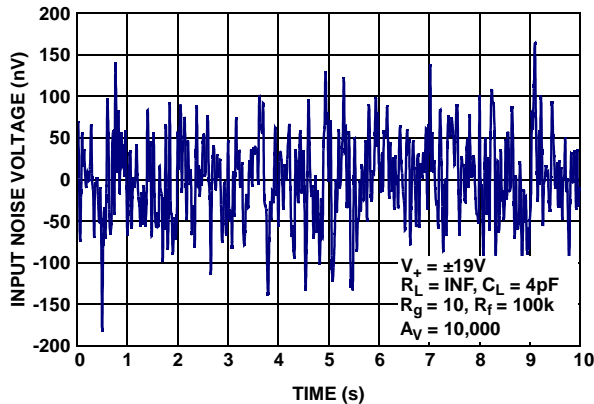


FIGURE 1. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

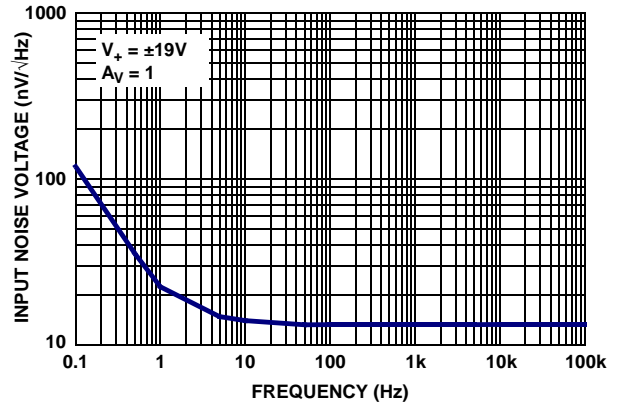


FIGURE 2. INPUT NOISE VOLTAGE SPECTRAL DENSITY

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

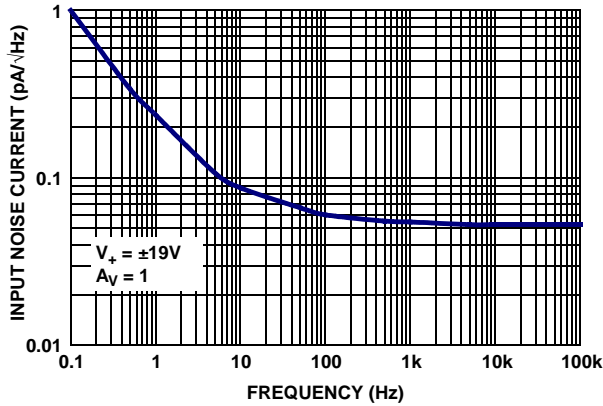


FIGURE 3. INPUT NOISE CURRENT SPECTRAL DENSITY

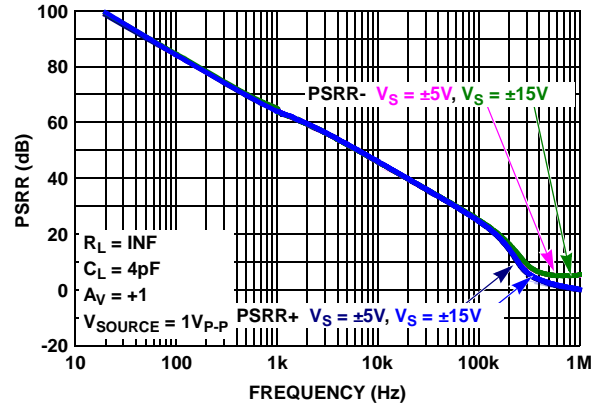


FIGURE 4. PSRR vs. FREQUENCY, $V_S = \pm 5V, \pm 15V$

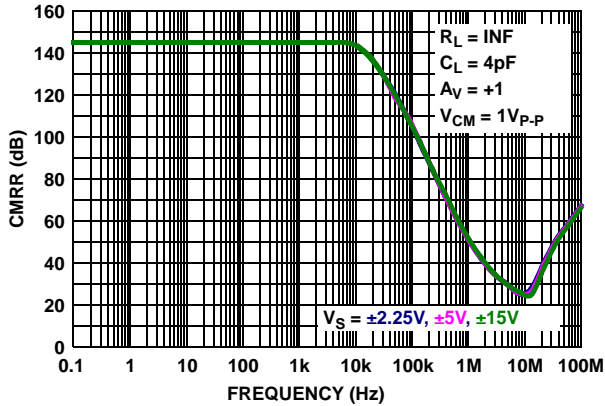


FIGURE 5. CMRR vs. FREQUENCY, $V_S = \pm 2.25V, \pm 5V, \pm 15V$

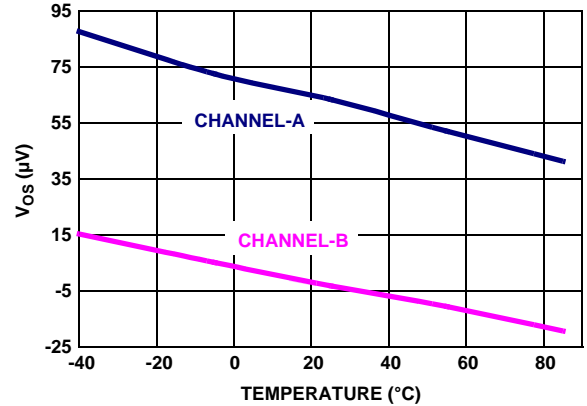


FIGURE 6. V_{OS} vs. TEMPERATURE

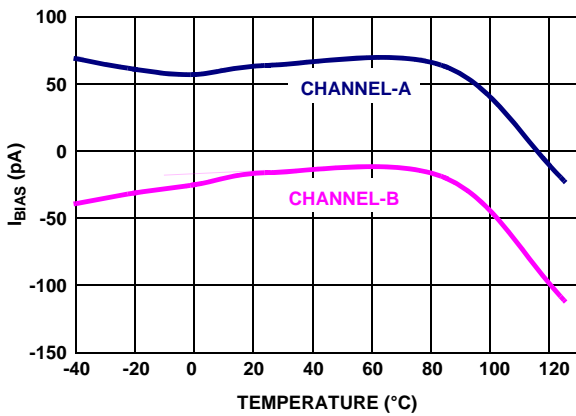


FIGURE 7. I_{IB} vs. TEMPERATURE, $V_S = \pm 5V$

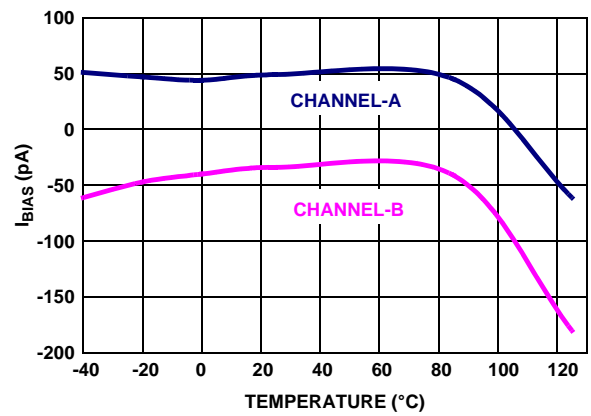


FIGURE 8. I_{IB} vs. TEMPERATURE, $V_S = \pm 15V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

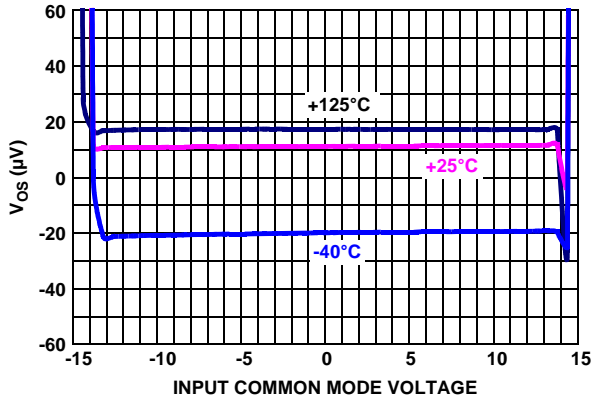


FIGURE 9. INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE VOLTAGE, $V_S = \pm 15V$

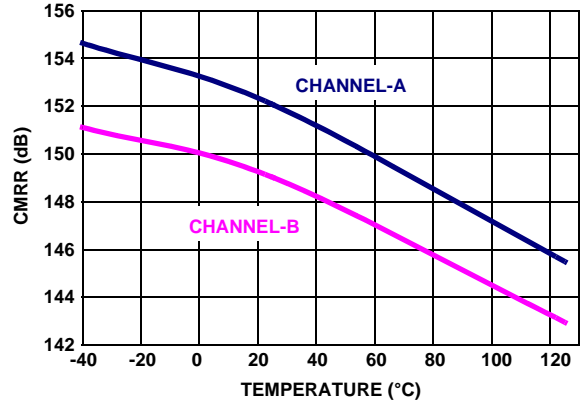


FIGURE 10. CMRR vs. TEMPERATURE, $V_S = \pm 15V$

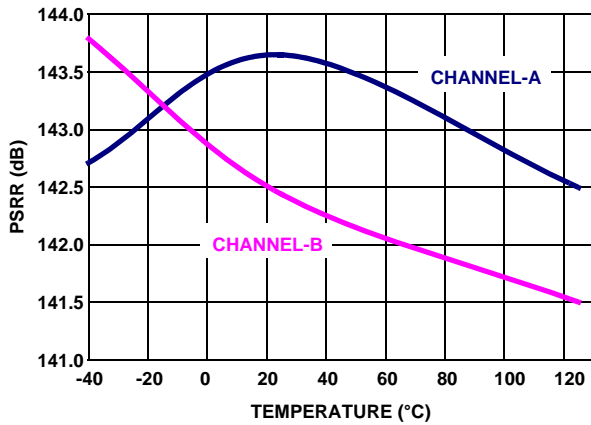


FIGURE 11. PSRR vs. TEMPERATURE, $V_S = \pm 5V$

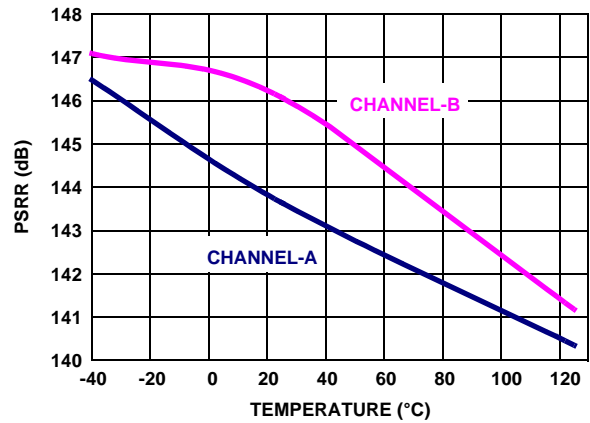


FIGURE 12. PSRR vs. TEMPERATURE, $V_S = \pm 15V$

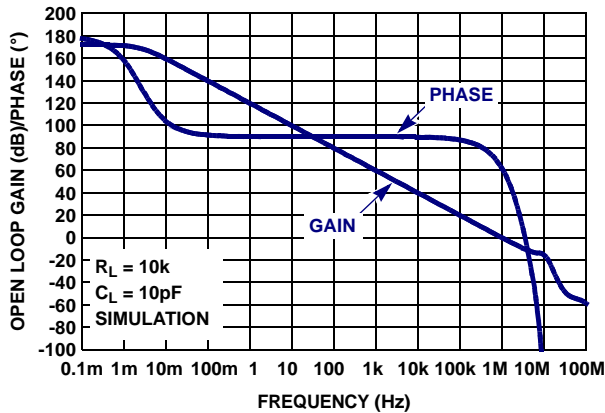


FIGURE 13. OPEN-LOOP GAIN, PHASE vs. FREQUENCY, $R_L = 10k\Omega$, $C_L = 10pF$

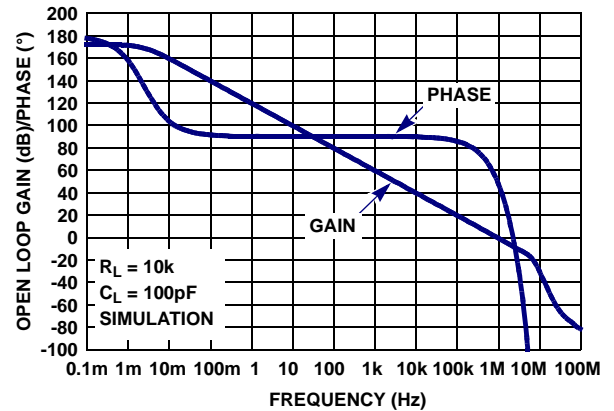


FIGURE 14. OPEN-LOOP GAIN, PHASE vs. FREQUENCY, $R_L = 10k\Omega$, $C_L = 100pF$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

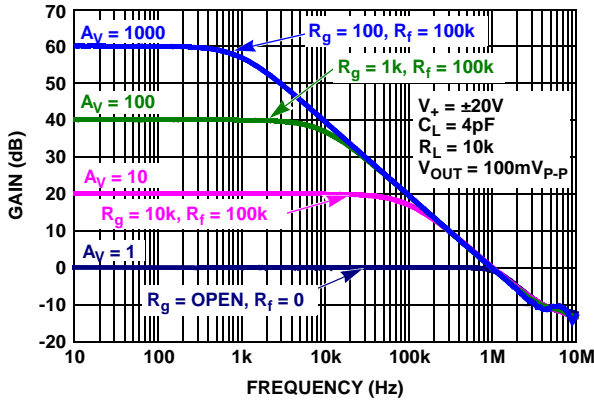


FIGURE 15. FREQUENCY RESPONSE vs. CLOSED LOOP GAIN

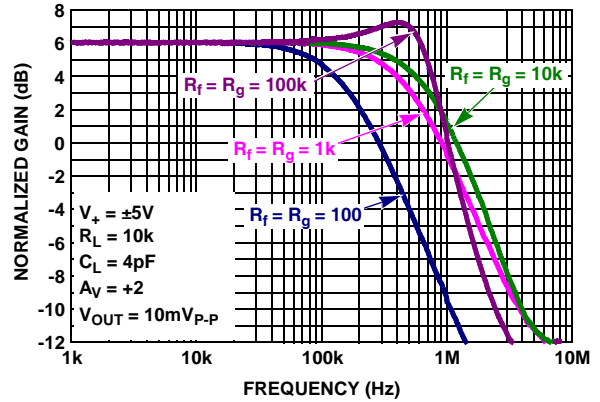


FIGURE 16. FREQUENCY RESPONSE vs. FEEDBACK RESISTANCE R_f/R_g

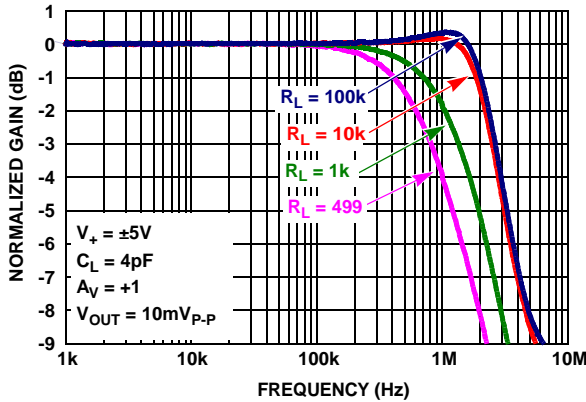


FIGURE 17. GAIN vs. FREQUENCY vs. R_L

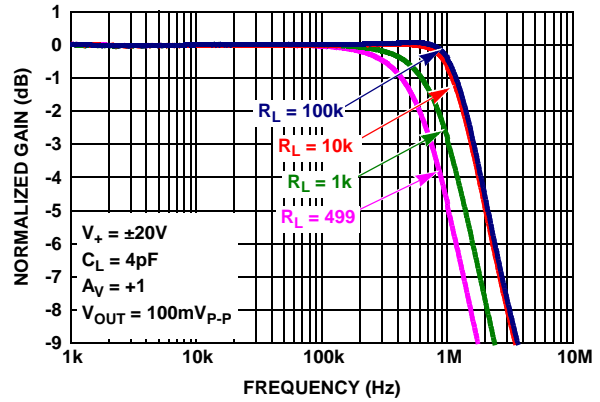


FIGURE 18. GAIN vs. FREQUENCY vs. R_L

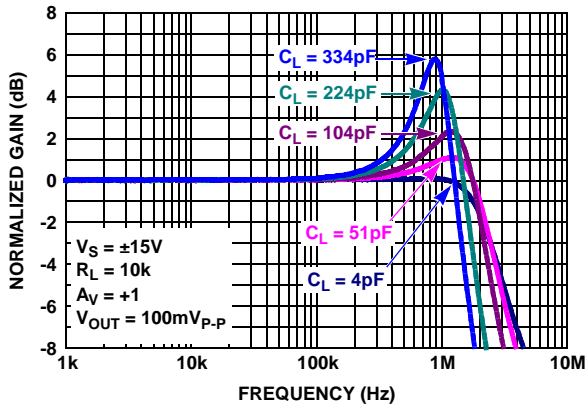


FIGURE 19. GAIN vs. FREQUENCY vs. C_L

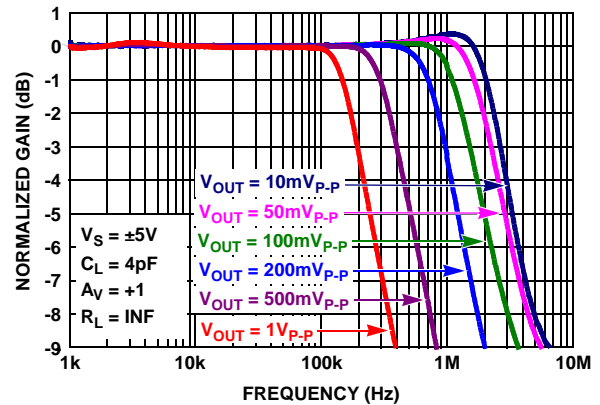


FIGURE 20. GAIN vs. FREQUENCY vs. OUTPUT VOLTAGE

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

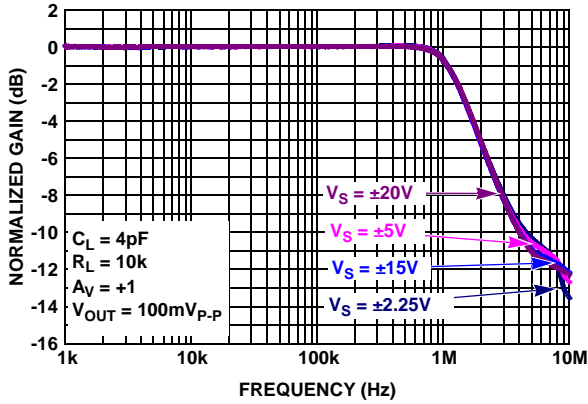


FIGURE 21. GAIN vs. FREQUENCY vs. SUPPLY VOLTAGE

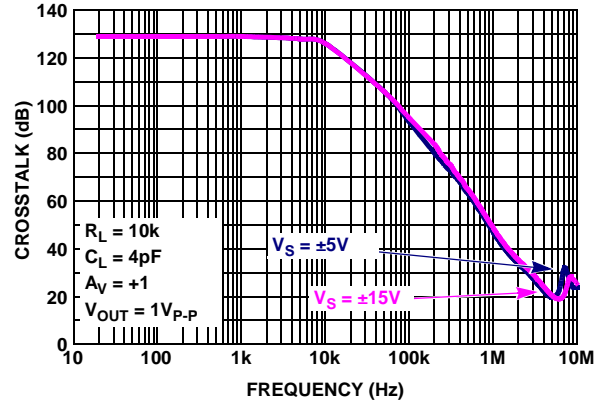


FIGURE 22. CROSSTALK vs. FREQUENCY, $V_S = \pm 5V, \pm 15V$

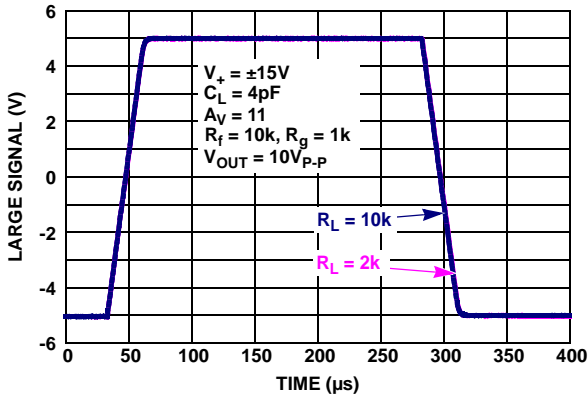


FIGURE 23. LARGE SIGNAL 10V STEP RESPONSE, $V_S = \pm 15V$

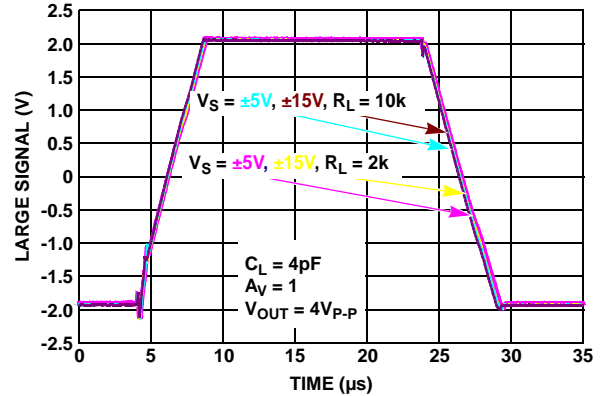


FIGURE 24. LARGE SIGNAL TRANSIENT RESPONSE vs. R_L
 $V_S = \pm 5V, \pm 15V$

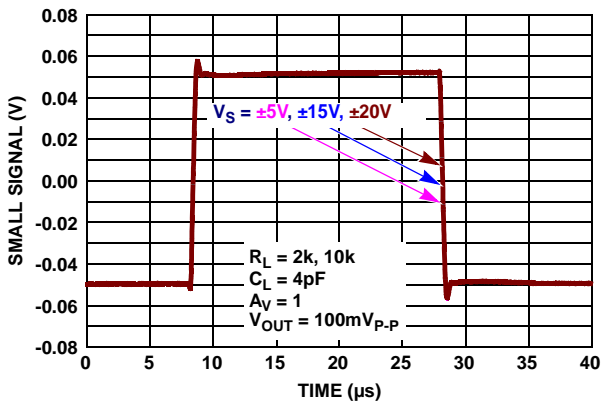


FIGURE 25. SMALL SIGNAL TRANSIENT RESPONSE
 $V_S = \pm 5V, \pm 15V, \pm 20V$

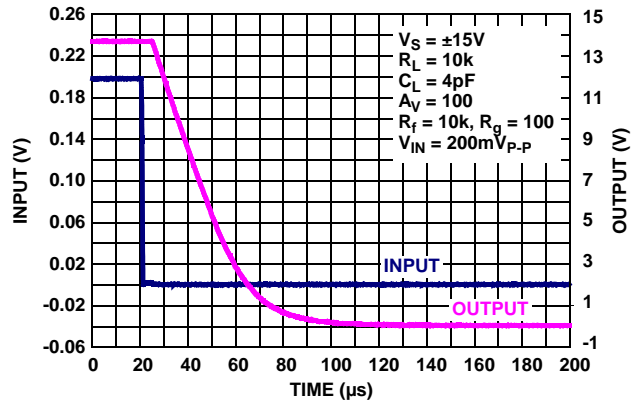


FIGURE 26. POSITIVE OUTPUT OVERLOAD RESPONSE
TIME, $V_S = \pm 15V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, unless otherwise specified. (Continued)

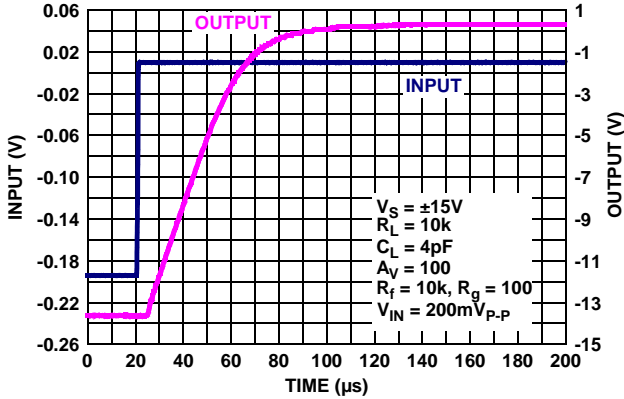


FIGURE 27. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 15V$

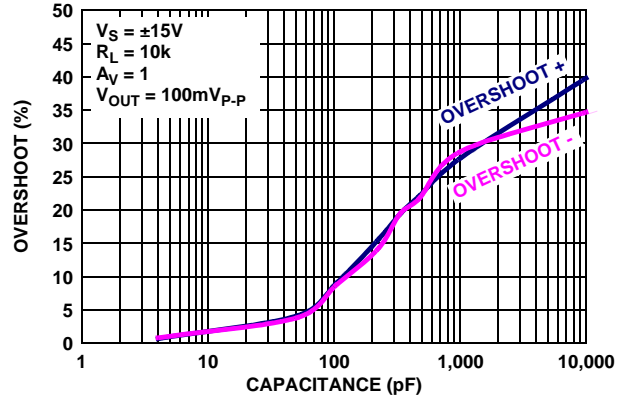
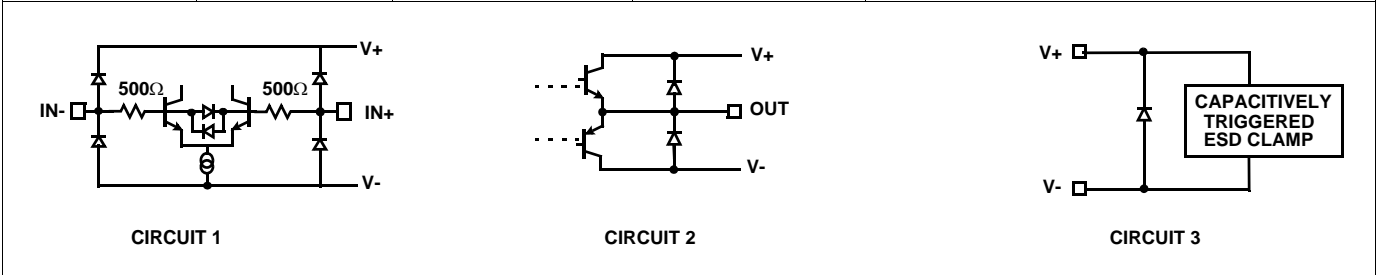


FIGURE 28. % OVERSHOOT vs. LOAD CAPACITANCE, $V_S = \pm 15V$

Pin Descriptions

ISL28107 (8 LD SOIC)	ISL28207 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	4	V-	Circuit 3	Negative power supply
	5	+IN_B	Circuit 1	Amplifier B non-inverting input
	6	-IN_B	Circuit 1	Amplifier B inverting input
	7	V _{OUTB}	Circuit 2	Amplifier B output
7	8	V+	Circuit 3	Positive power supply
6	1	V _{OUTA}	Circuit 2	Amplifier A output
2	2	-IN_A	Circuit 1	Amplifier A inverting input
1, 5, 8		NC	-	No internal connection



Applications Information

Functional Description

The ISL28107 and ISL28207 are single and dual, very low 1/f noise (14nV/√Hz @ 10Hz) precision op-amps. These amplifiers feature very high open loop gain (50kV/mV) for excellent CMRR (145dB), and gain accuracy. Both devices are fabricated in a new precision 40V complementary bipolar DI process.

The super-beta NPN input stage with bias current cancellation provides bipolar-like levels of AC performance with the low input bias currents approaching JFET levels. The temperature stabilization provided by bias current cancellation removes the high input bias current temperature coefficient commonly found in JFET amplifiers. Figures 7 and 8 show the input bias current variation over temperature.

The input offset voltage (V_{OS}) has a very low, worst case value of 75μV max at +25°C and a maximum T_C of 0.65μV/°C. Figure 6 shows V_{OS} as a function of supply voltage and temperature with the common mode voltage at 0V for split supply operation.

The complimentary bipolar output stage maintains stability driving large capacitive loads (to 10nF) without external compensation. The small signal overshoot vs. load capacitance is shown in Figure 28.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete 4.5V to 40V operating voltage range. Parameter variation with operating voltage is shown in the “Typical Performance Curves” beginning on page 4. The input common mode voltage range sensitivity to temperature is shown in Figure 9 (±15V).

Input ESD Diode Protection

The input terminals (IN+ and IN-) each have internal ESD protection diodes to the positive and negative supply rails, a series connected 500Ω current limiting resistor followed by an anti-parallel diode pair across the input NPN transistors (Circuit 1 in “Pin Descriptions” on page 9).

The resistor-ESD diode configuration enables a wide differential input voltage range equal to the lesser of the Maximum Supply Voltage in the “Absolute Maximum Ratings” on page 2 (42V) or, a maximum of 0.5V beyond the V+ and V- supply voltage. The internal protection resistors eliminate the need for external input current limiting resistors in unity gain connections and other circuit applications where large voltages or high slew rate signals are present. Although the amplifier is fully protected, high input slew rates that exceed the amplifier slew rate (±0.32V/μs) may cause output distortion.

Output Current Limiting

The output current is internally limited to approximately ±40mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op-amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28107 and ISL28207 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Using Only One Channel

The ISL28207 is a dual op-amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the inverting input and ground the positive input (as shown in Figure 29).

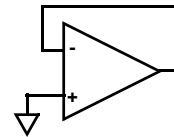


FIGURE 29. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

R_L = Load resistance

Revision History

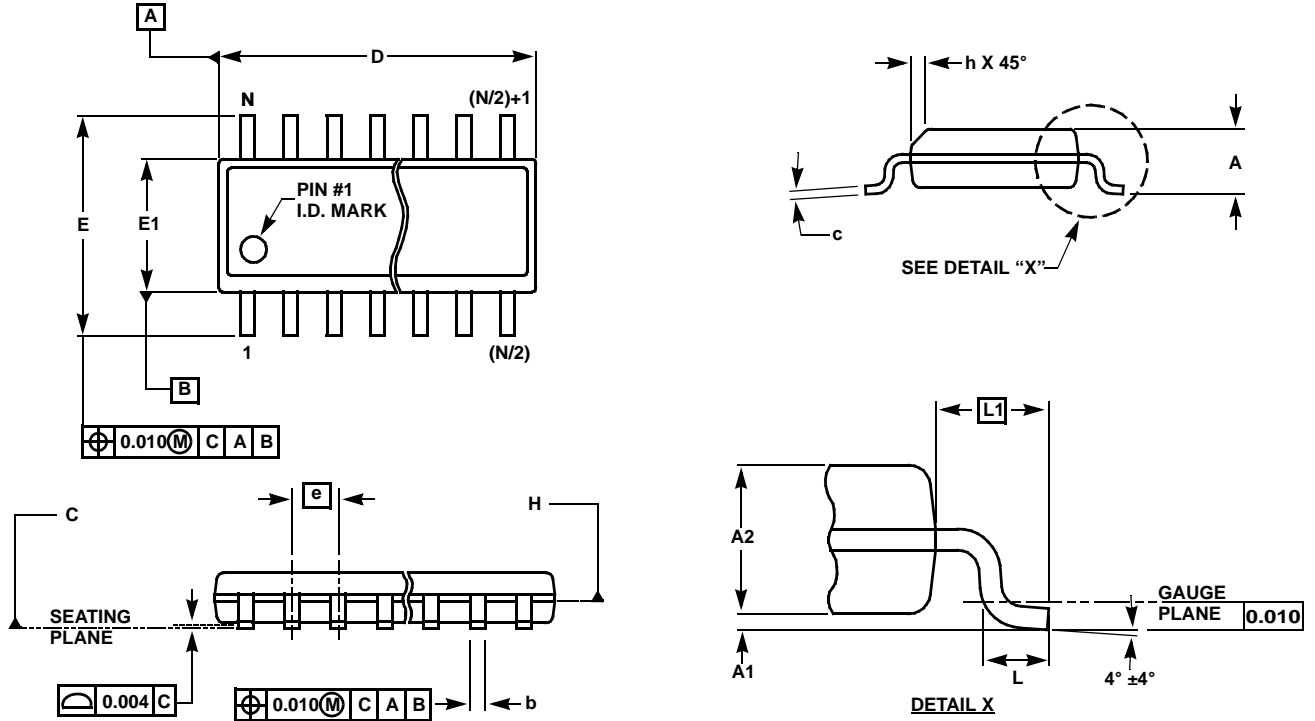
DATE	REVISION	CHANGE

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Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994