

TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

TA2151FN

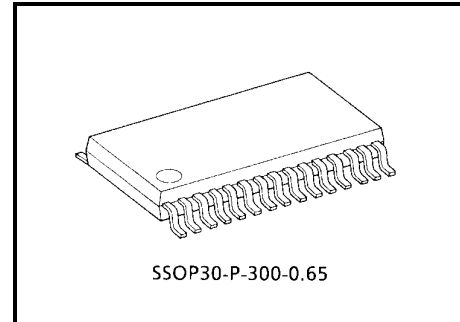
RF Amplifier for Digital Servo CD System

TA2151FN is a 3-beam type PUH compatible RF Amplifier for Digital Servo to be used in the CD system.

In combination with a CMOS single chip processor TC9462F/TC9495F, a CD system can be composed very simply.

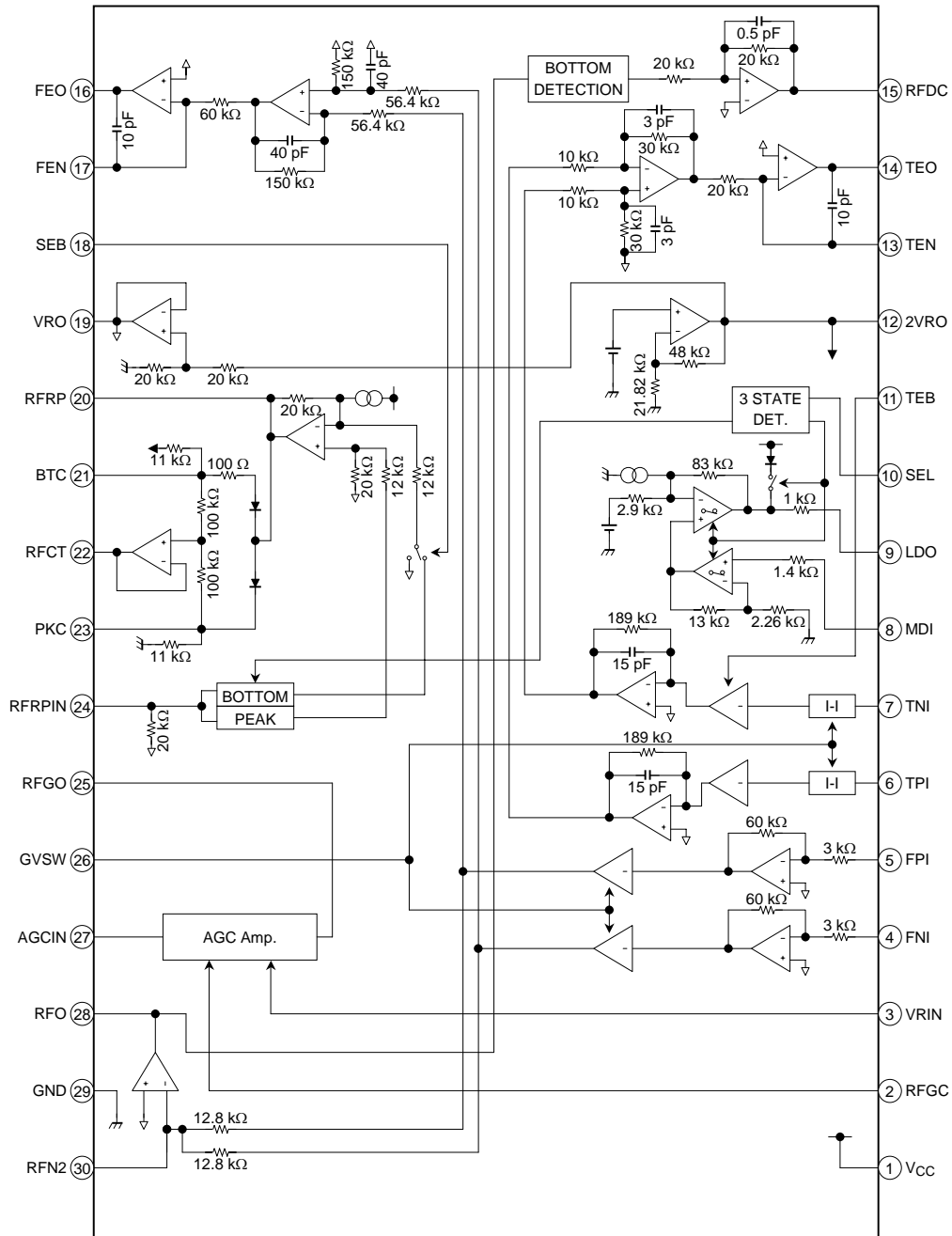
Features

- Built-in amplifier for reference (VRO, 2VRO) supply.
- Built-in Auto Laser Power Control circuit.
- Built-in RF amplifier.
- Built-in AGC amplifier.
- Built-in focus error amp and tracking error amp.
- Built-in gain change circuit for CD-RW.
- Capable of tracking balance control with TC9462F/TC9495F.
- Built-in signal amplifier for track counter.
- Capable of 4 times speed operation.
- 30 pin mini flat package.



Weight: 0.17 g (typ.)

Block Diagram



SEL	LDC			RFRP Detect Frequency
	SW1	SW2	SW3	
GND	ON	OFF	OFF	Low
HiZ	OFF	ON	ON	
V _{CC}				High

GVSW	Mode
GND	CD-RW
HiZ	Normal
V _{CC}	

SEB	Bottom Detect	Peak Detect
GND	ON	ON
HiZ		
V _{CC}	OFF	

Pin Function

Pin No.	Symbol	I/O	Functional Description	Remarks													
1	V _{CC}	—	Power supply input terminal.	—													
2	RFGC	I	RF amplitude adjustment control signal input terminal. Controlled by 3-PWM signals. (PWM carrier = 88.2 kHz) RFGC input voltage: V _{RO} ± 1.5 V AGC amplifier voltage gain: ×0.7~1.5 (typ.)	—													
3	VRIN	I	AGC amp. Reference voltage input terminal.	Connected to V _{RO}													
4	FNI	I	Main beam I-V amp input terminal.	Connected to pin diode output B + D (through resistor).													
5	FPI	I	Main beam I-V amp input terminal.	Connected to pin diode output A + C (through resistor).													
6	TPI	I	Sub beam I-V amp input terminal.	Connected to pin diode output F.													
7	TNI	I	Sub beam I-V amp input terminal.	Connected to pin diode output E.													
8	MDI	I	Monitor photo diode amp input terminal.	Connected to monitor photo diode.													
9	LDO	O	Laser diode amp input terminal.	Connected to laser diode control circuit.													
10	SEL	I	Laser diode control signal input terminal and APC circuit ON/OFF control signal terminal. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>SEL Level</th> <th>APC Circuit</th> <th>LDO</th> <th>Detect Frequency</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>OFF</td> <td>Connected to V_{CC} through resistor (1 kΩ)</td> <td>Low</td> </tr> <tr> <td>HiZ</td> <td rowspan="2">ON</td> <td rowspan="2">Control signal output</td> <td rowspan="2">High</td> </tr> <tr> <td>V_{CC}</td> </tr> </tbody> </table>	SEL Level	APC Circuit	LDO	Detect Frequency	GND	OFF	Connected to V _{CC} through resistor (1 kΩ)	Low	HiZ	ON	Control signal output	High	V _{CC}	3 signals input. (V _{CC} , HiZ, GND)
SEL Level	APC Circuit	LDO	Detect Frequency														
GND	OFF	Connected to V _{CC} through resistor (1 kΩ)	Low														
HiZ	ON	Control signal output	High														
V _{CC}																	
11	TEB	I	Tracking error balance adjustment signal input terminal. Controlled by 3-PWM signal. (PWM carrier = 88.2 kHz)	3 signals input. (2V _{RO} , V _{RO} , GND)													
12	2V _{RO}	O	Reference voltage (2V _{RO}) output terminal. 2V _{RO} = 4.2 V when V _{CC} = 5 V	—													
13	TEN	I	TE amp negative input terminal.	Connected to TEO through feedback resistor.													
14	TEO	O	TE error signal output terminal.	—													
15	RFDC	O	RF signal peak detect output terminal.	—													
16	FEO	O	Focus error signal output terminal.	—													
17	FEN	I	FE amp negative input terminal.	Connected to FEO through feedback resistor.													
18	SEB	I	RFRP output circuit switching terminal. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>SEB Level</th> <th>Bottom Detection</th> <th>Peak Detection</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>ON</td> <td rowspan="2">ON</td> </tr> <tr> <td>V_{CC}</td> <td>OFF</td> </tr> </tbody> </table>	SEB Level	Bottom Detection	Peak Detection	GND	ON	ON	V _{CC}	OFF	Low (GND) is for normal use.					
SEB Level	Bottom Detection	Peak Detection															
GND	ON	ON															
V _{CC}	OFF																
19	V _{RO}	O	Reference voltage (V _{RO}) output terminal. V _{RO} = 2.1 V when V _{CC} = 5 V	—													

Pin No.	Symbol	I/O	Functional Description	Remarks							
20	RFRP	O	Track count signal output terminal.	—							
21	BTC	I	Time constant adjustment terminal for bottom detection.	Adjusted by capacitance.							
22	RFCT	O	RFRP signal center level output terminal.	—							
23	PKC	I	Time constant adjustment terminal for peak detection.	Adjusted by capacitance.							
24	RFRPIN	I	Input terminal for track count signal output amp.	—							
25	RFGO	O	Output terminal for RF signal amplitude adjustment amp.	—							
26	GVSW	I	Amp (FE, TE) gain switching terminal. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>GVSW</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>CD-RW</td> </tr> <tr> <td>HiZ</td> <td rowspan="2">Normal</td> </tr> <tr> <td>V_{CC}</td> </tr> </tbody> </table>	GVSW	Mode	GND	CD-RW	HiZ	Normal	V _{CC}	Low (GND) is for 5 times gain.
GVSW	Mode										
GND	CD-RW										
HiZ	Normal										
V _{CC}											
27	AGCIN	I	Input terminal for RF signal amplitude adjustment amp.	Connected to RFO through capacitance.							
28	RFO	O	Output terminal for RF signal amp.	—							
29	GND	—	Ground terminal.	—							
30	RFN2	I	Input terminal for RF signal amp.	—							

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	8	V
Power dissipation	P _D	500	mW
Operating temperature	T _{opr}	-40~85	°C
Storage temperature	T _{stg}	-55~150	°C

Electrical Characteristics

(unless otherwise specified, $V_{CC} = 5\text{ V}$, $T_a = 25^\circ\text{C}$, $RFGC = V_{CC}$, $GVSW = V_{CC}$)

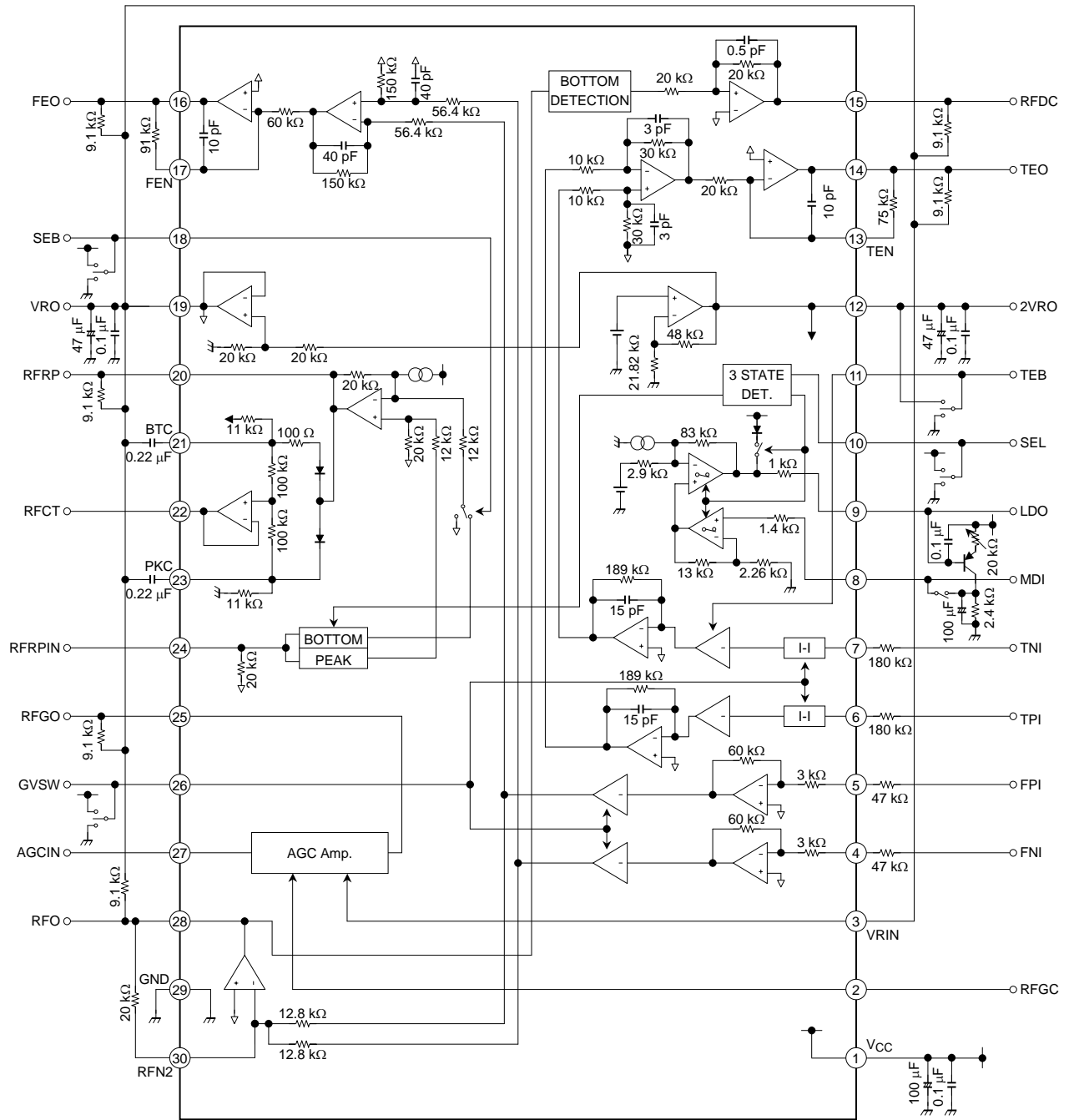
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Power supply	Assured power supply voltage	V_{CC}	—	—	4.5	5.0	5.5	V
	Power supply current 1 (normal mode)	I_{CC1}	—	SEL = HiZ REGC = HiZ	23	33	43	mA
	Power supply current 2 (CD-RW mode)	I_{CC2}						
Reference voltage (2VRO)	Reference voltage	2VR	—	—	4.0	4.2	4.4	V
	Output current	I_{OH2}	—	$\Delta V = -0.2\text{ V}$	2.0	—	—	mA
	Input current	I_{OL2}		$\Delta V = +0.1\text{ V}$				
Reference voltage (VRO)	Reference voltage	VR	—	—	2.0	2.1	2.2	V
	Reference voltage limit	ΔVR	—	$2 \times VR/2VR - 1$	-3.0	0.0	—	%
	Output current	I_{OH1}	—	$\Delta V = -0.2\text{ V}$	5.0	—	—	mA
	Input current	I_{OL1}		$\Delta V = +0.1\text{ V}$				
RF1	Transfer resistance1 (normal mode)	R_{T1}	—	f = 100 kHz Rf = 20 k Ω	153	180	207	k Ω
	Transfer resistance2 (CD-RW mode)	R_{T2}						
	Frequency band width1 (normal mode)	fc1	—	-3dB point Rf = 20 k Ω	—	8	—	MHz
	Frequency band width2 (CD-RW mode)	fc2						
	Output slew rate	SR	—	$C_{RFO} = 20\text{ pF}$	—	20	—	V/ μs
	Output offset voltage 1 (normal mode)	V_{OS1}	—	VR Reference Rf = 20 k Ω Input: Open	—	-50	—	mV
	Output offset voltage 2 (CD-RW mode)	V_{OS2}						
	Upper limit output voltage	V_{OH}	—	GND Reference	3.8	—	—	V
	Lower limit output voltage	V_{OL}						
	Permissible load resistance	R_{LM}	—	—	10	—	—	k Ω
RF2 (AGC)	Lower limit voltage gain	G_{VL}	—	f = 100 kHz	0.6	0.7	0.8	V/V
	Upper limit voltage gain	G_{VH}						
	Frequency band width	fc	—	-3dB point	—	20	—	MHz
	Output slew rate	SR	—	$C_{RFO} = 20\text{ pF}$	—	20	—	V/ μs
	Output offset voltage	V_{OS}	—	VR Reference, Input: Open	—	100	—	mV
	Upper limit output voltage	V_{OH}	—	GND Reference	3.8	—	—	V
	Lower limit output voltage	V_{OL}						
	Permissible load resistance	R_{LM}	—	—	10	—	—	k Ω
APC	Voltage gain	Gv	—	f = 1 kHz	—	200	—	V/V
	Operation ref. Voltage	V_{MDI}	—	$V_{LDO} = 3.5\text{ V}_{DC}$	170	178	192	mV
	LD off voltage	V_{LDOP}	—	SEL = GND, V_{CC} Reference	-0.7	—	—	V
	Input bias current	I_i	—	MDI = 178 mV	-200	—	200	nA

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit		
FE	Transfer resistance 1 (normal mode)	R_{T1}	—	$f = 1 \text{ kHz}$ $R_{NF} = 91 \text{ k}\Omega$	$GVSW = V_{CC}$	197	232	267	$\text{k}\Omega$	
	Transfer resistance 2 (CD-RW mode)	R_{T2}			$GVSW = GND$	0.89	1.05	1.20	$\text{M}\Omega$	
	Gain balance 1 (normal mode)	GB1	—	$f = 1 \text{ kHz}$ $R_{NF} = 91 \text{ k}\Omega$	$GVSW = V_{CC}$	-1.0	—	1.0	dB	
	Gain balance 2 (CD-RW mode)	GB2			$GVSW = GND$	-1.0	—	1.0		
	Frequency band width1 (normal mode)	f_{c1}	—	-3dB point $R_{NF} = 91 \text{ k}\Omega$	$GVSW = V_{CC}$	—	26.5	—	kHz	
	Frequency band width2 (CD-RW mode)	f_{c2}			$GVSW = GND$	—	26.5	—		
	Output offset voltage 1 (normal mode)	V_{OS1}	—	$R_{NF} = 91 \text{ k}\Omega$ VR Reference	$GVSW = V_{CC}$	-20	—	20	mV	
	Output offset voltage 2 (CD-RW mode)	V_{OS2}			$GVSW = GND$	-50	—	50		
	Upper limit output voltage	V_{OH}	—	GND Reference		3.8	—	—	V	
	Lower limit output voltage	V_{OL}				—	—	0.5		
	Permissible load resistance	R_{LM}	—	—		10	—	—	$\text{k}\Omega$	
TE	Transfer resistance 1 (normal mode)	R_{T1}	—	$f = 1 \text{ kHz}$ $R_{NF} = 75 \text{ k}\Omega$ TEB = HiZ	$GVSW = V_{CC}$	1.81	2.13	2.45	$\text{M}\Omega$	
	Transfer resistance 2 (CD-RW mode)	R_{T2}			$GVSW = GND$	8.15	9.59	11.02		
	Voltage gain adjustable range	max voltage ratio	ΔGv	—	T_{NI} input $R_{NF} = 75 \text{ k}\Omega$ TEB = VR Reference	TEB = GND	—	45	—	%
		min voltage ratio				TEB = 2VR	—	-45	—	
	Gain balance 1 (normal mode)	GB1	—	$f = 1 \text{ kHz}$ $R_{NF} = 75 \text{ k}\Omega$ TEB = VR	$GVSW = V_{CC}$	-1.0	—	1.0	dB	
	Gain balance 2 (CD-RW mode)	GB2			$GVSW = GND$	-1.0	—	1.0		
	Frequency band width1 (normal mode)	f_{c1}	—	-3dB point $R_{NF} = 75 \text{ k}\Omega$	$GVSW = V_{CC}$	—	44	—	kHz	
	Frequency band width2 (CD-RW mode)	f_{c2}			$GVSW = GND$	—	44	—		
	Output offset voltage 1 (normal mode)	V_{OS1}	—	$R_{NF} = 75 \text{ k}\Omega$ VR Reference	$GVSW = V_{CC}$	-80	—	80	mV	
	Output offset voltage 2 (CD-RW mode)	V_{OS2}			$GVSW = GND$	-300	—	300		
	Upper limit output voltage	V_{OH}	—	GND Reference		3.8	—	—	V	
Lower limit output voltage	V_{OL}				—	—	0.5			
Permissible load resistance	R_{LM}	—	—		10	—	—	$\text{k}\Omega$		
RFDC FNI (FPI) → RFDC	Detection frequency	f_c	—	—	—	40	—	kHz		
	Upper limit output voltage	V_{OH}	—	GND Reference		3.3	—	—	V	
	Lower limit output voltage	V_{OL}				—	—	0.9		
	Permissible load resistance	R_{LM}	—	—		10	—	—	$\text{k}\Omega$	

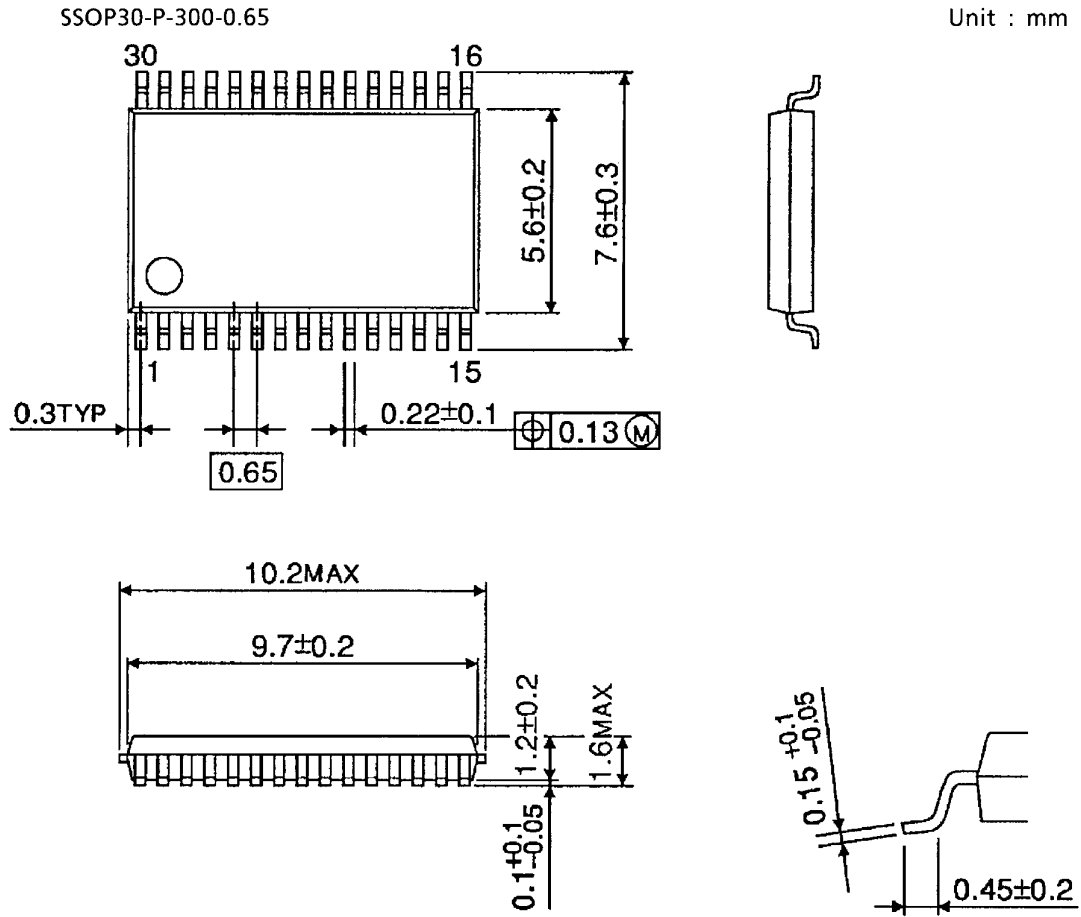
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
RFRP	Voltage gain	Gv	—	—	—	1.7	—	V/V
	Detection frequency characteristic 1	fc1	—	SEL = HiZ	—	100	—	kHz
	Detection frequency characteristic 2	fc2		SEL = V _{CC}	—	200	—	
	Operation reference voltage 1	V _{OPR1}	—	VR Reference No Input	-1.1	-1.0	-0.9	V
	Operation reference voltage 2	V _{OPR2}		VR Reference 700 kHz, 1.2 Vp-p	0.7	0.8	0.9	
	Permissible load resistance	R _{LM}	—	—	10	—	—	kΩ
RFCT	Detection frequency characteristic 1	fc1	—	C _{BTC} = 0.22 μF	—	70	—	Hz
RFRP →RFCT	Detection frequency characteristic 2	fc2		C _{PKC} = 0.22 μF	—	70	—	
	Output offset voltage	V _{OS}	—	RFRP Reference, RFCT	-50	—	50	mV

Note: If the IC is used abnormally (ex. wrongly mounted), it may be damaged or destroyed.

Test Circuit



Package Dimensions



Weight: 0.17 g (typ.)

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000707EBA

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