

## PLL with I<sup>2</sup>C Bus for AM/FM Receivers

SDA 2121-2

Preliminary Data

CMOS IC

### Features

- High input sensitivity (50 mV<sub>rms</sub> on FM and 30 mV<sub>rms</sub> on AM)
- High input frequencies (150 MHz on FM and 25 MHz on AM)
- Extremely fast phase detector with very short anti-backlash pulses
- I<sup>2</sup>C bus
- Large divider ratios:
  - 16 Bit N divider
  - 16 Bit R divider
  - Divider factor without vacancy
- Adjustable raster width (< 1 kHz for AM, < 12.5 kHz for FM)\*
- Two-pin oscillator provides connection of a piezoelectric crystal for reference frequency generation
- Switchable phase detector polarity
- Switchable phase detector current
- One phase detector output each for FM and AM with the corresponding analog phase detector outputs
- Open drain switching outputs for 10 V

OSC IN 2-65535  
AM IN 2-65535  
FM IN /2 2-65535

Type	Ordering Code	Package
SDA 2121-2	Q67100-H5025	P-DIP-20
SDA 2121-2X	Q67100-H5026	P-DSO-20

Raster width = Input frequency / divider factor  
[On FMIN input frequency / 2 is to be used due to the prescaler]

The SDA 2121-2 is an integrated circuit in CMOS technology which has been especially designed for application in radio equipment.

The SDA 2121-2 is a complex PLL component in CMOS technology for processor controlled frequency synthesis.

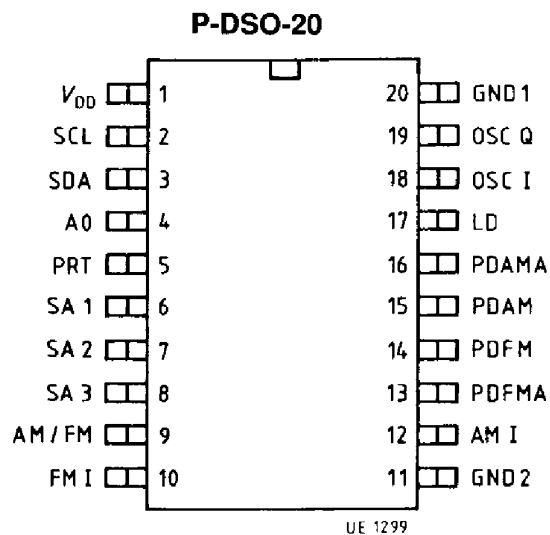
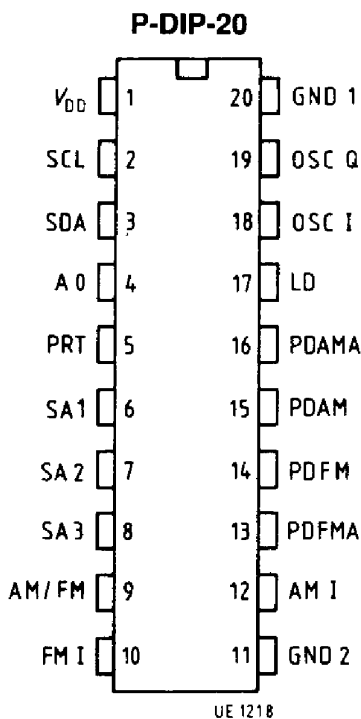
Function and dividing ratios are selected via an I<sup>2</sup>C bus interface (licensed by Philips) at pins SCL, SDA and A0. The chip address is set via address input A0. Thus it is possible to address two components via the I<sup>2</sup>C bus. The reference frequency can be applied at input OSC IN or it can be generated internally by a piezoelectric crystal. Its maximum value is 15 MHz. The VCO frequency is applied at input FM or AM respectively. Its maximum value is 150 MHz at the FM input and 25 MHz at the AM input. The FM input signal is divided by two by an asynchronous prescaler.

Outputs PDFM and PDAM supply the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Polarity and current of the PD outputs can be switched. The component also has corresponding analog phase detector outputs and lock-detect output (LD).

Additional outputs are the open-drain switching outputs (SA 1, 2, 3, AM/FM) with a dielectric strength of 10 V and a port output (PRT).

**Pin Configuration**

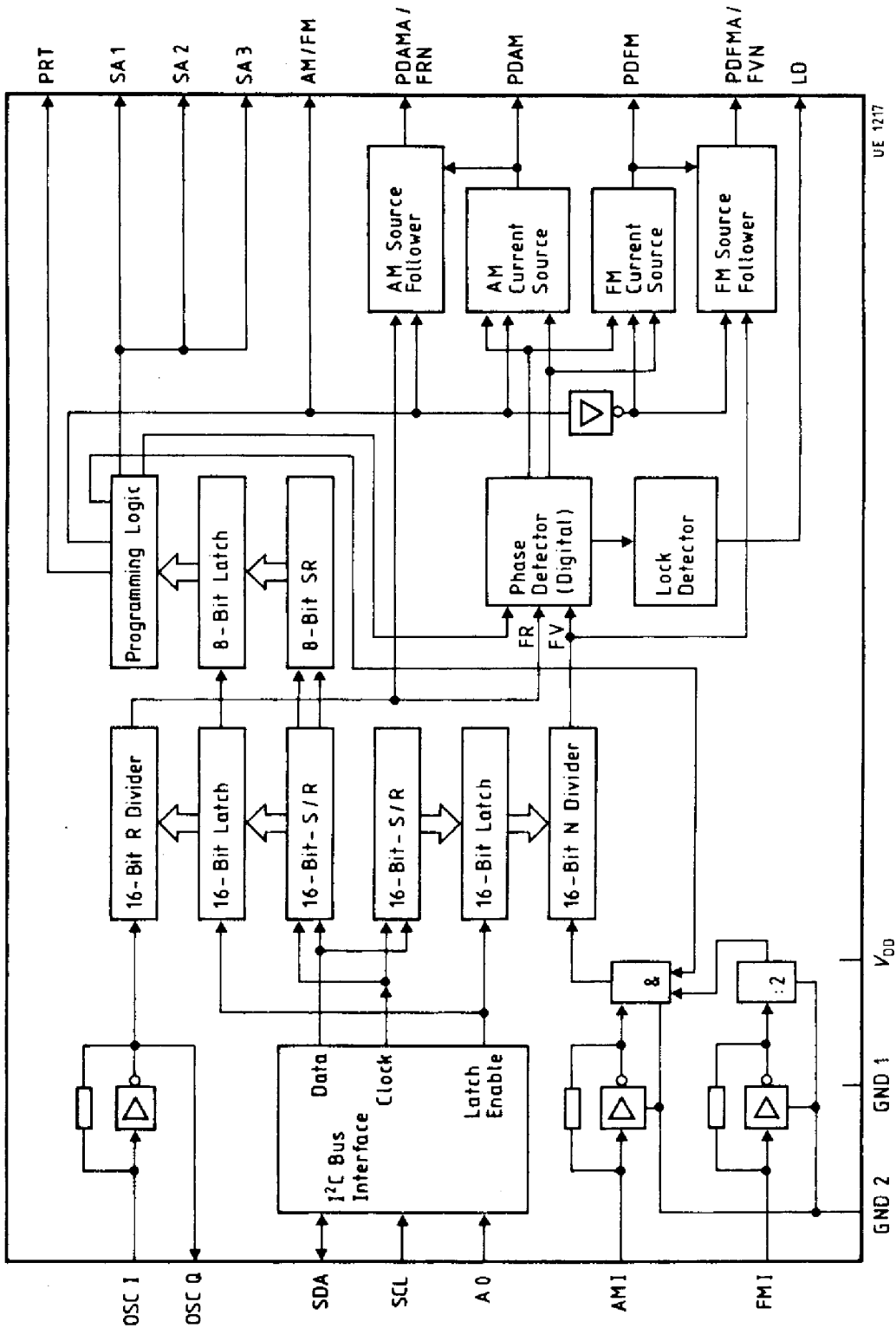
(top view)



### Pin Definitions and Functions

Pin No.	Symbol	Function
1	V <sub>DD</sub>	Supply voltage
2	SCL	I <sup>2</sup> C bus clock
3	SDA	I <sup>2</sup> C bus data input and acknowledge output
4	A0	Address input
5	PRT	Port output
6	SA 1	Switch output (open drain output for 10 V)
7	SA 2	Switch output (open drain output for 10 V)
8	SA 3	Switch output (open drain output for 10 V)
9	AM/FM	Switch output (open drain output, 10 V) switching AM/FM operation
10	FM I	FM input
11	GND2	Ground connection for AM and FM input amplifier
12	AMI	AM input
13	PDFMA	Analog output corresponding to the phase detector output, in test operation open drain output of FRN and FVN signal
14	PDFM	Phase detector output for AM or FM active or tristate depending on operating mode
15	PDAM	Phase detector output for AM or FM active or tristate depending on operating mode
16	PDAMA	Analog output corresponding to the phase detector output, in test operation open drain output of FRN and FVN signal
17	LD	Lock-detect output
18	OSCI	Connection for reference oscillator input and output
19	OSCQ	Connection for reference oscillator input and output
20	GND1	Ground

Block Diagram



**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	$V_{DD}$	- 0.3		6	V
Input voltage	$V_I$	- 0.3		$V_{DD} + 0.3$	V
Power dissipation per output	$P_Q$			10	mW
Total power dissipation	$P_{tot}$			300	mW
Storage temperature	$T_{stg}$	- 40		125	°C
Output voltage switch outputs	$V_{QH}$			10.5	V

**Operating Range**

Supply voltage	$V_{DD}$	4.5	5	5.5	V
Supply current	$I_{DD}$		6	10	mA
Ambient temperature	$T_A$	-25		85	°C
Output voltage switch outputs	$V_{QH}$			10	V

## Test conditions for supply voltage

- $V_{DD} = 5.5$  V
- $T_A = 25^\circ\text{C}$  outputs not connected
- No test operation
- Max. permissible operating frequency on AM, FM, OSC IN = 15 MHz
- $V_{IFM}, V_{IAM}, V_{IOSCIN} = 100$  mVrms
- Minimal divider ratios
- PLL in in-lock condition

**Characteristics** $T_A = 25\text{ }^\circ\text{C}$ ; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input Signals SCL, SDA, A0**

H-input voltage	$V_{IH}$	$0.7 \times V_{DD}$		$V_{DD}$	V	$V_I = V_{DD}$
L-input voltage	$V_{IL}$	0		1.5	V	
Input capacitance	$C_I$			10	pF	
Input current	$I_I$			10	$\mu\text{A}$	

**Input Signal OSC IN**

Input frequency	$f$			15	MHz	$V_{DD} = 4.5\text{ V}$ (sine wave)
Input voltage	$V_I$	100			mVrms	
Input capacitance	$C_I$			10	pF	$V_I = V_{DD}$
Input current	$I_I$			30	$\mu\text{A}$	

**Input Signal AM**

Input frequency	$f$	0.5		25	MHz	$V_{DD} = 4.5\text{ V}$ (sine wave)
Input voltage	$V_I$	30			mVrms	
Input capacitance				10	pF	$V_I = V_{DD}$
Input current	$I_I$			30	$\mu\text{A}$	

**Input Signal FM**

Input frequency	$f$	10		150	MHz	$V_{DD} = 4.5\text{ V}$ (sine wave)
Input voltage	$V_I$	50			mVrms	
Input capacitance	$C_I$			10	pF	$V_I = V_{DD}$
Input current	$I_I$			30	$\mu\text{A}$	

**Characteristics (cont'd)** $T_A = 25\text{ }^\circ\text{C}$ ; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Output signal PDFM (tristate output)**

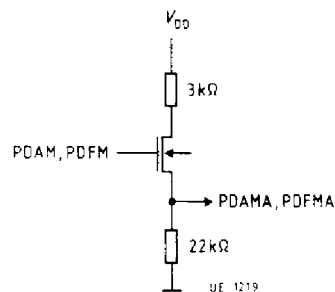
PD current value A	$I_{\alpha}$	340	$\pm 570$	800	$\mu\text{A}$	$V_{DD} = 5\text{ V}$
PD current value B	$I_{\alpha}$	85	$\pm 145$	205	$\mu\text{A}$	$T_A = -25\text{ }^\circ\text{C} \dots 60\text{ }^\circ\text{C}$
PD leakage current	$I_{\alpha}$		$\pm 50$	500	nA	

**Output Signal PDAM (tristate output)**

PD current value A	$I_{\alpha}$	70	$\pm 115$	160	$\mu\text{A}$	$V_{DD} = 5\text{ V}$
PD current value B	$I_{\alpha}$	15	$\pm 30$	45	$\mu\text{A}$	$T_A = -25\text{ }^\circ\text{C} \dots 60\text{ }^\circ\text{C}$
PD leakage current	$I_{\alpha}$		$\pm 50$	500	nA	no load at the output

**Output Signal PDAMA, PDFMA (analog output)**

H-output current	$I_{QH}$		1	2.5	mA	$V_{PD} = V_{DD} = 5\text{ V}$
L-output current	$I_{QL}$	0.1	0.5		mA	$V_{PD} = \text{GND}$

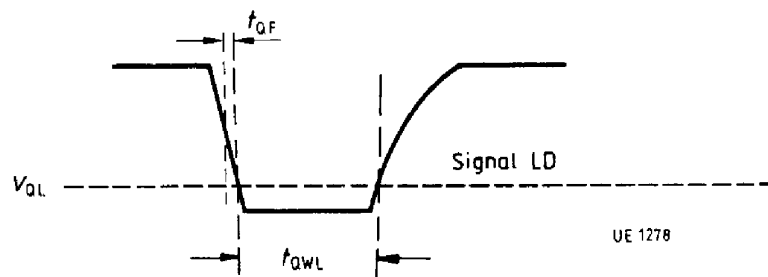


**Characteristics (cont'd)** $T_A = 25\text{ }^\circ\text{C}$ ; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Output Signal LD (open drain output)**

L-output signal	$V_{OL}$			0.4	V	$I_{OL} = 3\text{ mA}$ $V_{DD} = 5\text{ V}$ $C_L = 20\text{ pF}$
L-output pulse width	$t_{QWL}$		30		ns	



UE 1278

**Output Signal PRT**

H-output voltage	$V_{OH}$	$V_{DD} - 0.4$			V	$I_{OH} = 1\text{ mA}$
L-output voltage	$V_{OL}$			0.4	V	$I_{OL} = 1\text{ mA}$
	$V_{OL}$			0.1	V	$I_{OL} = 0.1\text{ mA}$

**Output Signal SA 1, 2, 3 and FM (open drain switching outputs)**

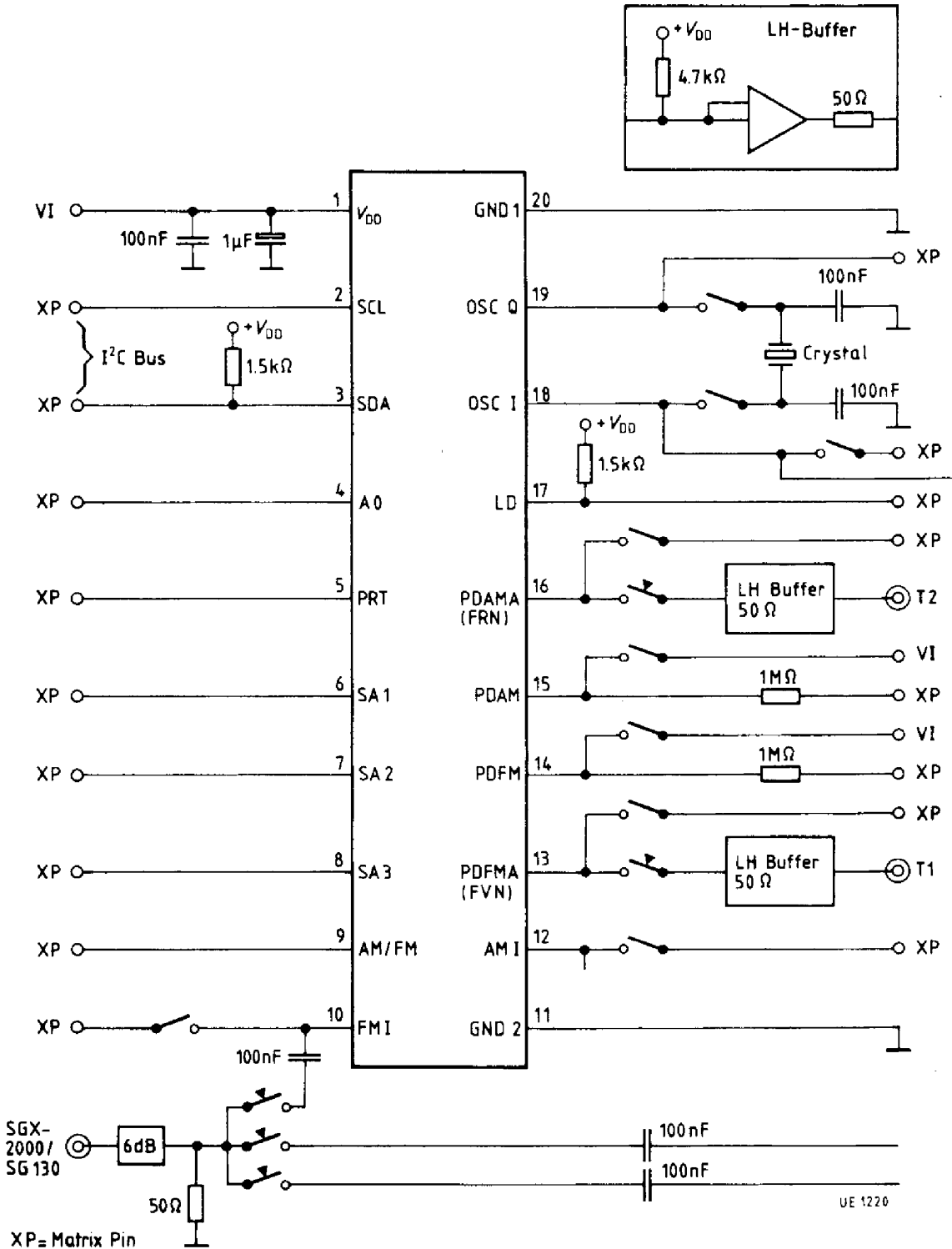
L-output voltage	$V_{OL}$			0.4	V	$I_{OL} = 1\text{ mA}$ $V_{DD} = 5\text{ V}$
	$V_{OL}$			0.1	V	$I_{OL} = 0.1\text{ mA}$

**Output Signal SDA**

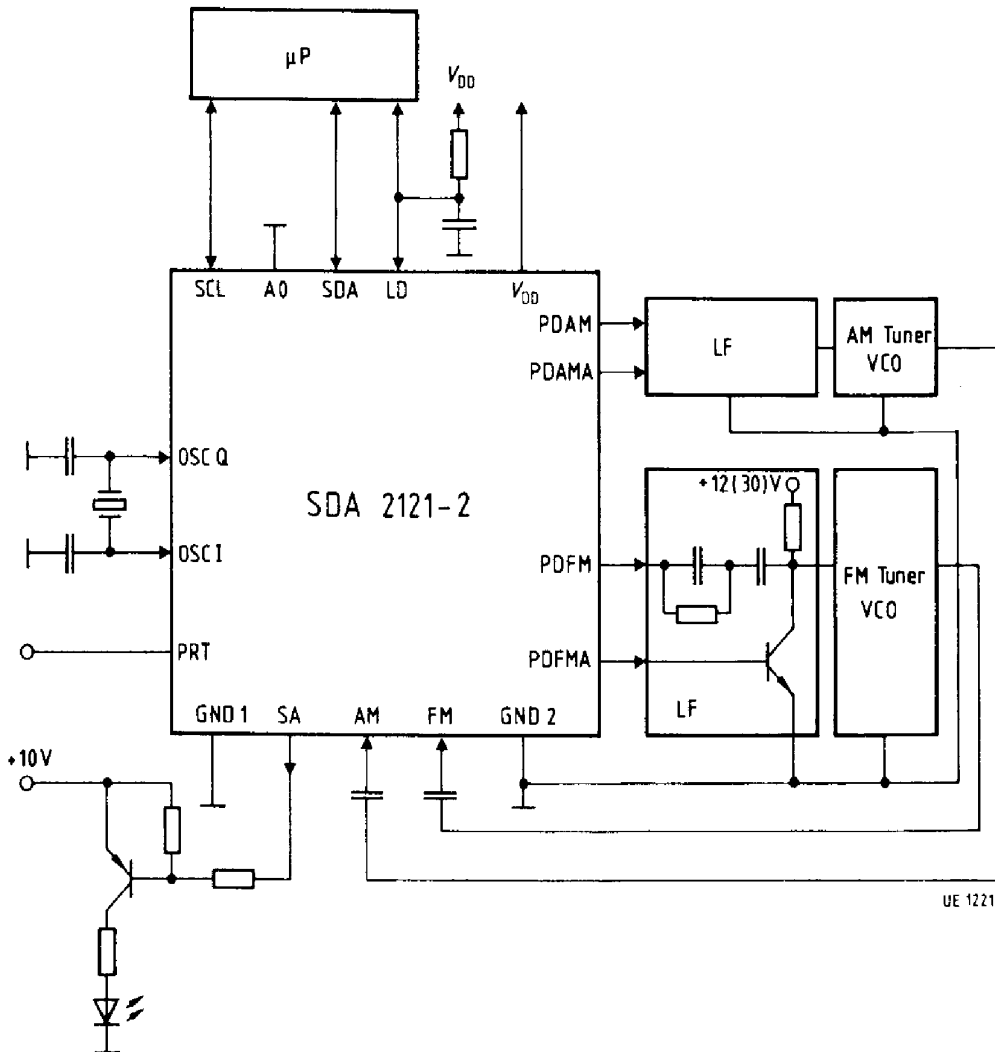
L-output voltage	$V_{OL}$			0.4	V	$I_{OL} = 3\text{ mA}$ $V_{DD} = 5\text{ V}$ $C_L = 400\text{ pF}$
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Test Circuit



Application Circuit



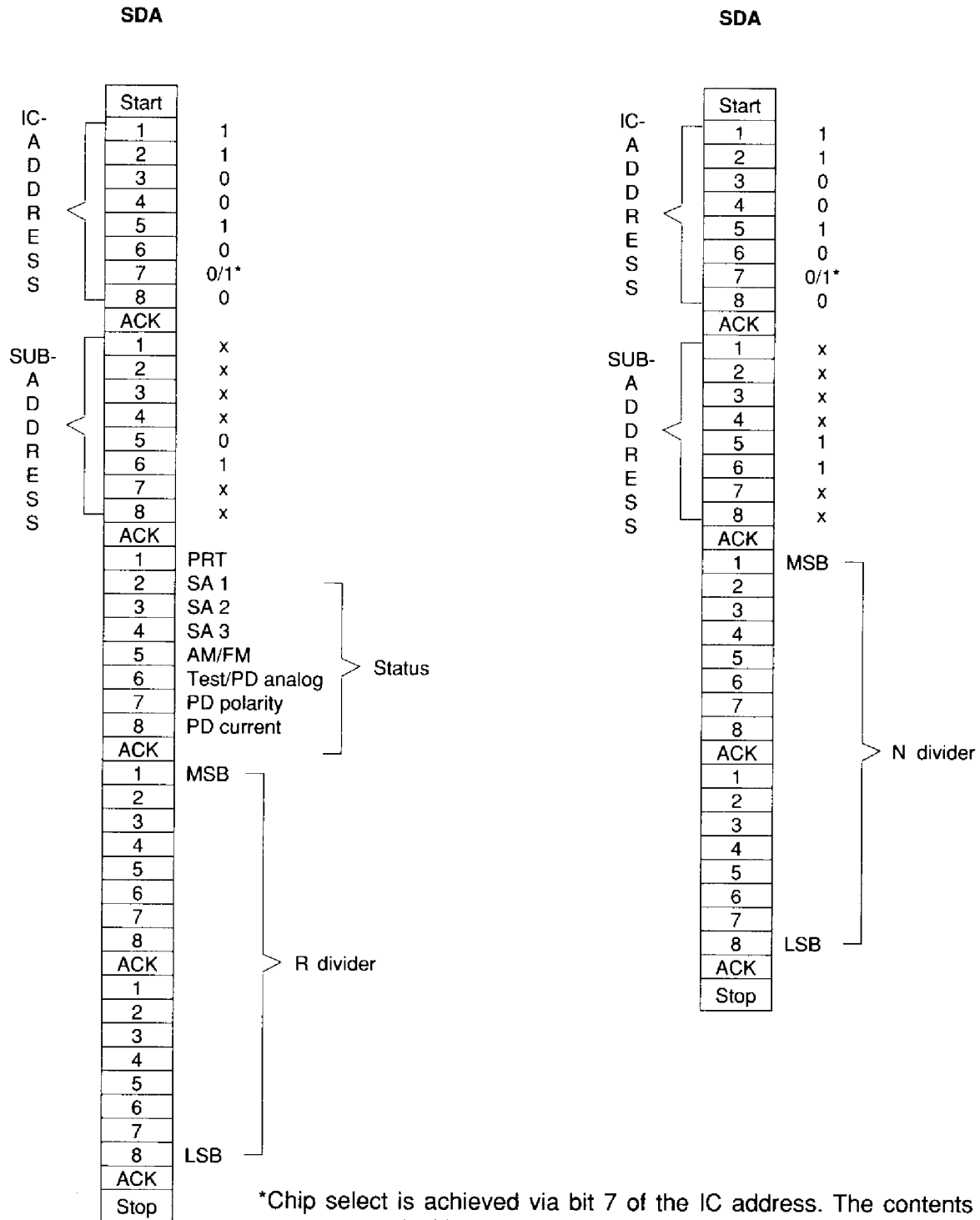
**Diagram****Status Programming Table**

Bit		Status Bit	
		0	1
1	PRT	L	H
2	SA 1	L	H
3	SA 2	L	H
4	SA 3	L	H
5	AM/FM	L (FM operation)	H (AM operation)*
6	PD analog/test	PD analog	test**
7	PD polarity	neg.	pos.
8	PD current	value B	value A (AM or FM operation)

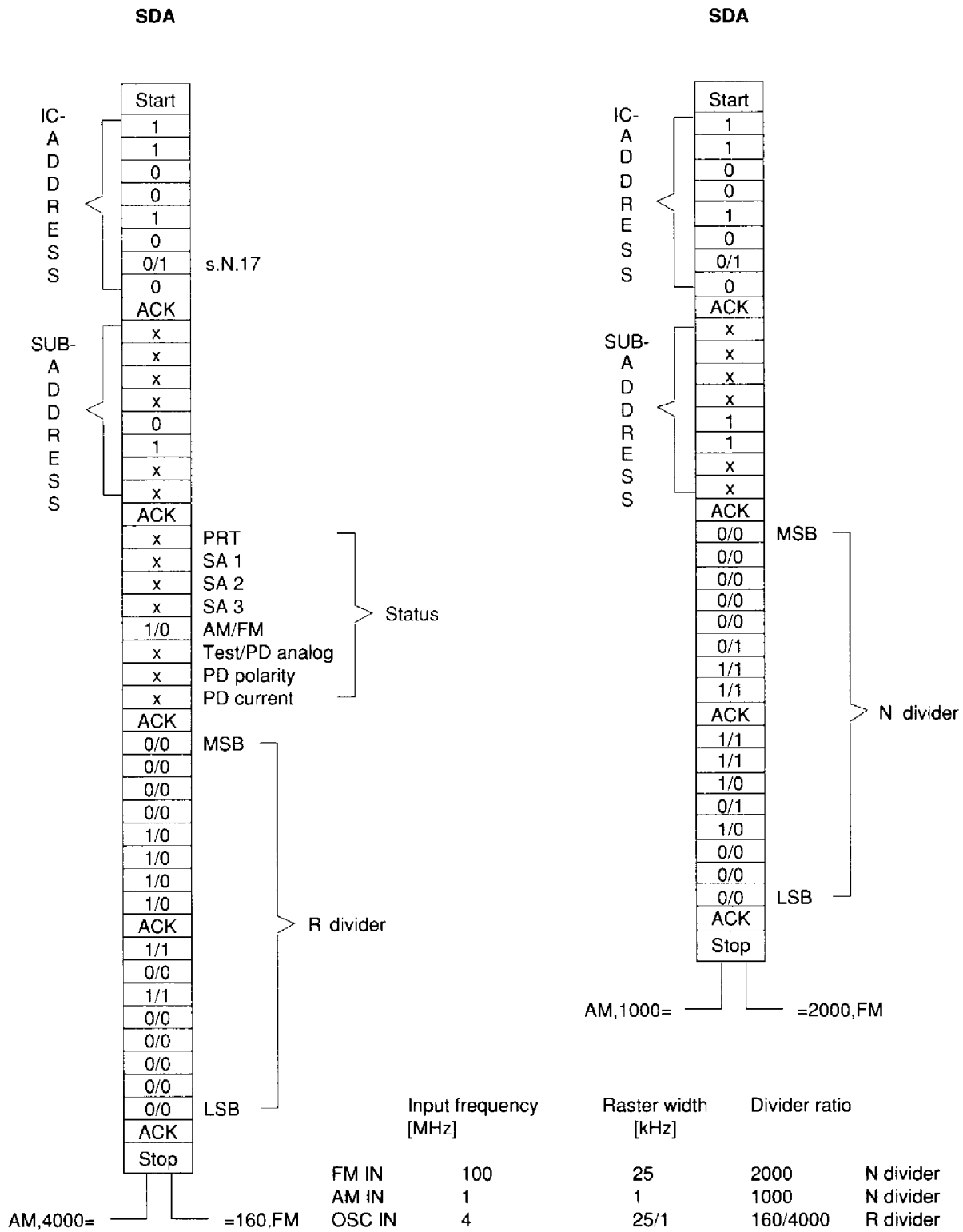
\*When the switch output FM is switched from "H" to "L" via bit 5 (FM), operation is switched from AM to FM  
PDAM is in tristate and vice versa

\*\*In test operation PDFMA and PDAMA outputs are switched as FVN and FRN outputs respectively

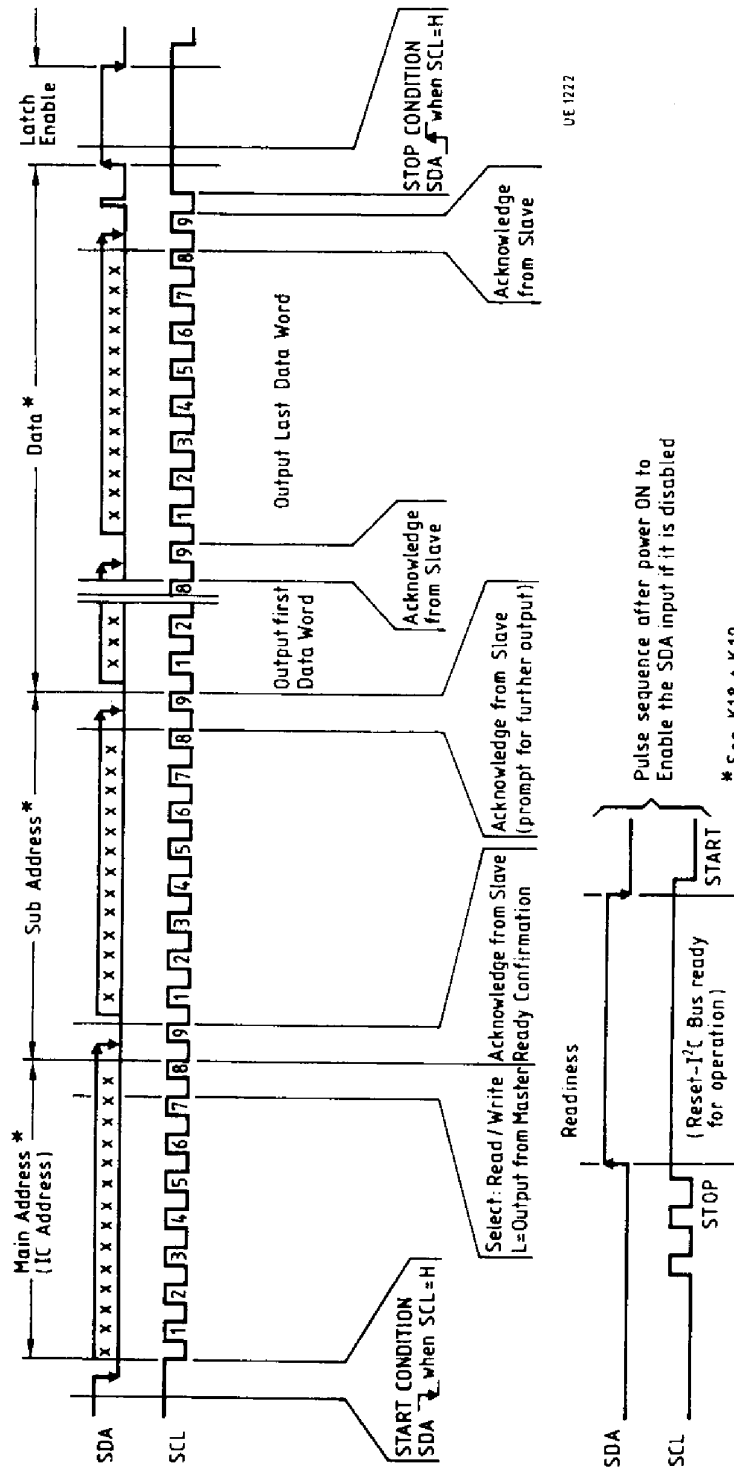
I<sup>2</sup>C Bus Transfer Protocol

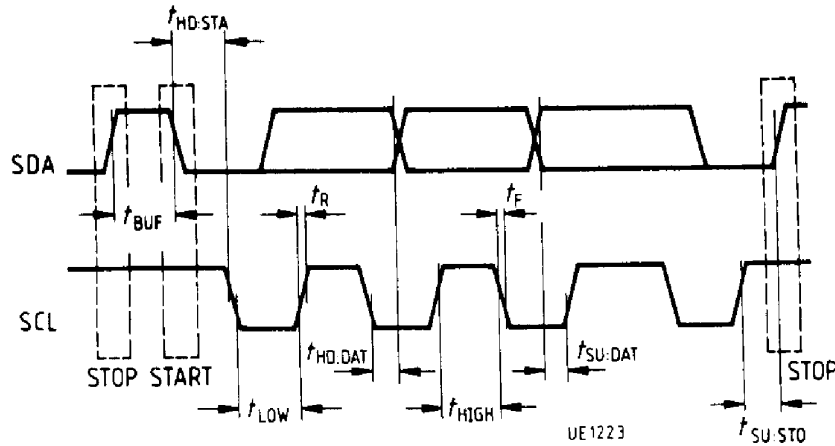


Programming Example



Transfer Protocol for I<sup>2</sup>C Bus



I<sup>2</sup>C Bus Timing, PRT, SA, AM/FM

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	$f_{SCL}$	0	100	kHz
Hold time data to SCL <sub>LOW</sub>	$t_{HD:DAT}$	0		μs
Inactive time prior to next transfer	$t_{BUF}$	4.7		μs
Hold time during start condition (first CLOCK pulse is generated after this time period)	$t_{HD:STA}$	4.0		μs
LOW clock phase	$t_{LOW}$	4.7		μs
HIGH clock phase	$t_{HIGH}$	4.0		μs
Set-up time for DATA	$t_{SU:DAT}$	250		ns
Rise time for SDA and SCL signal	$t_R$		1	μs
Fall time for SDA and SCL signal	$t_F$		300	ns
Set-up time for SCL clock during STOP condition	$t_{SU:STO}$	4.7		μs
PRT delay time relative to STOP condition	$t_D$		500	μs

All values are referenced to specified input levels  $V_{IH}$  and  $V_{IL}$ .

Pulse Diagram

Phase Detector/Lock Detector

