

## SDA 2112-2 TV PLL for 125 kHz Resolution

The SDA 2112-2 is fabricated in ASBC technology. In connection with a VCO (tuner) and a high-speed 1:64 divider, it forms a digitally programmable phase-locked loop for TV sets designed to use the PLL frequency synthesis tuning principle. The PLL enables crystal-controlled setting of the tuner oscillator frequency for a 125 kHz resolution in the frequency bands I/III, IV, and V.

A serial interface provides for simple connection to a microprocessor. The latter loads the programmable divider and the band-selection outputs with the appropriate information.

### Features

- No external integrator necessary
- Internal buffer
- Microprocessor compatible

**Maximum ratings**

Supply voltage pin 18	$V_{S1}$	-0.3 to 7.5	V
<b>Inputs</b> Q 1, Q 2, F, $\bar{F}$ pin 1, 2, 15, 16 CPL, IFO, PLE pin 7, 8, 10	$V_I$	-0.3 to $V_{S1} + 0.2$	V
	$V_I$	-0.3 to 5.5	V
<b>Outputs</b> UHF, VHF, Bd I/III pin 3, 4, 5 CLK (pin 6) $\overline{LDM}$ (pin 17) LOCK IND (pin 12) PD (pin 14) $V_D$ (pin 11) OSC (pin 13)  Junction temperature Storage temperature range  Thermal resistance (system-air)	$V_Q$	-0.3 to 16	V
	$V_6$	-0.3 to 16	V
	$I_6$	3	mA
	$V_{17}$	-0.3 to 7.5	V
	$I_{17}$	3	mA
	$V_{12}$	-0.3 to $V_{S1} + 0.2$	V
	$I_{14}$	1	mA
	$V_{11}$	-0.3 to 33	V
	$V_{13}$	-0.3 to $V_{S1} + 0.2$	V
	$I_{13}$	8	mA
	$T_j$	140	°C
	$T_{stg}$	-40 to 125	°C
	$R_{thSA}$	80	K/W

**Operating range**

Supply voltage range	$V_{S1}$	4.5 to 7.15	V
Input frequency	$f_{F, \bar{F}}$	16	MHz
Divider factor	$N$	256 to 8191	
Crystal frequency	$f_Q$	3	MHz
Tuning voltage	$V_D$	0.3 to 33	V
Ambient temperature	$T_A$	0 to 70	°C

**Characteristics** $V_{S1} = 5\text{ V}; T_A = 25\text{ }^\circ\text{C}$ 

	Test circuit	min	typ	max	
Supply current, pin 18	$I_{S1}$		20	35	mA
Oscillator output, pin 13 $R_{L2} = 3.5\text{ k}\Omega$	$V_{13H}$	4	4.5		V
OSC $R_{L2} = 3.5\text{ k}\Omega$	$V_{13L}$	4		0.7	V
<b>Signal inputs F/<math>\bar{F}</math>, pin 15, 16</b>					
Input voltage	$V_{15H}$	1	4.1	$V_{S1} + 0.2$	V
	$V_{15L}$	1	3.8	$V_{S1} - 0.1$	V
Input current	$I_{15}$	1		50	$\mu\text{A}$
$V_{15} = 5\text{ V}$					
Input sensitivity (peak-to-peak) Sine push-pull $f = 16\text{ MHz}$	$V_{15,16}$	1	300	1200	mV
<b>Bus inputs CPL, IFO, PLE, pin 7, 8, 10</b>					
Upper threshold voltage	$V_{7u}$	2	1.0	1.3	V
Lower threshold voltage	$V_{7l}$	2	0.5	0.7	V
Hysteresis	$\Delta V_7$	2		0.6	V
H input current	$I_{7H}$	2		8	$\mu\text{A}$
$V_{7H} = 5\text{ V}$					
L input current	$I_{7L}$	2	-50		$\mu\text{A}$
$V_{7L} = 0.4\text{ V}$					
<b>Band selection outputs UHF, VHF, Bd I/III pins 3, 4, 5</b>					
Reverse current	$I_{3H}$	3		10	$\mu\text{A}$
$V_{3H} = 15\text{ V}$					
Forward current (current drain) $2\text{ V} \leq V_3 \leq 15\text{ V}$	$I_{3L}$	3	0.8	1.7	mA
<b>Clock output CLK, pin 6</b>					
H output voltage	$V_{6H}$	4	14		V
$V_{S3} = 15\text{ V}$					
L output voltage	$V_{6L}$	4		1.5	V
$R_{L1} = 6.8\text{ k}\Omega$					
<b>Tuning section <math>V_D</math>, PD, pins 11, 14</b>					
Tuning voltage	$V_{11}$	5	0.3	32.5	V
$V_{S2} = 33\text{ V}$					
Charge-pump current PLL locked	$I_{14}$	5	-150	$\pm 100$	$\mu\text{A}$
PLL unlocked	$I_{14}$	5	-450	$\pm 300$	$\mu\text{A}$

**Characteristics (cont'd)** $V_{S1} = 15 \text{ V}; T_A = 25^\circ\text{C}$ **Lock indication, pin 12**

H output voltage

L output voltage

	Test circuit	min	typ	max	
$V_{12H}$	5	2.8			V
$V_{12L}$	5			0.4	V

**Carry synchronous divider LDM****Pin 17 (open collector)**

Reverse current

 $V_{17H} = 5 \text{ V}$ 

L output voltage

 $R_L = 5 \text{ k}\Omega$ 

$I_{17}$	1			10	$\mu\text{A}$
$V_{17L}$				0.4	V

**Switching times**

IFO, PLE

Set-up time

Hold time

CLK

H pulse width

L pulse width

HL transition time

 $R_{L1} = 6.8 \text{ k}\Omega$ 

LH transition time

 $C_{L1} = 50 \text{ pF}$ 

CPL

H pulse width

L pulse width

OSC

H pulse width

L pulse width

HL transition time

 $R_{L2} = 3.5 \text{ k}\Omega$ 

LH transition time

 $C_{L2} = 8 \text{ pF}$ 

$t_S$	2	2	1.5		$\mu\text{s}$
$t_H$	2	2	1.5		$\mu\text{s}$
$t_{TH}$	4		8.0		$\mu\text{s}$
$t_{TL}$	4		8.0		$\mu\text{s}$
$t_{THL}$	4	0		0.5	$\mu\text{s}$
$t_{TLH}$		0		1.5	$\mu\text{s}$
$t_{CH}$	2	2	1.5		$\mu\text{s}$
$t_{CLH}$	2	2	1.5		$\mu\text{s}$
$t_{OH}$	4	133			ns
$t_{OL}$	4			200	ns
$t_{OHL}$	4			20	ns
$t_{OLH}$	4			50	ns

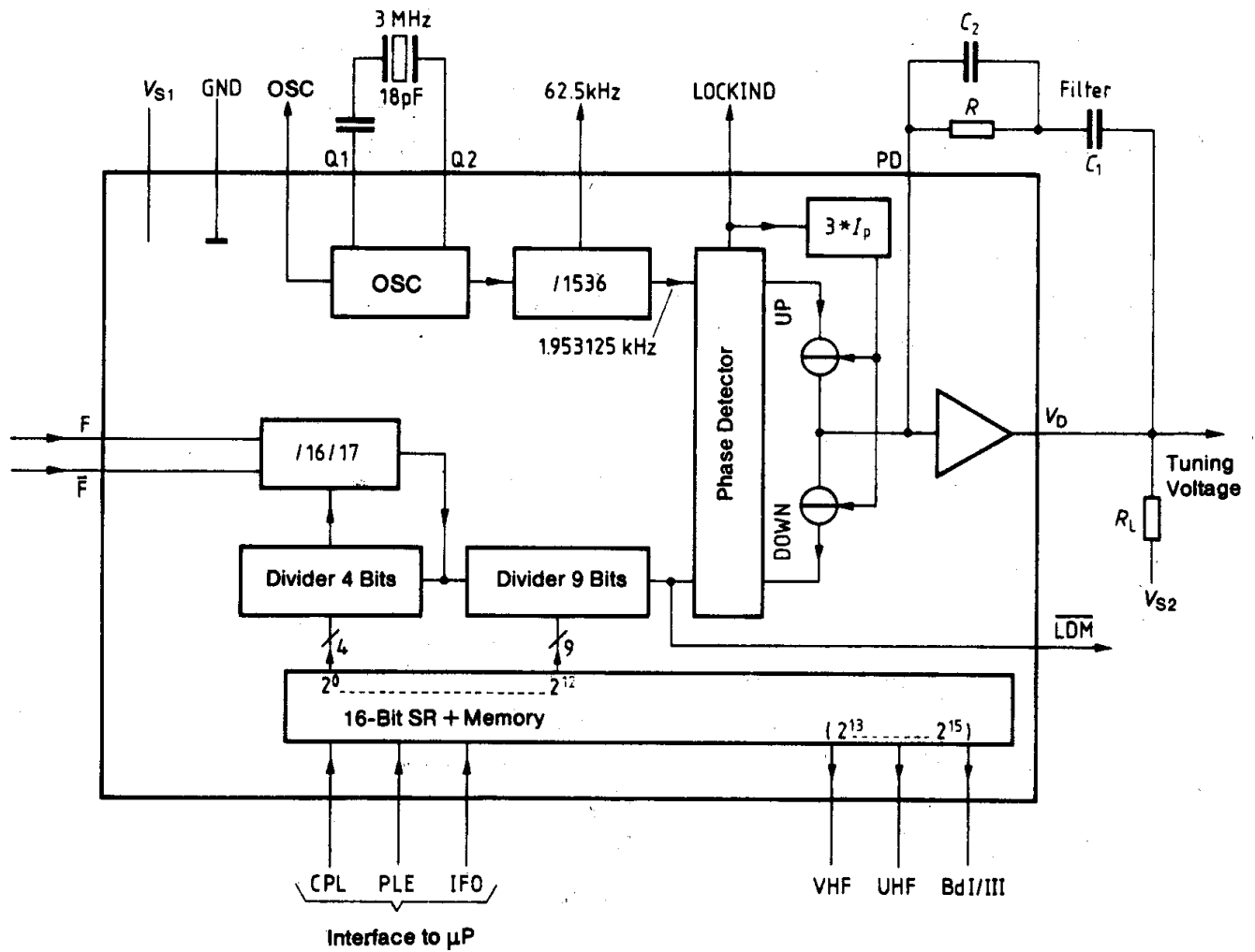
**Circuit description** (refer to block diagram)

- F,  $\bar{F}$**  A switchable 16/17 counter is triggered by the ECL signal inputs  $F/\bar{F}$ . The counter, in connection with a 4-bit and a 9-bit programmable, synchronous counter, forms a programmable, 13-bit synchronous divider using the dual-modulus technique, the 4-bit counter controlling the switchover from 16 to 17. Divider ratios of  $N = 256$  to 8191 are possible. For test purposes the carry of the synchronous divider is available at the  $\overline{\text{LDM}}$  output (open collector).
- $\overline{\text{LDM}}$**  The 16-bit shift register and latch is subdivided into 13 bits for storing the divider ratio  $N$  and 3 bits for controlling the three band-selection outputs.
- IFO**
- CPL** The telegram is shifted in via the serial data input IFO with the HL edge of the shift clock CPL when the enable input PLE is also on high level. First the complement of the divider ratio  $N$ , beginning with the LSB, is inserted in binary code, followed by the three control bits for the band-selection switching (see truth table). The 16-bit latch takes the data from the shift register when the enable input PLE is on low level.
- PLE**
- Q1, Q2** The IC includes a crystal-controlled, 3-MHz clock oscillator. The output signal is divided down to 1.953125 kHz (reference signal) by a 1/1536 reference divider.
- OSC** The oscillator frequency appears at the TTL output OSC.
- CLK** The clock of 62.5 kHz is available at the open-collector output CLK.
- PD** The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector turns to high level for the duration of this phase difference. In the reverse case the UP output turns to high level. If the two signals are in phase, both outputs remain at low level. The UP/DOWN outputs control the two current sources  $I^+$  and  $I^-$  (charge pump). If the two outputs are low (PLL locked), the charge-pump output PD will turn to the high-impedance state (TRISTATE).
- LOCK** An L signal appears at the LOCK IND output if frequency and phase are synchronous. The current sources  $I^+$  and  $I^-$  are then reduced from 300 to 100  $\mu\text{A}$ .
- IND**
- $V_D$**  The current pulses generated by the charge pump are integrated to form the tuning voltage by means of an active lowpass filter (external pull-up resistor to supply  $V_{S2}$  and external RC circuitry). The dc output signal appears at  $V_D$  and serves as a tuning voltage for the VCO.
- UHF** The band-selection outputs (UHF, VHF, Bd I/III) contain current drains with open collectors. In this way PNP transistors working as band-selection switches can be connected directly without current-limiting resistors (see application circuit).
- VHF**
- Bd I/III**

## Pin description

Pin	Symbol	Function
1	Q 2	Crystal
2	Q 1	Crystal
3	UHF	} Band selection outputs
4	VHF	
5	Bd I/III	
6	CLK	Clock output
7	CPL	Clock input
8	IFO	Data input
9	GND	Ground
10	PLE	Shift register enable input
11	$V_D$	Tuning voltage
12	LOCK IND	Lock indication output
13	OSC	Oscillator output
14	$V_{PD}$	Phase detector voltage
15	$\overline{F}$	Inverted input
16	F	Input
17	$\overline{LDM}$	Carry
18	$V_{S1}$	Supply voltage

Block diagram



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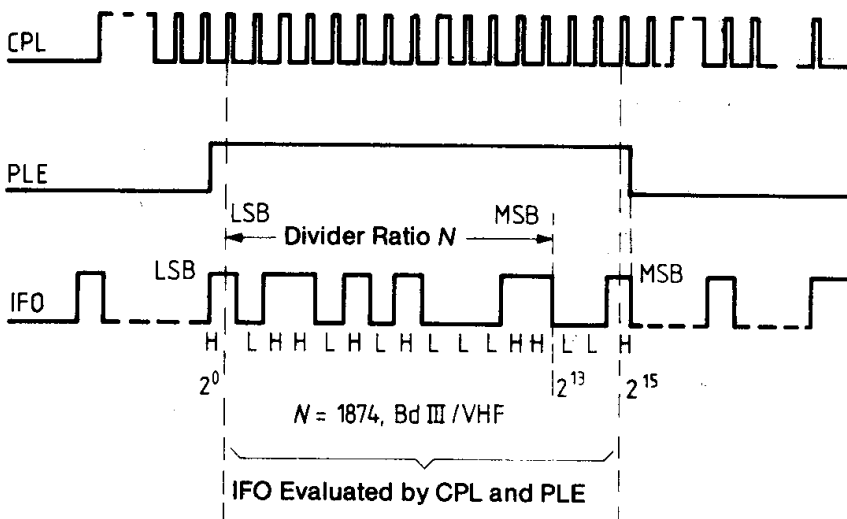


**Truth table**

Input "IFO" bit			Outputs			Meaning
$2^{13}$	$2^{14}$	$2^{15}$	Bd I/III	VHF	UHF	
H	H	L	H	H	L	"UHF"
H	L	H	H	L	H	"Bd I/VHF"
L	L	H	L	L	H	"Bd III/VHF"
L	H	H	L	H	H	"Bd III/VHF"

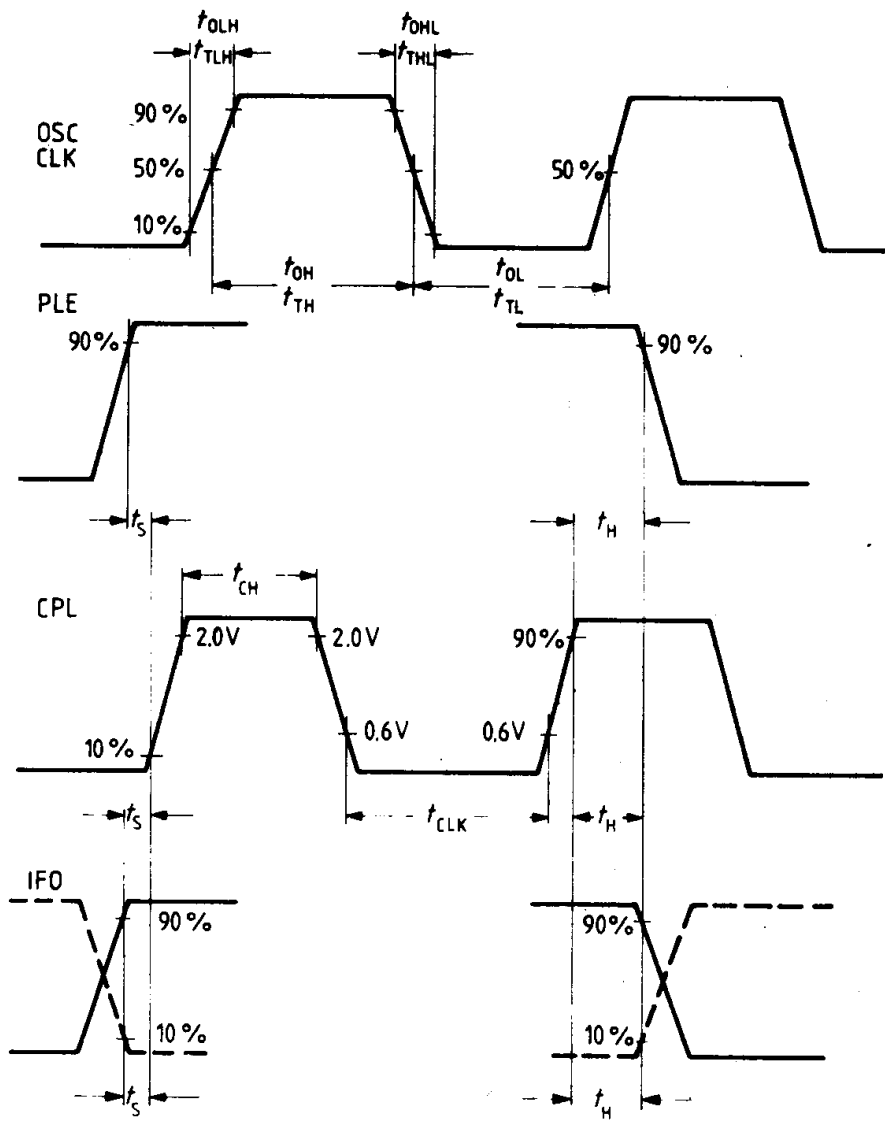
At positive logic, the "IFO" bits  $2^0 \dots 2^{12}$  complement the dual code from divider ratio  $N$ .

**Pulse diagram**

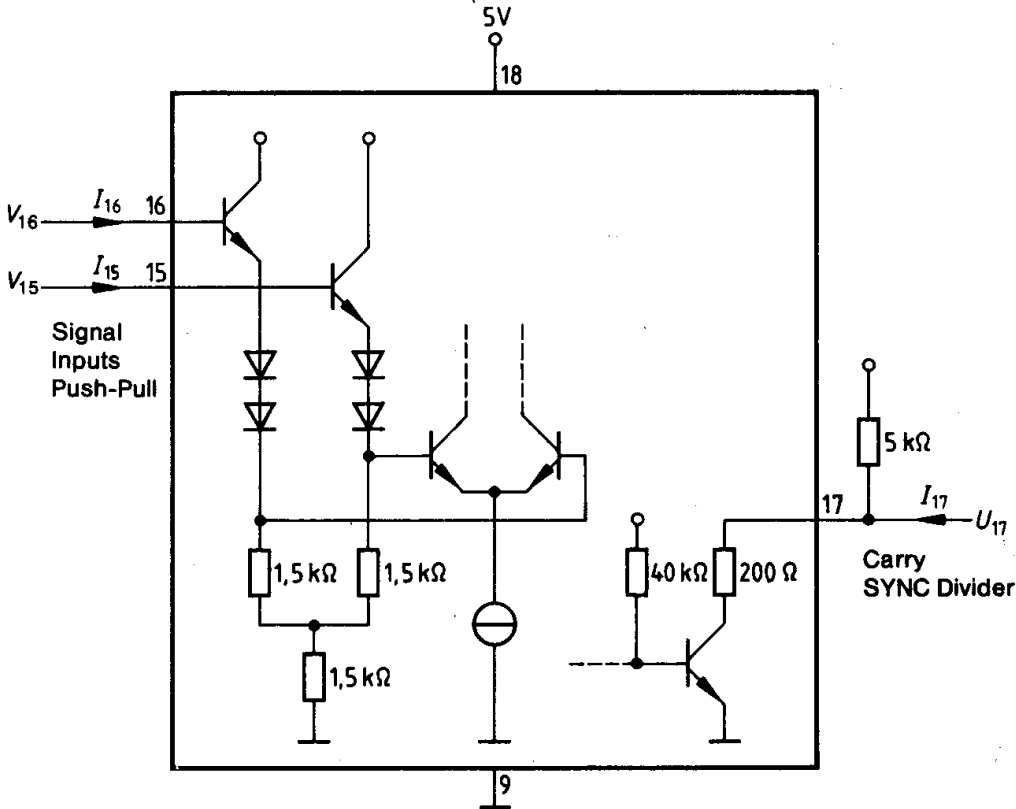


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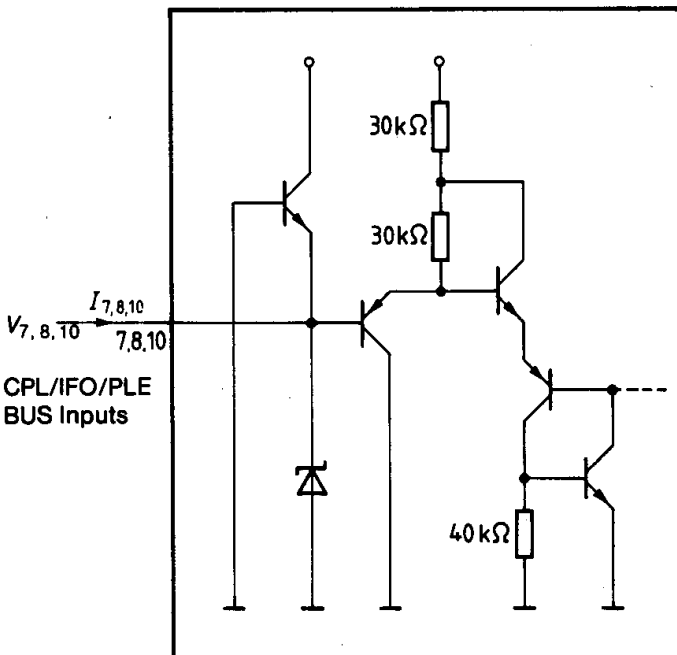
Pulse diagram



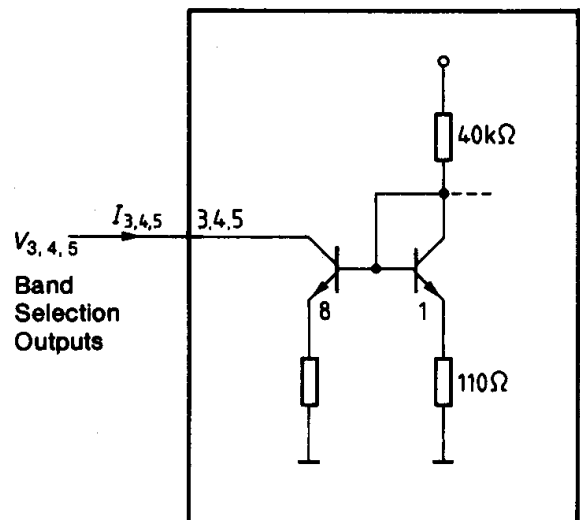
Test and measurement circuits



Test circuit 1

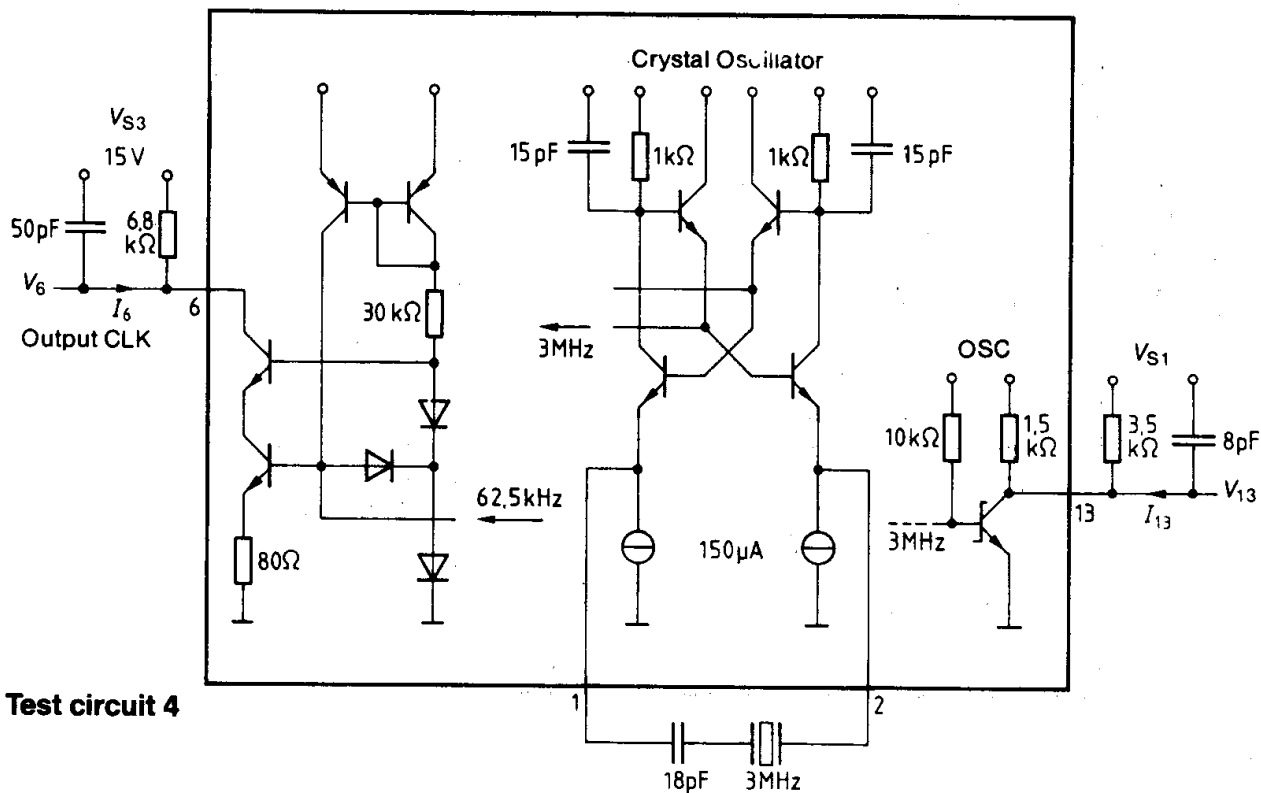


Test circuit 2

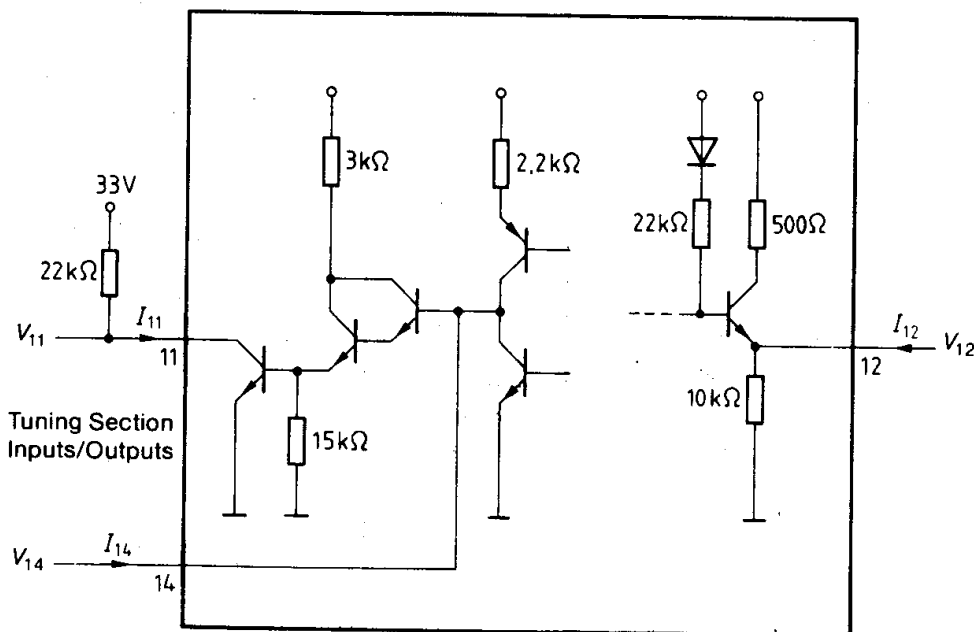


Test circuit 3

Test and measurement circuits



Test circuit 4



Test circuit 5