KSH13009L

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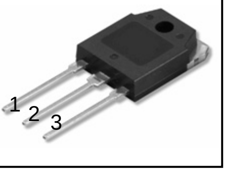
Switch Mode series NPN silicon Power Transistor

- High voltage, high speed power switching
- Suitable for switching regulator, inverters motor controls

12 Amperes
NPN Silicon Power Transistor
100 Watts

TO-3P
1. Base
2. Collector
3. Emitter



Absolute Maximum Ratings TC=25℃ unless otherwise noted

CHARACTERISTICS	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	700	V
Collector-Emitter Voltage	V_{CEO}	400	V
Emitter-Base Voltage	V_{EBO}	9	V
Collector Current(DC)	I_C	12	A
Collector Current(Pulse)	I_{CP}	24	A
Base Current	I_B	6	A
Collector Dissipation(Tc=25℃)	P_C	130	W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-65~150	℃

Electrical Characteristics TC=25℃ unless otherwise noted

CHARACTERISTICS	SYMBOL	Test Condition	Min	Typ.	Max	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}(sus)$	I_C=10mA, I_B=0	400			V
Emitter Cut-off Current	I_{EBO}	V_{EB}=9V,I_C=0			1	mA
*DC Current Gain	h_{FE1} h_{FE2}	V_{CE}=5V,I_C=5A V_{CE}=5V,I_C=8A	8 6		40 30	
*Collector-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C=5A,I_B=1A I_C=8A,I_B=1.6A I_C=12A,I_B=3A			1 1.5 3	V V V
*Base-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C=5A,I_B=1A I_C=8A,I_B=1.6A			1.2 1.6	V V
Output Capacitance	C_{ob}	V_{CB}=10V, f=0.1MHz		180		pF
Current Gain Bandwidth Product	f_T	V_{CE}=10V,I_C=0.5A	4			MHz
Turn on Time	t_{on}	Vcc=125V, Ic=8A I_{B1}=1.6A, I_{B2}= -1.6A R_L=15.6Ω			1.1	µS
Storage Time	t_{stg}				3	µS
Fall Time	t_F				0.7	µS

* Pulse Test: Pulse Width≤300µs, Duty Cycle≤2%

Note : **h_{FE1} Classification** **R** :8 ~ 17, **O** : 15 ~ 28, **Y** : 26 ~ 39

Typical Characteristics

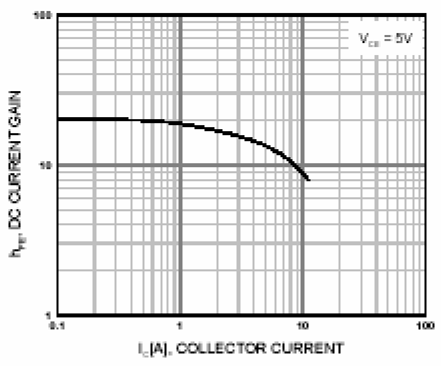


Figure 1. DC current Gain

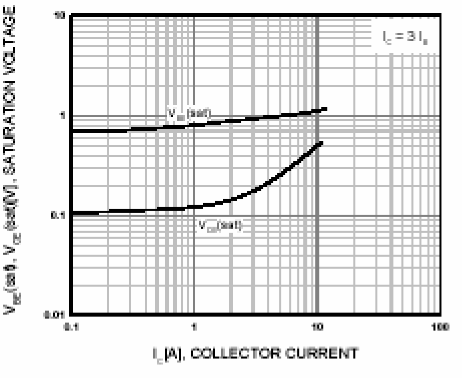


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

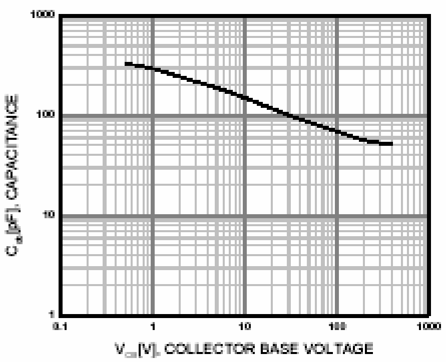


Figure 3. Collector Output Capacitance

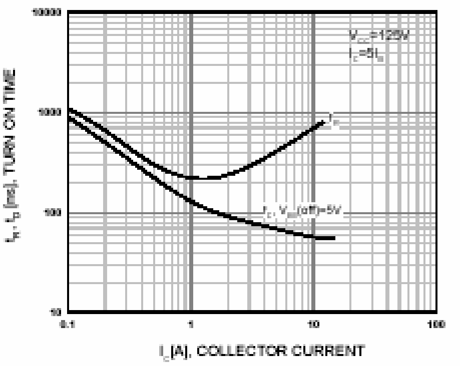


Figure 4. Turn On Time

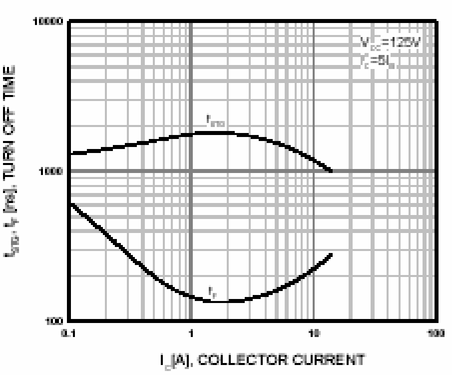


Figure 5. Turn Off Time

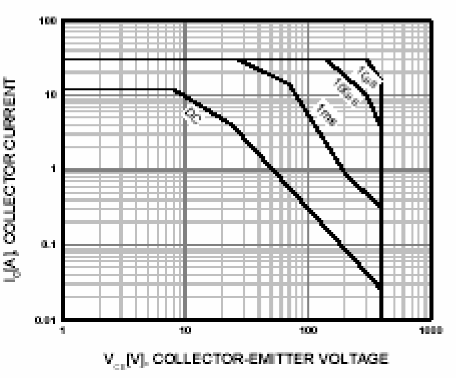


Figure 6. Forward Bias Safe Operating Area

Typical Characteristics (Continued)

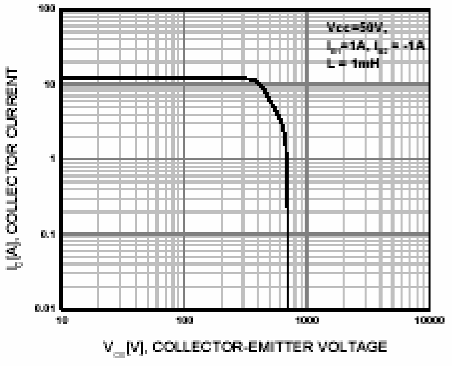


Figure 7. Reverse Bias Safe Operating Area

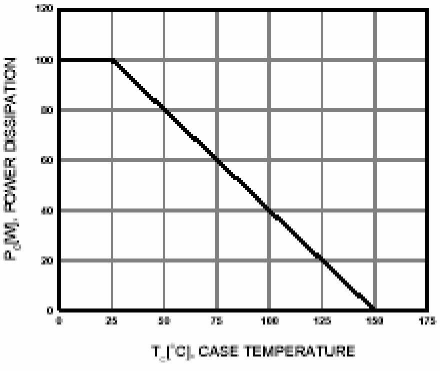
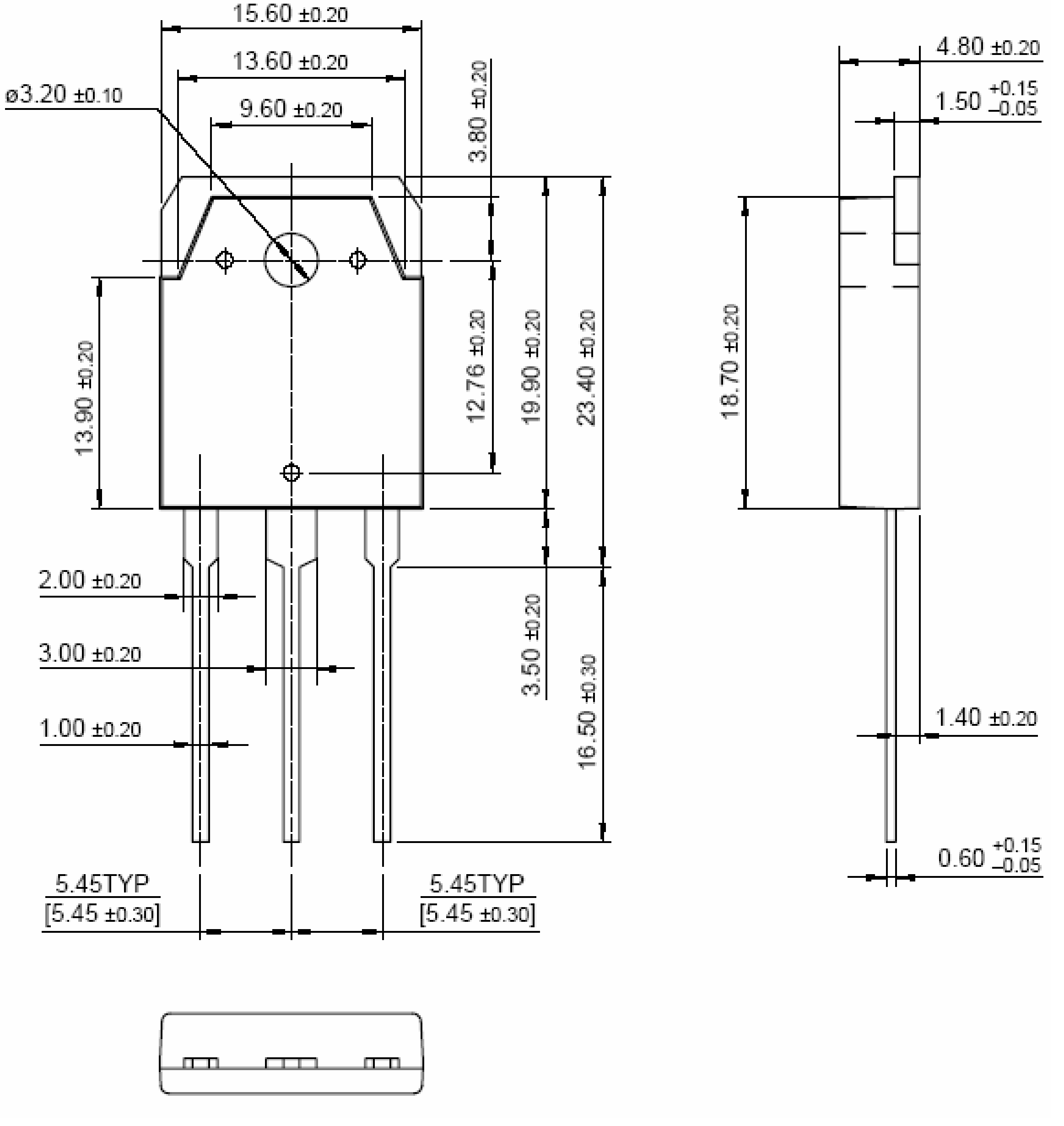


Figure 8. Power Derating

Package Dimensions

TO-3P



Dimensions in Millimeters

Reliability Qualification

A. High Temperature Reverse Bias (HTRB)

The purpose of this test is to determine the sensitivity of the product to mobile ion contamination and related failure mechanisms.

Conditions: JESD22-A108, JIS C 7021 B-8

T_A=150℃ V_{CB}=80% max rated V_{CB}

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

B. Pressure Cooker Test (PCT)

Autoclave (ACLV)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: JESD22-A102, JIS C 7021 A-6

T_A=121℃ RH=100% P=1 atmosphere (15psig)

Sample Size	#of Fail	Cum. Fail%	48hrs
45	0	0.0%	0

C. Temperature Humidity Bias (THBT)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components.
The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place.
with time, this is a catastrophically destructive test.

Conditions: JESD22-A101

T_A=85℃ RH=85% V_{CB}=80% max rated V_{CB}

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

Reliability Qualification (Continued)

D. High Temperature Storage Life (HTSL)

The purpose of this test is to expose time/temperature failure mechanisms and to evaluate long-term strong stability.

Conditions: JESD22-A103, JIS C 7021 B-10

$T_A = T_{stg}$(max)

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

E. Temperature Cycle Air-to Air (TMCL)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperature and the transition between temperature extreme, and to exposure excessive thermal mismatch between materials.

Conditions: JESD22-A104, JIS C 7021 A-4

Air to air, −65℃~150℃, 15 minutes dwell time at each temperature

Sample Size	#of Fail	Cum. Fail%	100cycles	200cycles
45	0	0.0%	0	0