

# KSH13007



# KSH13007

## Switch Mode series NPN silicon Power Transistor


- High voltage, high speed power switching
- Suitable for switching regulator, inverters motor controls

8 Amperes  
NPN Silicon Power Transistor  
80 Watts

### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

CHARACTERISTICS	SYMBOL	RATING	UNIT
Collector-Base Voltage	$V_{CBO}$	700	V
Collector-Emitter Voltage	$V_{CEO}$	400	V
Emitter-Base Voltage	$V_{EBO}$	9	V
Collector Current(DC)	$I_C$	8	A
Collector Current(Pulse)	$I_{CP}$	16	A
Base Current	$I_B$	4	A
Collector Dissipation( $T_C=25^\circ\text{C}$ )	$P_C$	80	W
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-65~150	$^\circ\text{C}$

TO-220  
1. Base  
2. Collector  
3. Emitter



### Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

CHARACTERISTICS	SYMBOL	Test Condition	Min	Typ.	Max	Unit
Collector-Emitter Breakdown Voltage	$V_{CEO}$	$I_C=10\text{mA}, I_B=0$	400			V
Emitter Cut-off Current	$I_{EBO}$	$V_{EB}=9\text{V}, I_C=0$			1	mA
*DC Current Gain	$h_{FE1}$ $h_{FE2}$	$V_{CE}=5\text{V}, I_C=2\text{A}$ $V_{CE}=5\text{V}, I_C=5\text{A}$	8 5		60 30	
*Collector-Emitter Saturation Voltage	$V_{CE}(\text{sat})$	$I_C=2\text{A}, I_B=0.4\text{A}$ $I_C=5\text{A}, I_B=1\text{A}$ $I_C=8\text{A}, I_B=2\text{A}$			1 2 3	V V V
*Base-Emitter Saturation Voltage	$V_{BE}(\text{sat})$	$I_C=2\text{A}, I_B=0.4\text{A}$ $I_C=5\text{A}, I_B=1\text{A}$			1.2 1.6	V V
Output Capacitance	$C_{ob}$	$V_{CB}=10\text{V}, f=0.1\text{MHz}$		110		pF
Current Gain Bandwidth Product	$f_T$	$V_{CE}=10\text{V}, I_C=0.5\text{A}$	4			MHz
Turn on Time	$t_{on}$	$V_{CC}=125\text{V}, I_C=5\text{A}$ $I_{B1}=1\text{A}, I_{B2}=-1\text{A}$ $R_L=50\Omega$			1.6	$\mu\text{S}$
Storage Time	$t_{sig}$				3.0	$\mu\text{S}$
Fall Time	$t_F$				0.7	$\mu\text{S}$

\* Pulse Test: Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 2\%$

Note :  $h_{FE1}$  Classification R : 15 ~ 28, O : 26 ~ 39, Y : 37 ~ 50

## Typical Characteristics

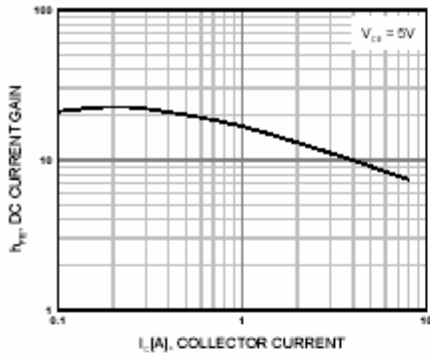


Figure 1. DC current Gain

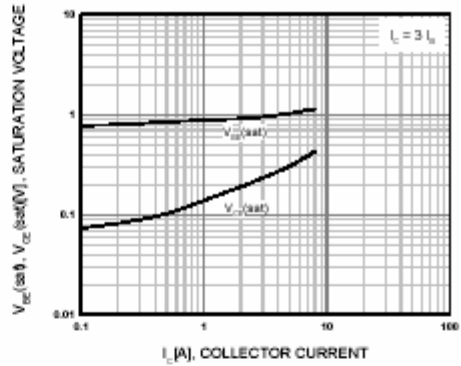


Figure 2. Base-Emitter Saturation Voltage  
Collector-Emitter Saturation Voltage

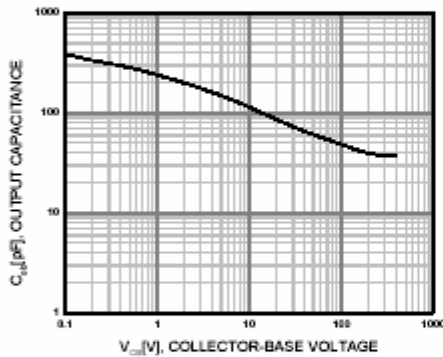


Figure 3. Collector Output Capacitance

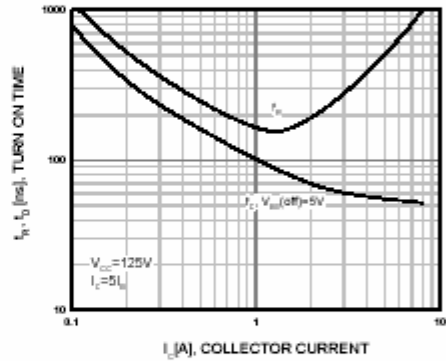


Figure 4. Turn On Time

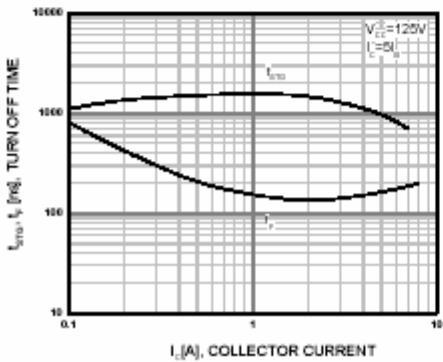


Figure 5. Turn Off Time

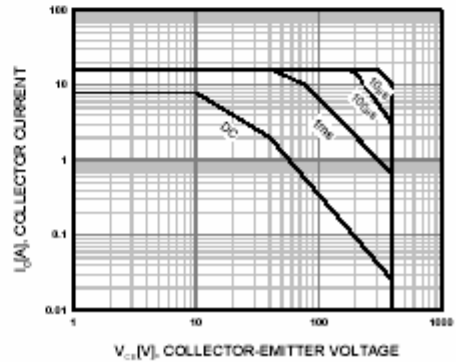
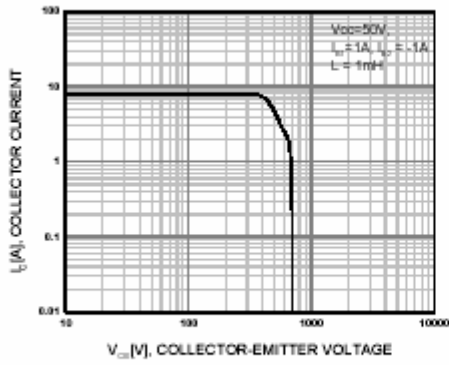
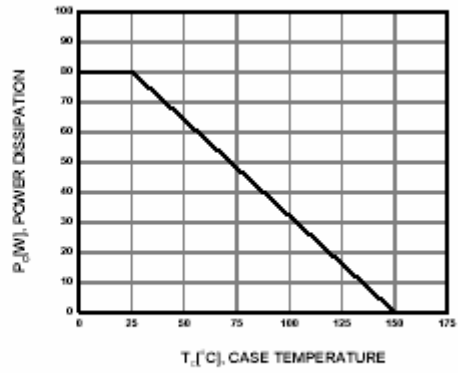


Figure 6. Forward Bias Safe Operating Area

**Typical Characteristics (Continued)**



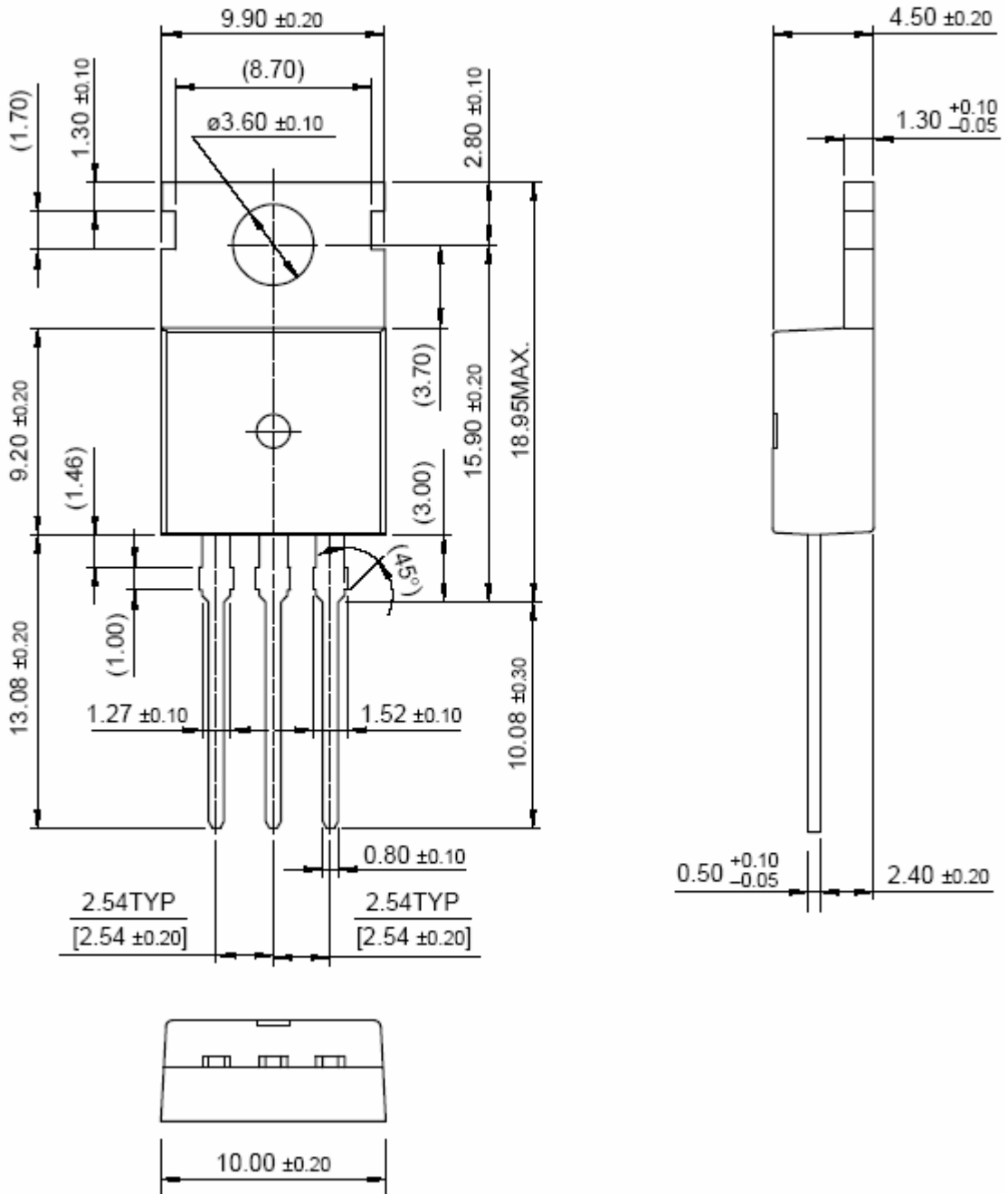
**Figure 7. Reverse Bias Safe Operating Area**



**Figure 8. Power Derating**

### Package Dimensions

## TO-220



Dimensions in Millimeters

## Reliability Qualification

### A. High Temperature Reverse Bias ( HTRB )

The purpose of this test is to determine the sensitivity of the product to mobile ion contamination and related failure mechanisms.

Conditions: JESD22-A108, JIS C 7021 B-8

$T_A=150^{\circ}\text{C}$   $V_{CB}=80\%$  max rated  $V_{CB}$

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

### B. Pressure Cooker Test ( PCT )

#### Autoclave ( ACLV )

The purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: JESD22-A102, JIS C 7021 A-6

$T_A=121^{\circ}\text{C}$  RH=100% P=1 atmosphere (15psig)

Sample Size	#of Fail	Cum. Fail%	48hrs
45	0	0.0%	0

### C. Temperature Humidity Bias ( THBT )

The purpose of this test is to evaluate the moisture resistance of non-hermetic components.

The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place. with time, this is a catastrophically destructive test.

Conditions: JESD22-A101

$T_A=85^{\circ}\text{C}$  RH=85%  $V_{CB}=80\%$  max rated  $V_{CB}$

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

**Reliability Qualification (Continued)****D. High Temperature Storage Life ( HTSL )**

The purpose of this test is to expose time/temperature failure mechanisms and to evaluate long-term strong stability.

Conditions: JESD22-A103, JIS C 7021 B-10

$T_A = T_{stg}(\max)$

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

**E. Temperature Cycle Air-to Air ( TMCL )**

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperature and the transition between temperature extreme, and to exposure excessive thermal mismatch between materials.

Conditions: JESD22-A104, JIS C 7021 A-4

Air to air,  $-65^{\circ}\text{C} \sim 150^{\circ}\text{C}$ , 15 minutes dwell time at each temperature

Sample Size	#of Fail	Cum. Fail%	100cycles	200cycles
45	0	0.0%	0	0