

# Quad Bus Receiver

The MC10129 data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

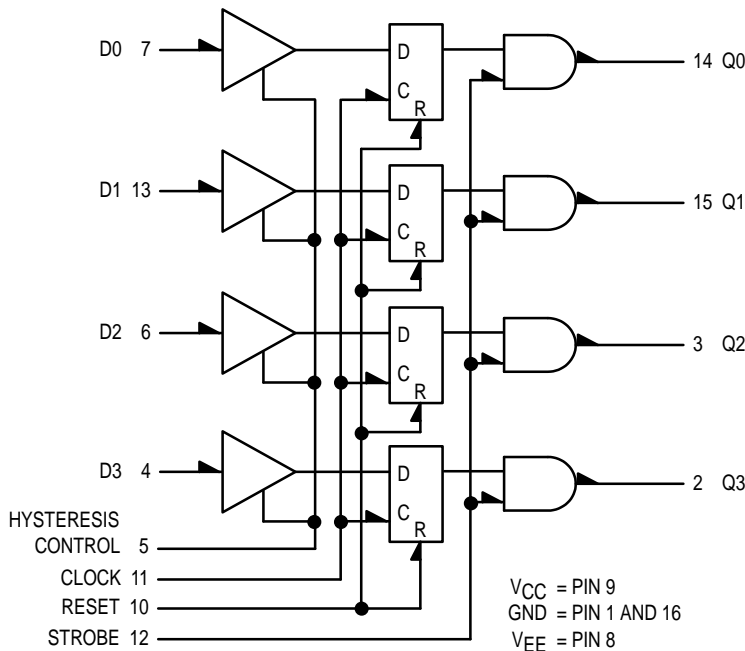
The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, and the reset input is disabled, the outputs will follow the D inputs. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V<sub>CC</sub> or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V<sub>EE</sub>. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V<sub>EE</sub>. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

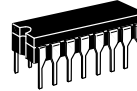
The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.

$P_D = 750 \text{ mW typ/pkg (No Load)}$   
 $t_{pd} = 10 \text{ ns typ}$   
 $V_{CC} \text{ Max} = 7.0 \text{ Vdc}$

**LOGIC DIAGRAM**

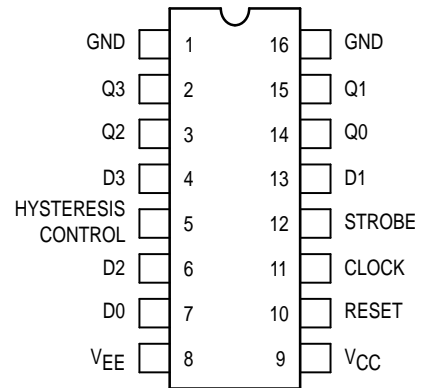


# MC10129



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

**PIN ASSIGNMENT**



**TRUTH TABLE**

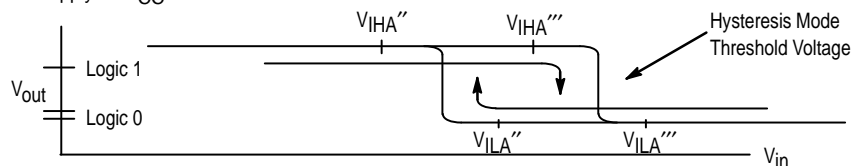
D	C	STROBE	RESET	Q <sub>n+1</sub>
X	X	L	X	L
X	H	X	H	L
L	L	H	X	L
X	H	H	L	Q <sub>n</sub>
H	L	H	X	H



**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C		+85°C			
			Min	Max	Min	Typ	Max	Min		Max
Negative Power Supply Drain Current	$I_E$	8 8		167 189			152 172		167 189	mAdc
Positive Power Supply Drain Current	$I_{CC}$	9		8.0			8.0		8.0	mAdc
Input Current	$I_{inH}$	4		150			95		95	$\mu$ Adc
		6		150			95		95	
		7		150			95		95	
		10		720			450		450	
		11		390			245		245	
		12		390			245		245	
		13		150			95		95	
	$I_{CBO} (1.)$	4		1.5			-1.0		1.0	$\mu$ Adc
		6		1.5			-1.0		1.0	
		7		1.5		-1.0			1.0	
		13								
	$I_{inL}$	10	0.5		0.5			0.3		$\mu$ Adc
		11	0.5		0.5			0.3		
		12	0.5		0.5			0.3		
Output Voltage Logic 1	$V_{OH}$	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	$V_{OL}$	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	$V_{OHA}$	2 (2.)	-1.080		-0.980			-0.910		Vdc
		2	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
		2 (3.)	-1.080		-0.980			-0.910		
		2 (4.)	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	$V_{OLA}$	2 (2.)		-1.655			-1.630		-1.595	Vdc
		2		-1.655			-1.630		-1.595	
		2 (2.)		-1.655			-1.630		-1.595	
		2		-1.655			-1.630		-1.595	
		2 (3.)		-1.655			-1.630		-1.595	
		2 (4.)		-1.655			-1.630		-1.595	
Switching Times Propagation Delay									ns	
Data Input	$t_{7+14+}$	14	3.7	15	3.7	10	15	3.7	30	
	$t_{7-14-}$	14	3.7	15	3.7	10	15	3.7	40	
Clock Input	$t_{11-14+}$	14	2.7	11	2.7	5.0	9.0	2.7	11	
	$t_{11-14-}$	14	2.7	11	2.7	5.0	9.0	2.7	11	
Strobe Input	$t_{12+14+}$	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0	
	$t_{12-14-}$	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0	
Reset Input	$t_{10+14-}$	14	2.0	8.0	2.0	5.0	6.5	2.0	8.0	
Hysteresis Mode	$t_{7+14+}$	14	6.6	30	6.7	18	25	6.6	30	
	$t_{7-14-}$	14	3.7	17	3.7	10	15	3.7	40	
Setup Time	$t_{setup}$	14	30		2.7	15		30		
Hold Time	$t_{hold}$	14	0		-2.0	15		-2.0		
Rise Time	$t_+$	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	
Fall Time	$t_-$	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	

1. Pin 5 to  $V_{EE}$ ,  $V_{IL}$  to Data input one at a time.
2. Output latched to logic high state prior to test.  $V_{IHA}'$ ,  $V_{ILA}'$  are standard logic 1 and logic 0 MTTL threshold voltages.  $V_{IHA}''$ ,  $V_{ILA}''$ ,  $V_{IHA}'''$  and  $V_{ILA}'''$  are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3-2.
3. Input level on data input taken from +0.4V up to voltage level given.
4. Input level on data input taken from +4.0V down to voltage level given.
5. Operation and limits shown also apply for  $V_{CC} = +6.0V$ .



**Figure 1. Hysteresis Mode Threshold Voltage**

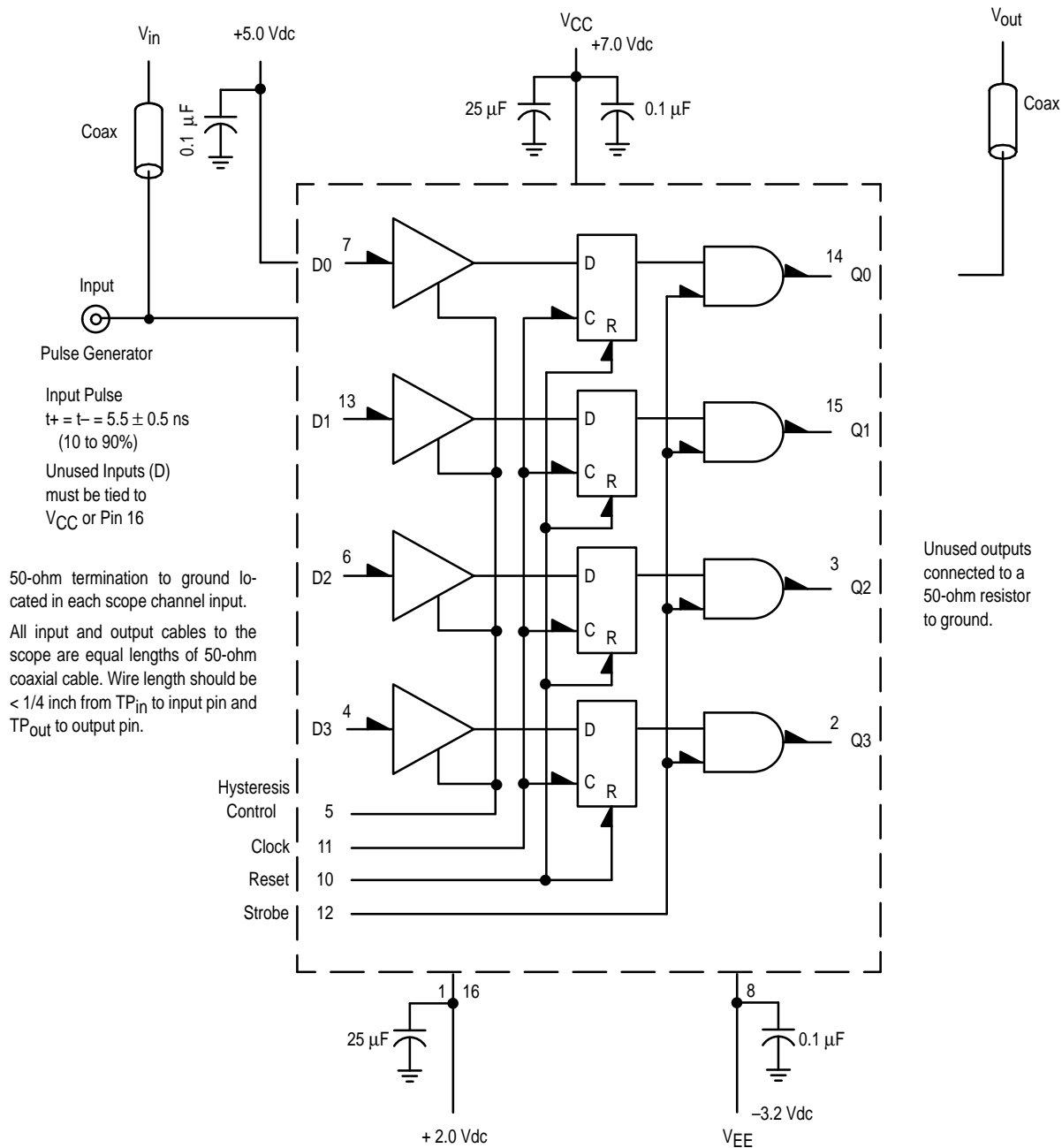
## ELECTRICAL CHARACTERISTICS

@ Test Temperature -30°C +25°C +85°C			TEST VOLTAGE VALUES (Volts)								Gnd												
			MECL 10,000 INPUT LEVELS				TTL INPUT LEVELS (6.)																
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA'</sub>	V <sub>ILA'</sub>													
			-0.890	-1.890	-1.155	-1.500	3.000	0.400	2.000	0.800													
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW																				
Characteristic	Symbol	Pin Under Test	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA'</sub>	V <sub>ILA'</sub>	Gnd												
Negative Power Supply Drain Current	I <sub>E</sub>	8 8	11 11	12 12							1,5,16 1,16												
Positive Power Supply Drain Current	I <sub>CC</sub>	9						4,6,7,13			1,16												
Input Current	I <sub>inH</sub>	4 6 7 10 11 12 13	10,11 11 12				4 6 7 13				1,16 1,16 1,16 1,16 1,16 1,16 1,16												
		I <sub>CBO</sub> (1.)		4 6 7 13				4 6 7 13			1,16 1,16 1,16 1,16												
		I <sub>inL</sub>		10 11 12	10 11 12						1,16 1,16 1,16												
Output Voltage Logic 1	V <sub>OH</sub>	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11			4 6 4 6				1,16 1,16 1,5,16 1,5,16												
		Output Voltage Logic 0	V <sub>OL</sub>	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11			4 6 4 6			1,16 1,16 1,5,16 1,5,16											
				Threshold Voltage Logic 1	V <sub>OHA</sub>	2 (2.) 2 2 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12 12	10,11 10,11 10,11 10,11 10,11 10,11	12 11	10 4 4		4		1,16 1,16 1,16 1,16 1,5,16 1,5,16									
						Threshold Voltage Logic 0	V <sub>OLA</sub>	2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12 12	10,11 10,11 10,11 10,11 10,11 10,11	10 11	4 4 4			4	1,16 1,16 1,16 1,16 1,5,16 1,5,16							
Switching Times Propagation Delay																							
		Data Input	t <sub>7+14+</sub> t <sub>7-14-</sub>														14 14	12 12	10,11 10,11	7 7	14 14		
		Clock Input	t <sub>11-14+</sub> t <sub>11-14-</sub>	14 14	12 12												10 10	7,11 7,11	14 14				Figure 6 Figure 6
			Strobe Input	t <sub>12+14+</sub> t <sub>12-14-</sub>	14 14		10,11 10,11										12 12	14 14	7 7			Figure 4 Figure 4	1,16 1,16
		Reset Input		t <sub>10+14-</sub>	14	12											10,11	14	7	7		Figure 5	1,16
		Hysteresis Mode	t <sub>7+14+</sub> t <sub>7-14-</sub>	14 14	12 12	10,11 10,11	7 7										14 14				Figure 3 Figure 3	1,5,16 1,5,16	
			Setup Time	t <sub>setup</sub>	14	12	10										7,11	14			Figure 7	1,16	
		Hold Time	t <sub>hold</sub>	14	12	10	7,11										14			Figure 7	1,16		
		Rise Time	t <sub>+</sub>	14	12	10,11	7										14			Figure 3	1,16		
		Fall Time	t <sub>-</sub>	14	12	10,11	7										14			Figure 3	1,16		

- Pin 5 to V<sub>EE</sub>, V<sub>IL</sub> to Data input one at a time.
- Output latched to logic high state prior to test. V<sub>IHA'</sub>, V<sub>ILA'</sub> are standard logic 1 and logic 0 M TTL threshold voltages. V<sub>IHA''</sub>, V<sub>ILA''</sub>, V<sub>IHA'''</sub> and V<sub>ILA'''</sub> are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3-2.
- Input level on data input taken from +0.4V up to voltage level given.
- Input level on data input taken from +4.0V down to voltage level given.
- Operation and limits shown also apply for V<sub>CC</sub> = +6.0V.
- When testing, choose either TTL or IBM input levels.

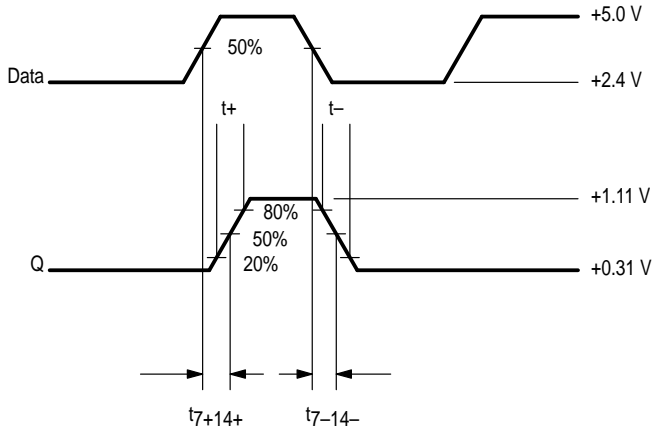


Figure 2. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

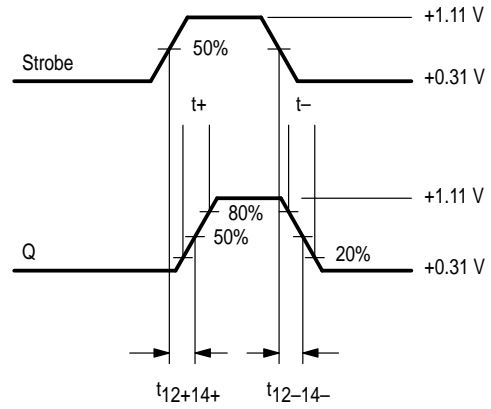


NOTE: All power supplies and logic levels are shifted 2 volts positive.

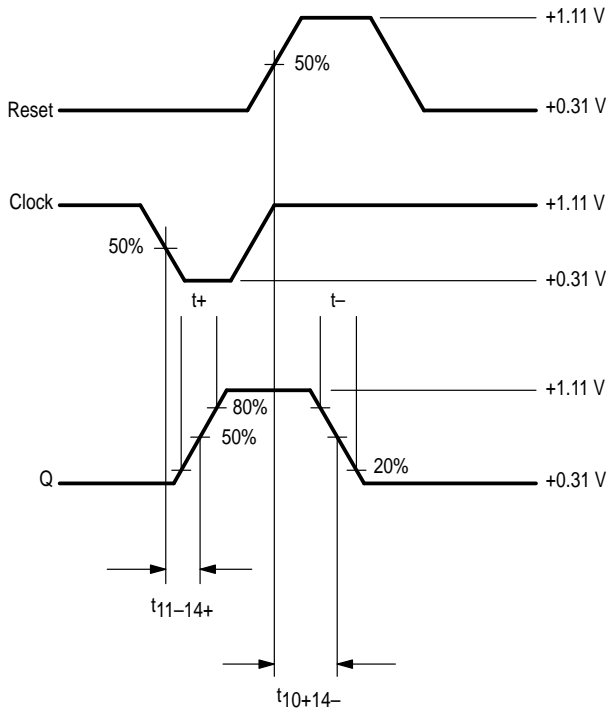
**Figure 3 – DATA to OUTPUT**  
(Clock and Reset are low, Strobe is high)



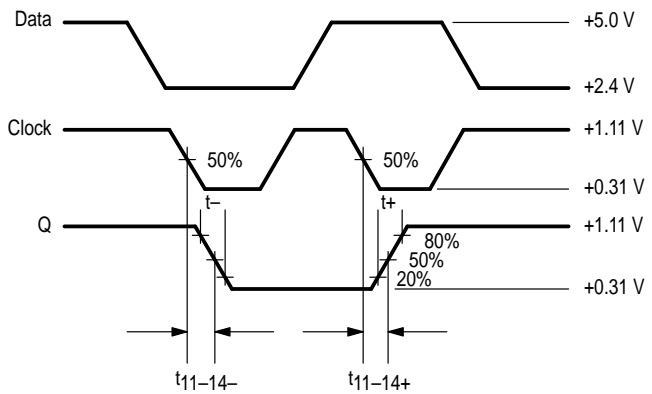
**Figure 4 – STROBE to OUTPUT**  
(Data is high, Clock and Reset are low)



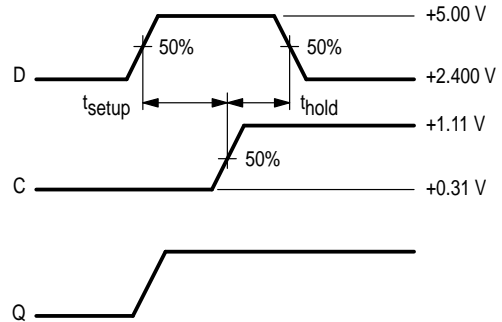
**Figure 5 – RESET to OUTPUT**  
(Data and Strobe are high)



**Figure 6 – CLOCK to OUTPUT**  
(Reset is low, Strobe is high)

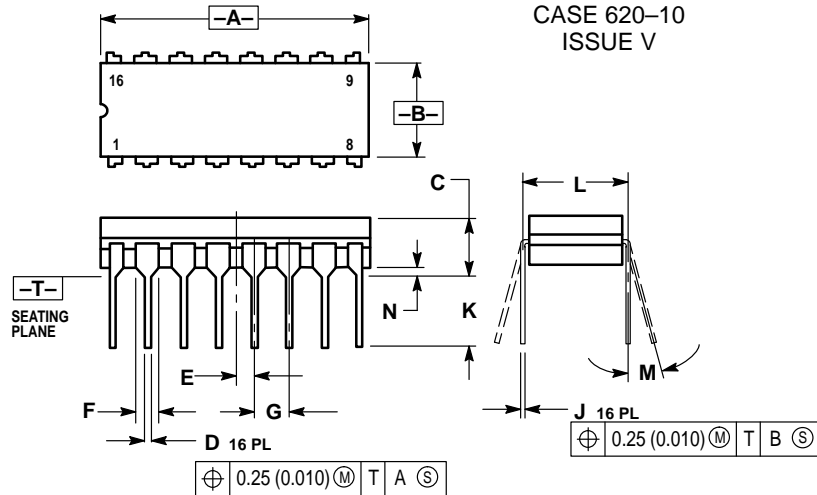


**Figure 7 – TSET UP AND THOLD WAVEFORMS**



OUTLINE DIMENSIONS

L SUFFIX  
CERAMIC DIP PACKAGE  
CASE 620-10  
ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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