MC100EP139

Product Preview

÷2/4, ÷4/5/6 Clock Generation Chip

The MC100EP139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single–ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device. If a single–ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip–flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip–flops will attain a random state; therefore, for systems which utilize multiple EP139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP139, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/5/6 outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

- 50ps Output–to–Output Skew
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >2KV HBM, >100V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 758 devices

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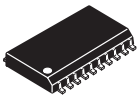
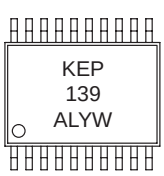
TSSOP–20
DT SUFFIX
CASE 948E



SO–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EP139DT	TSSOP	75 Units/Rail
MC100EP139DTR2	TSSOP	2500 Tape/Reel
MC100EP139DW	SOIC	38 Units/Rail
MC100EP139DWR2	SOIC	2500 Tape/Reel

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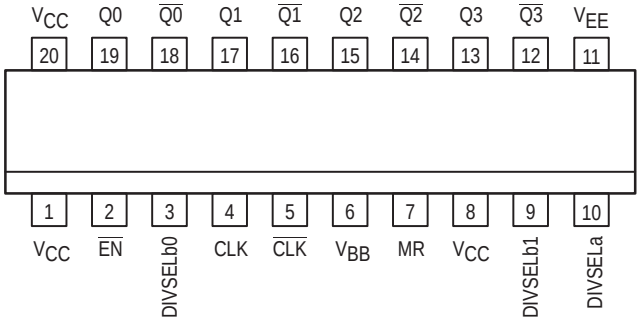


Figure 1. 20–Lead SOIC (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLES

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low–to–High Transition
ZZ = High–to–Low Transition

DIVSELa	Q0:1 OUTPUTS
0	Divide by 2
1	Divide by 4

DIVSELb0	DIVSELb1	Q2:3 OUTPUTS
0	0	Divide by 4
1	0	Divide by 6
0	1	Divide by 5
1	1	Divide by 5

PIN DESCRIPTION	
PIN	**FUNCTION**
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	ECL Diff ÷2/4 Outputs
Q2, Q3, $\overline{Q2}$, $\overline{Q3}$	ECL Diff ÷4/5/6 Outputs
DIVSELa	ECL Freq. Select Input ÷2/4
DIVSELb0	ECL Freq. Select Input ÷4/5/6
DIVSELb1	ECL Freq. Select Input ÷4/5/6
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative, 0 Supply

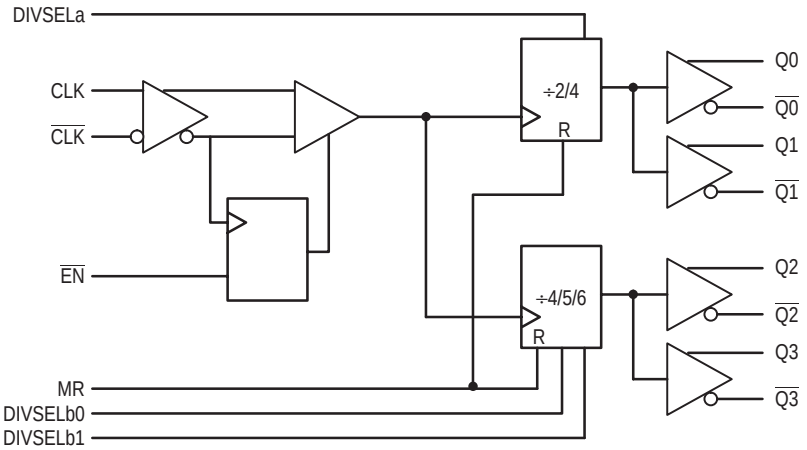


Figure 2. Logic Diagram

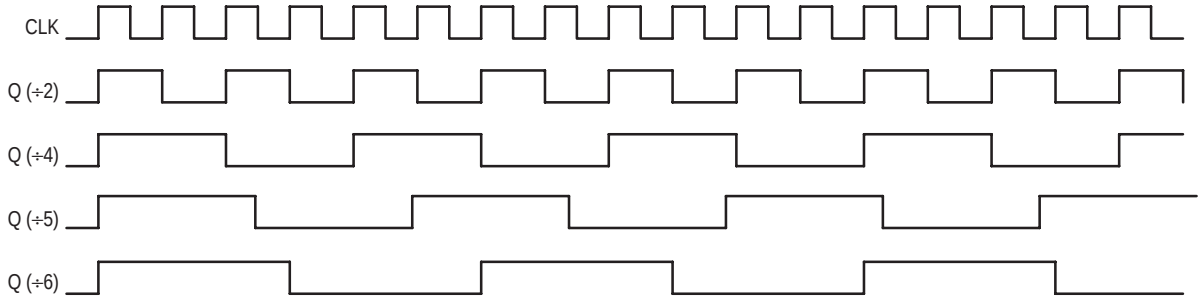


Figure 3. Timing Diagram

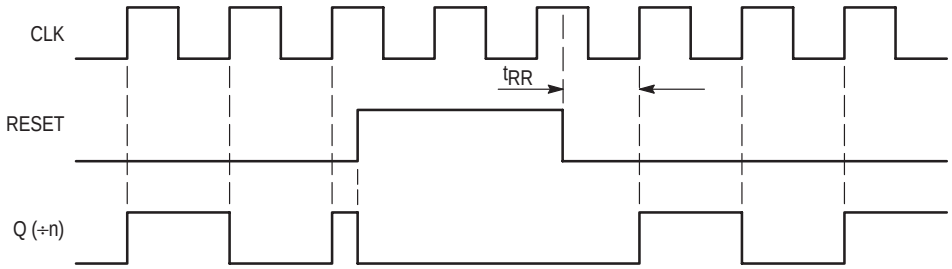


Figure 4. Timing Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA} (DT Suffix)	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	140 100	°C/W
θ_{JC} (DT Suffix)	Thermal Resistance (Junction–to–Case)	23 to 41 ± 5%	°C/W
θ_{JA} (DW Suffix)	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	90 60	°C/W
θ_{JC} (DW Suffix)	Thermal Resistance (Junction–to–Case)	33 to 35 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –5.5V to –3.0V) (Note 3.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1250	–1100	–895	–1250	–1100	–895	–1250	–1100	–895	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1995	–1850	–1650	–1995	–1850	–1650	–1995	–1850	–1650	mV
V_{IH}	Input HIGH Voltage Single Ended		–1022			–1022			–1022		mV
V_{IL}	Input LOW Voltage Single Ended		–1642			–1642			–1642		mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC} –2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	70	83	100	70	87	105	75	90	110	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2050	2200	2405	2050	2200	2405	2050	2200	2405	mV
V_{OL}	Output LOW Voltage (Note 5.)	1305	1450	1650	1305	1450	1650	1305	1450	1650	mV
V_{IH}	Input HIGH Voltage Single Ended		2277			2277			2277		mV
V_{IL}	Input LOW Voltage Single Ended		1657			1657			1657		mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.0V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC} –2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	70	85	100	70	90	105	75	95	110	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3750	3900	4105	3750	3900	4105	3750	3900	4105	mV
V_{OL}	Output LOW Voltage (Note 8.)	3005	3150	3350	3005	3150	3350	3005	3150	3350	mV
V_{IH}	Input HIGH Voltage Single Ended		3977			3977			3977		mV
V_{IL}	Input LOW Voltage Single Ended		3357			3357			3357		mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC} –2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

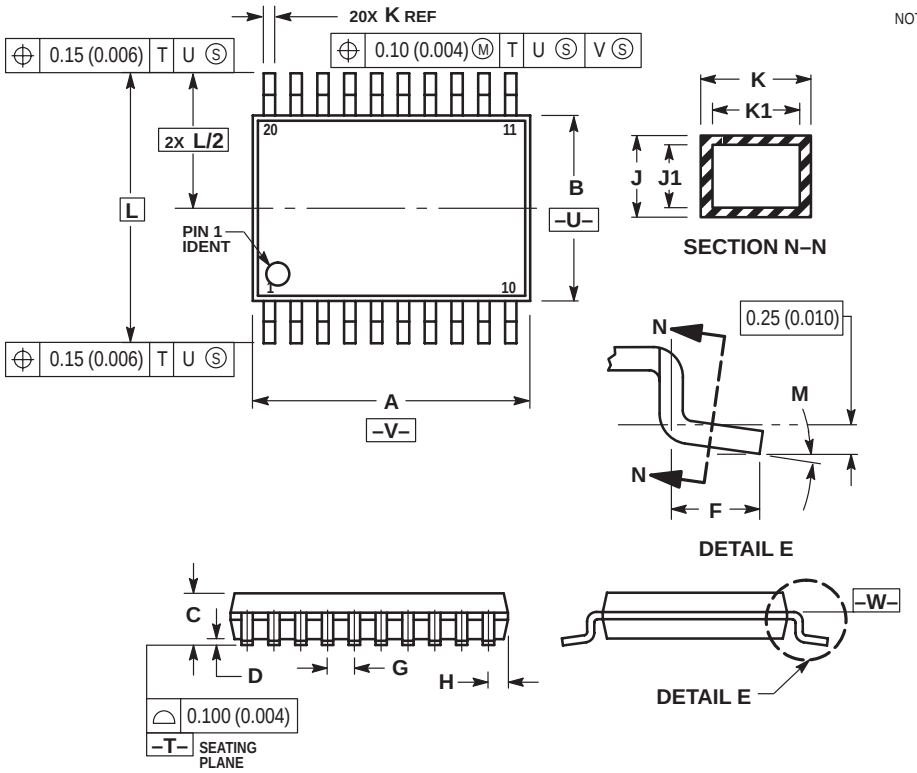
AC CHARACTERISTICS (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V) or (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 10.)	1.0	1.2		1.0	1.2		1.0	1.2		GHz
t_{PLH}, t_{PHL}	Propagation Delay CLK, Q(DIFF) CLK, Q(SE) MR, Q	550	700	800	600	750	900	675	825	975	ps
t_{SKEW}	Device Skew Q, $\overline{Q}$ Part–to–Part (Note 11.)					50 200					ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise and Fall Times Q, $\overline{Q}$ (20% – 80%)	110	180	250	125	190	275	150	215	300	ps
t_s	Setup Time $\overline{EN}$, $\overline{CLK}$ DIVSEL, CLK	200 400	120		200 400	120		200 400	120		ps
t_h	Hold Time $\overline{CLK}$, $\overline{EN}$ CLK, DIVSEL	100 150	50		100 150	50		100 150	50		ps
V_{pp}	Input Voltage Swing (Diff)	300	800	1200	300	800	1200	300	800	1200	mV
t_{rr}	Reset Recovery Time					100					ps
t_{pw}	Minimum Pulse Width CLK MR	550	450		550	450		550	450		ps

10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions.

PACKAGE DIMENSIONS

TSSOP–20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A

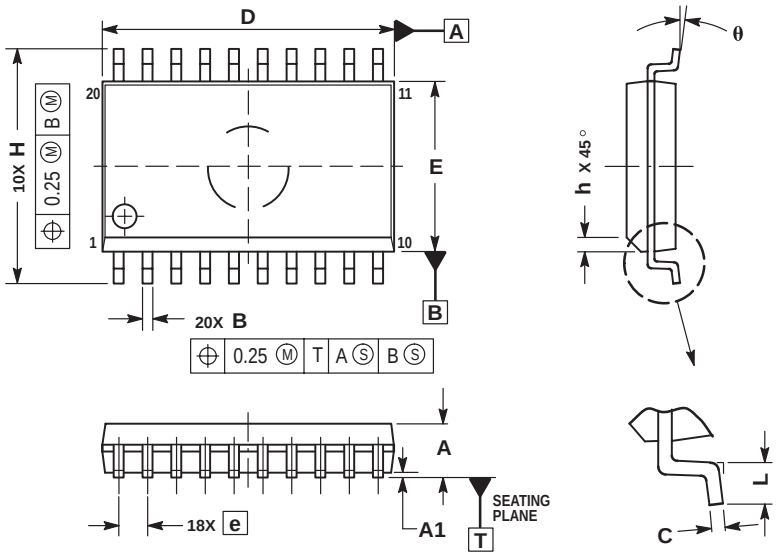


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SO–20
DW SUFFIX
20 PIN PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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