Dual Differential Data and Clock D Flip-Flop With Set and Reset

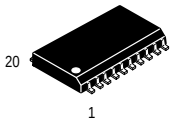
MC100LVEL29
MC100EL29

The MC100LVEL29 is a dual master–slave flip flop. The device features fully differential Data and Clock inputs as well as outputs. The MC100EL29 is pin and functionally equivalent to the MC100LVEL29 but is specified for operation at the standard 100E ECL voltage supply. A V_{BB} output is provided for AC coupling, refer to the interfacing section of the ECLinPS Data Book (DL140) for more information on AC coupling ECL signals. Data enters the master latch when the clock is LOW and transfers to the slave upon a positive transition on the clock input.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE} and the $\overline{D}$ input will bias around $V_{CC}/2$. The outputs will go to a defined state, however the state will be random based on how the flip flop powers up.

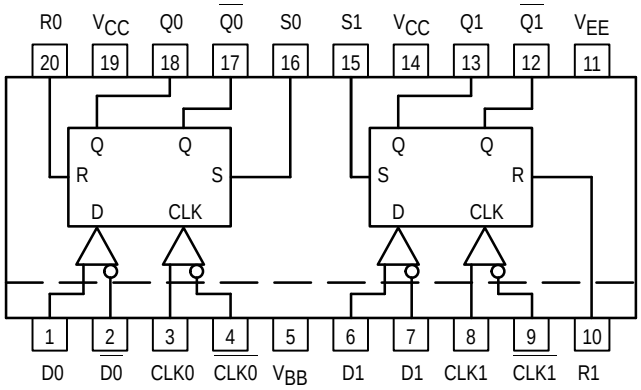
Both flip flops feature asynchronous, overriding Set and Reset inputs. Note that the Set and Reset inputs cannot both be HIGH simultaneously.

- 1100MHz Flip–Flop Toggle Frequency
- 20–lead SOIC Package
- 580ps Propagation Delays



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition

PIN NAMES

Pins	Function
D0–D1	Data Inputs
R0–R1	Reset Inputs
CLK0–CLK1	Clock Inputs
S0–S1	Set Inputs

MC100LVEL29
DC CHARACTERISTICS (V_{EE} = –3.0V to –3.8V; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35	50		35	50		35	50		35	50	mA
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current $\overline{Dn}$ Inputs Dn Inputs	0.5 –300			0.5 –300			0.5 –300			0.5 –300			µA

MC100LVEL29
AC CHARACTERISTICS (V_{EE} = –3.0V to –3.8V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency	1.1			1.1			1.1			1.1			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	480 480		680 700	490 490		690 710	500 500		700 720	520 520		720 740	ps
t_S t_H	Setup Time Hold Time	0 100			0 100			0 100			0 100			ps
t_{RR}	Set/Reset Recovery	100			100			100			100			ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			400			ps
V_{PP}	Minimum Input Swing	150			150			150			150			mV
V_{CMR}[1]	Common V_{PP}<500mV Mode Range V_{PP}≥500mV	–2.0 –1.8		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	280		550	ps

1. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

MC100EL29
DC CHARACTERISTICS (V_{EE} = –4.2V to –5.5V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		35	50		35	50		35	50		35	50	mA
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current D̄n Inputs Dn Inputs	0.5 –300			0.5 –300			0.5 –300			0.5 –300			µA

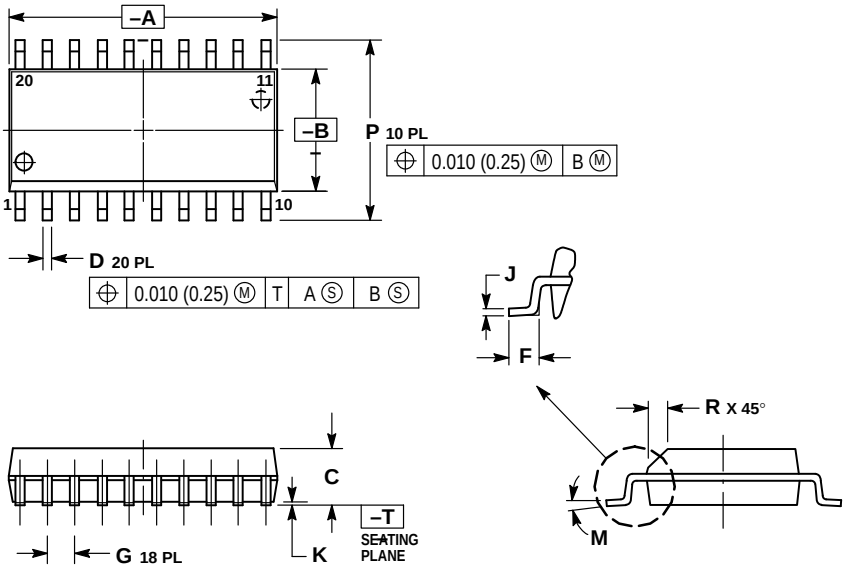
MC100EL29
AC CHARACTERISTICS (V_{EE} = –4.2V to –5.5V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency	1.1			1.1			1.1			1.1			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	480 480		680 700	490 490		690 710	500 500		700 720	520 520		720 740	ps
t_S t_H	Setup Time Hold Time	0 100			0 100			0 100			0 100			ps
t_{RR}	Set/Reset Recovery	100			100			100			100			ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			400			ps
V_{PP}	Minimum Input Swing	150			150			150			150			mV
V_{CMR}[1]	Common V_{PP}<500mV Mode Range V_{PP}≥500mV	–3.2 –3.0		–0.4 –0.4	–3.3 –3.1		–0.4 –0.4	–3.3 –3.1		–0.4 –0.4	–3.3 –3.1		–0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	280		550	ps

1. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –4.5V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0V – |V_{CMR}(min)|.

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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