

Silicon PNP Power Transistors

2SB1272

DESCRIPTION

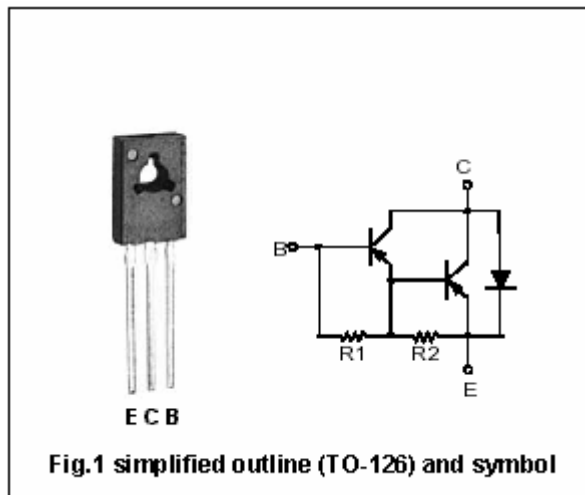
- With TO-126 package
- DARLINGTON
- High DC current gain

APPLICATIONS

- For low frequency power amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute maximum ratings (Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CB0}	Collector-base voltage	Open emitter	-100	V
V _{CEO}	Collector-emitter voltage	Open base	-100	V
V _{EBO}	Emitter -base voltage	Open collector	-7	V
I _C	Collector current		-2	A
P _C	Collector power dissipation	T _C =25°C	10	W
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA; I _B =0	-100			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA; I _E =0	-100			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-5mA; I _C =0	-7			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-2A; I _B =-2mA			-2.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-2A; I _B =-2mA			-2.5	V
I _{CBO}	Collector cut-off current	V _{CB} =100V; I _E =0			-0.1	mA
I _{CEO}	Collector cut-off current	V _{CE} =100V; I _B =0			-0.5	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-7V; I _C =0			-5.0	mA
h _{FE}	DC current gain	I _C =-1A ; V _{CE} =-2V	1000		10000	

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PACKAGE OUTLINE

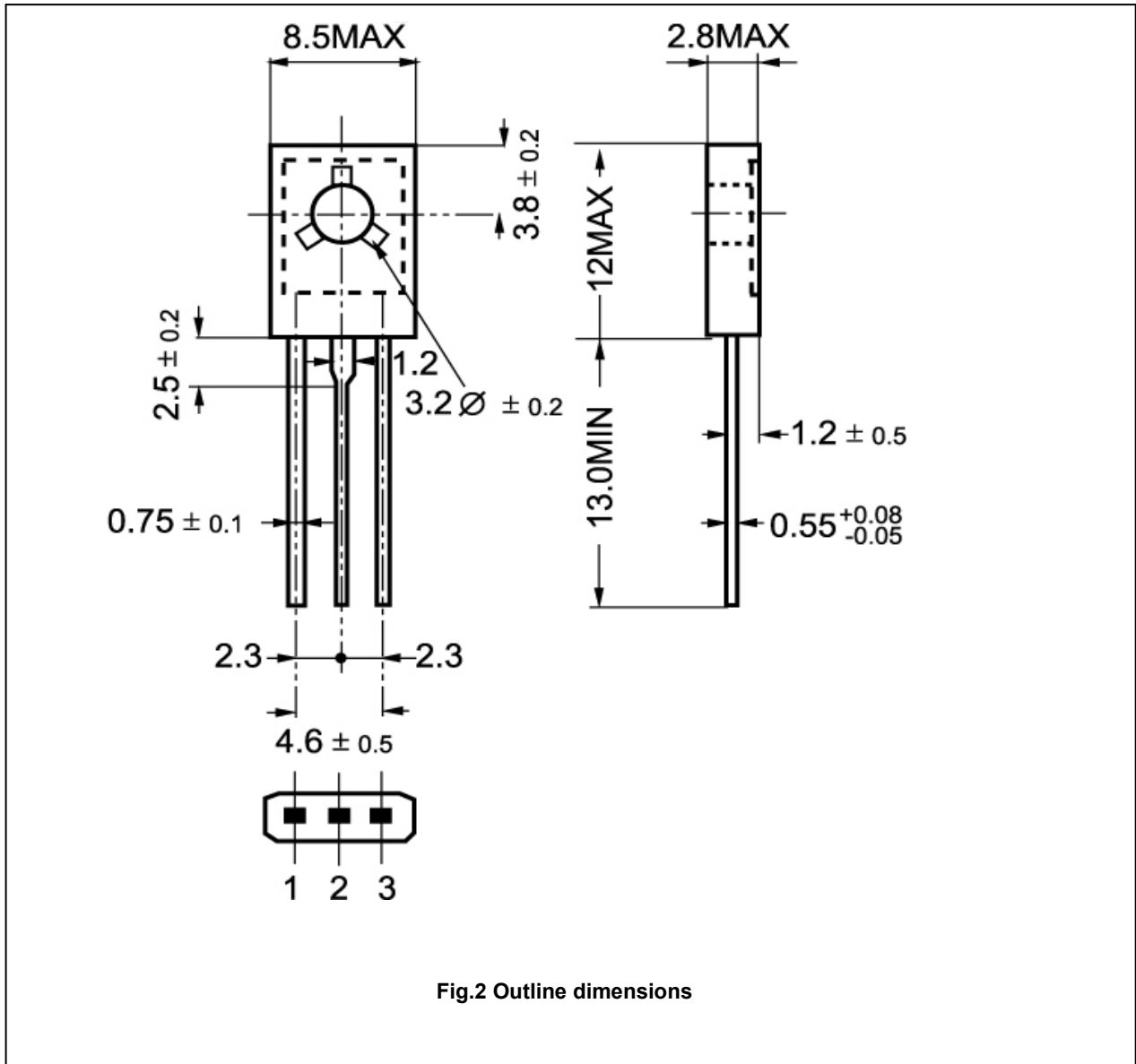


Fig.2 Outline dimensions