MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

PNP 2N6053 2N6054 2N6298 2N6299 · NPN 2N6055 2N6056 2N6300 2N6301

PNP	NPN
2N6053	2N6055
2N6054	2N6056
2N6298	2N6300
2N6299	2N6301

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain — h_{FE} = 3000 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6053, 2N6055, 2N6298, 2N6300
  = 80 Vdc (Min) — 2N6054, 2N6056, 2N6299, 2N6301
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80 VOLTS
75,100 WATTS

*MAXIMUM RATINGS

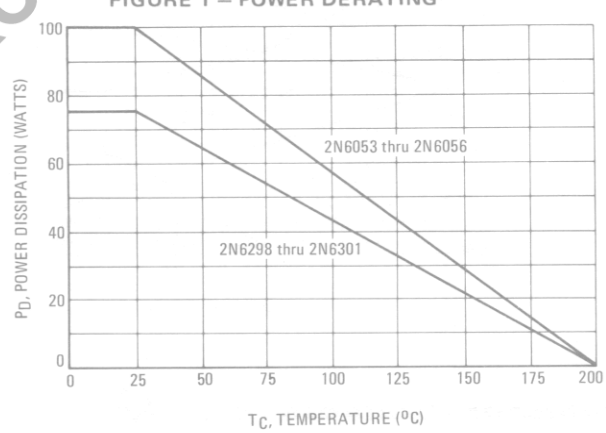
Rating	Symbol	2N6053 2N6055 2N6298 2N6300	2N6054 2N6056 2N6299 2N6301	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous / Peak	I_C	8.0 / 16		Adc
Base Current	I_B	120		mAdc
		2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	
Total Device Dissipation @ T_C = 25°C / Derate above 25°C	P_D	100 / 0.571	75 / 0.428	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

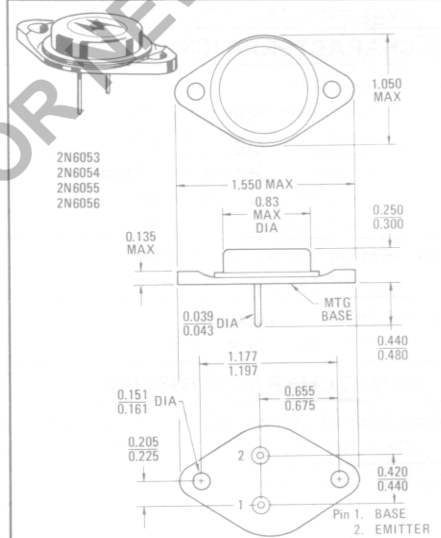
THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.75	2.33	°C/W

*Indicates JEDEC Registered Data.

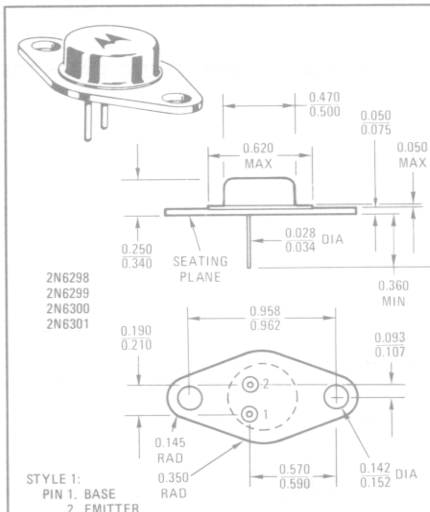
FIGURE 1 — POWER DERATING





All JEDEC dimensions and notes apply
Collector connected to case

CASE 11
TO-3



All JEDEC dimensions and notes apply
Collector connected to case

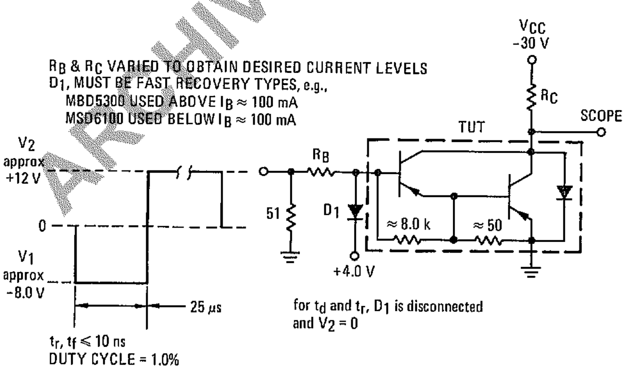
CASE 80-02
TO-66

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0) 2N6053, 2N6055, 2N6298, 2N6300	$V_{CEO(sus)}$	60	–	Vdc
2N6054, 2N6056, 2N6299, 2N6301		80	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) 2N6053, 2N6055, 2N6298, 2N6300	I_{CEO}	–	0.5	mAdc
(V_{CE} = 40 Vdc, I_B = 0) 2N6054, 2N6056, 2N6299, 2N6301		–	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	0.5	mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	750	18000	–
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)		100	–	
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc)	$V_{CE(sat)}$	–	2.0	Vdc
(I_C = 8.0 Adc, I_B = 80 mAdc)		–	3.0	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small-Signal Short Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N6053, 2N6054, 2N6298, 2N6299	C_{ob}	–	300	pF
2N6055, 2N6056, 2N6300, 2N6301		–	200	
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	–	–

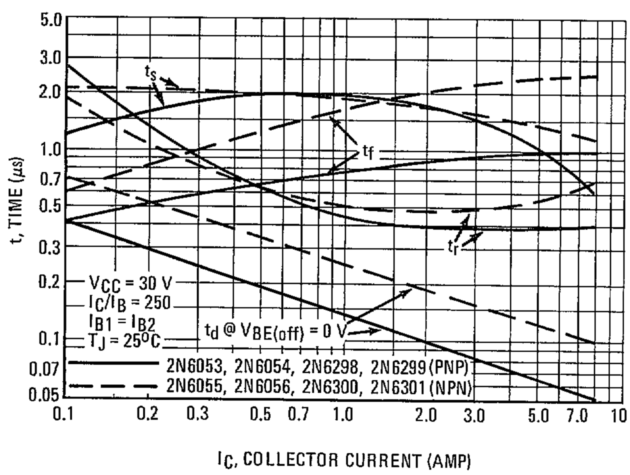
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0 %.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode, polarities and input pulses.

FIGURE 3 — SWITCHING TIMES



PNP — 2N6053, 2N6054, 2N6298, 2N6299

NPN — 2N6055, 2N6056, 2N6300, 2N6301

FIGURE 12 – TEMPERATURE COEFFICIENTS

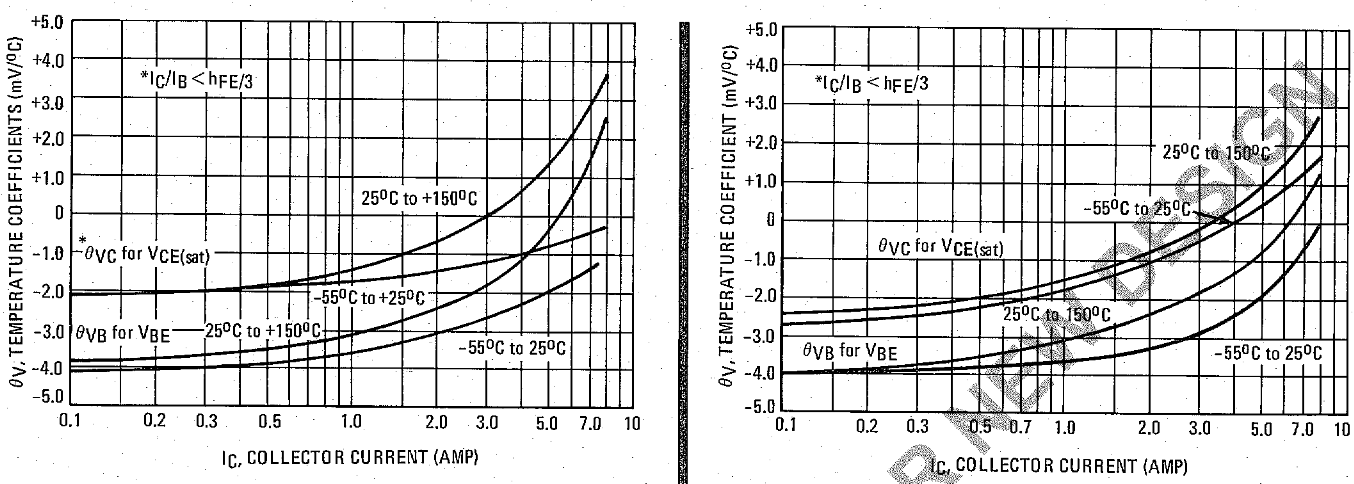


FIGURE 13 – COLLECTOR CUT-OFF REGION

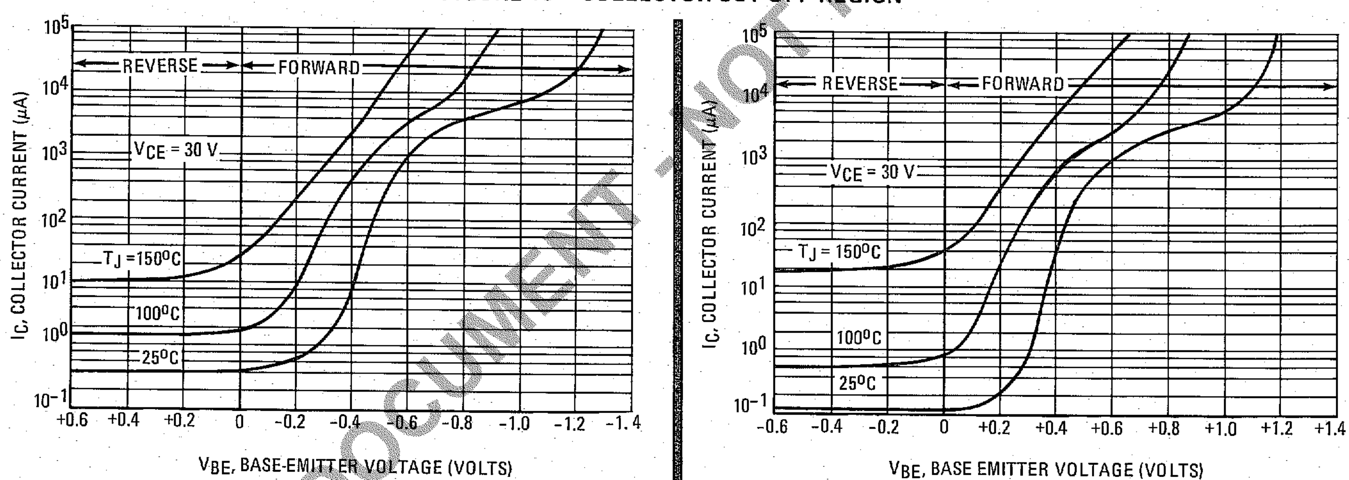
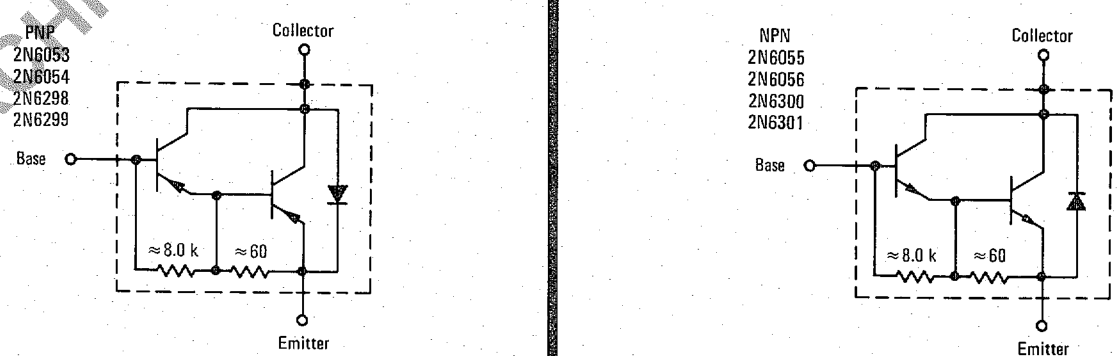


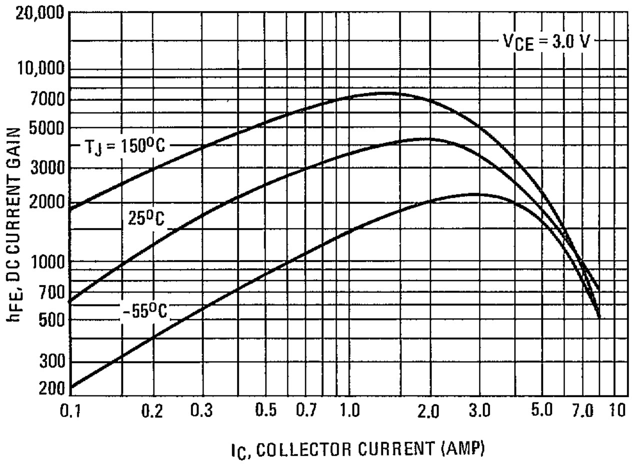
FIGURE 14 – DARLINGTON SCHEMATIC



PNP — 2N6053, 2N6054, 2N6298, 2N6299

NPN — 2N6055, 2N6056, 2N6300, 2N6301

FIGURE 9 — DC CURRENT GAIN



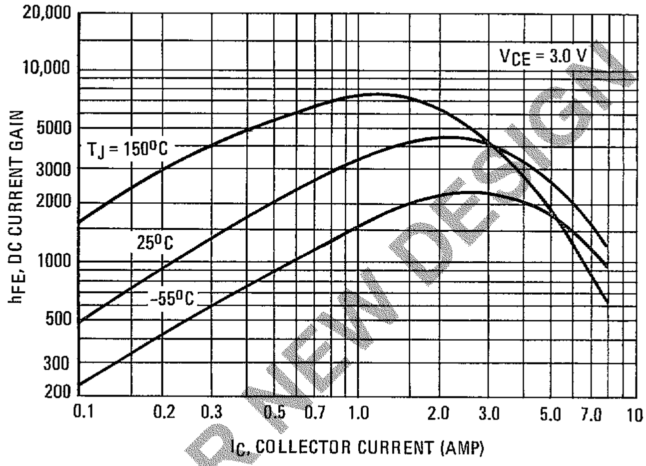
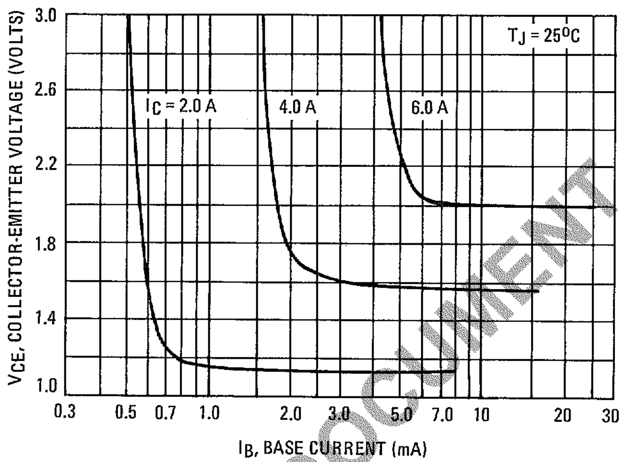


FIGURE 10 — COLLECTOR SATURATION REGION



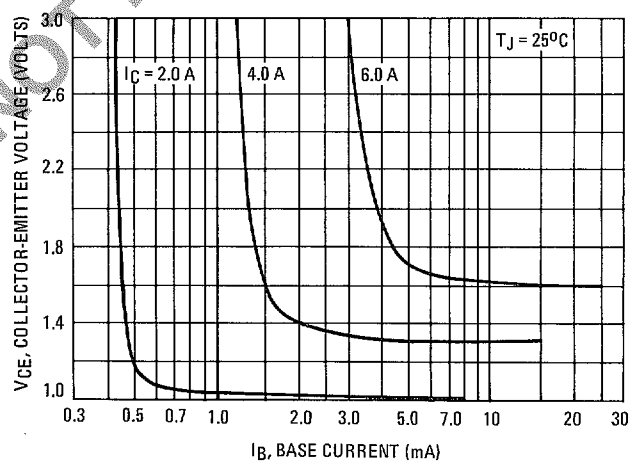
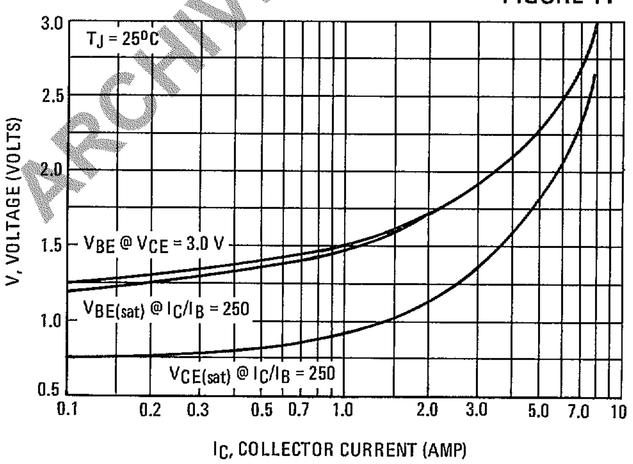


FIGURE 11 — "ON" VOLTAGES



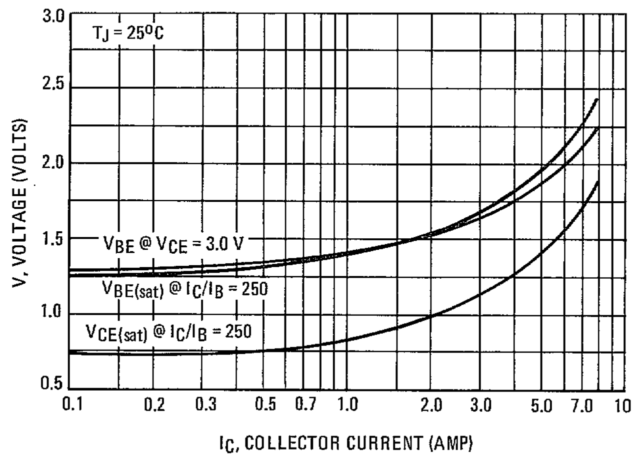
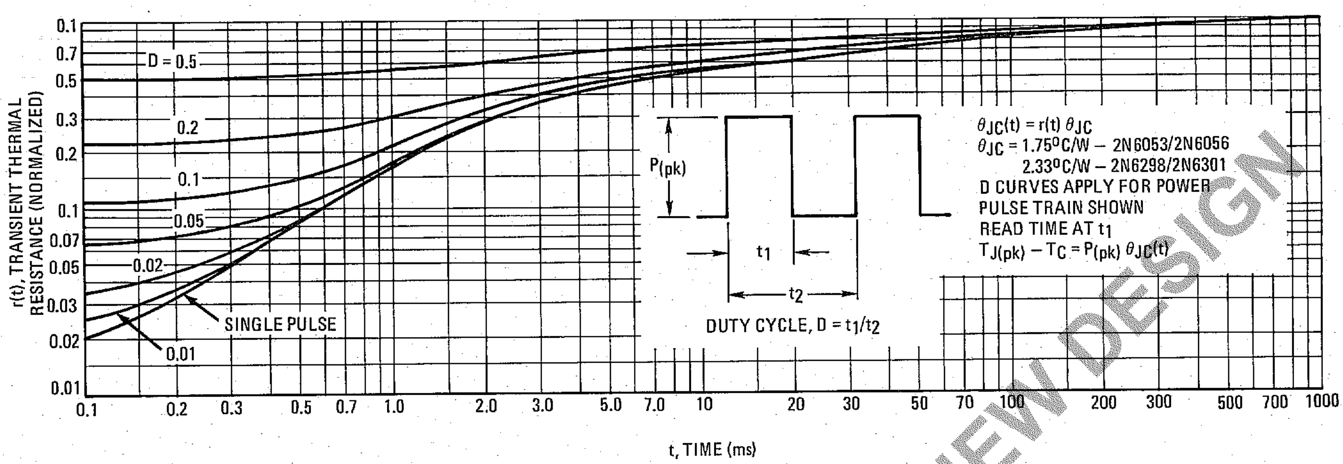


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6053 thru 2N6056

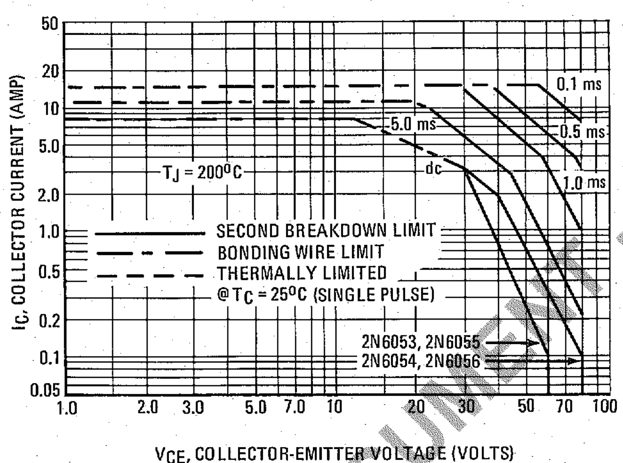
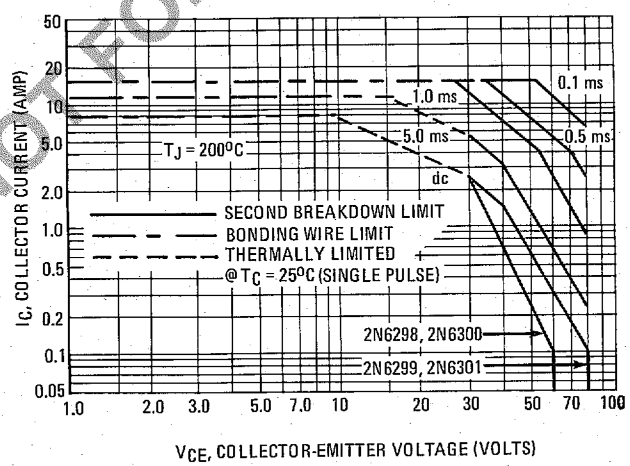


FIGURE 6 – 2N6298 thru 2N6301



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

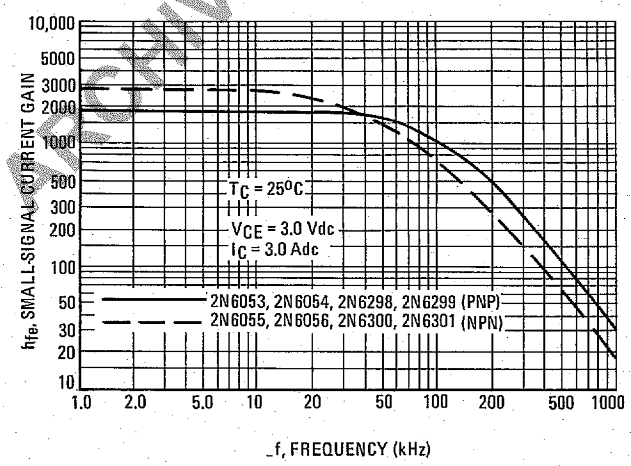
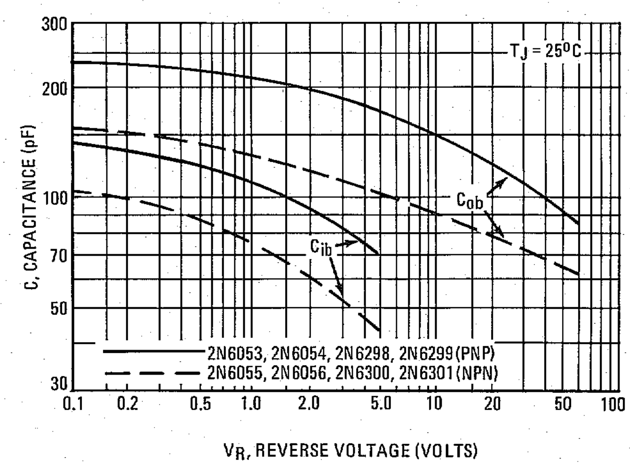


FIGURE 8 – CAPACITANCE



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