Data Sheet | July 2003 | FN5042.4

5GHz VCO

The ISL3084 is a 5GHz SiGe monolithic VCO circuit designed to simplify and reduce the cost and size of miniature wireless transceivers.

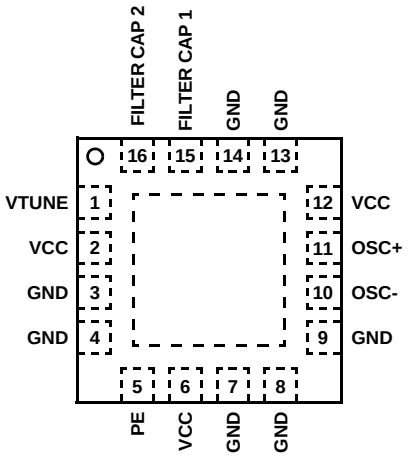
A fully integrated VCO requiring no external elements such as inductors and varactors greatly simplifies low cost local oscillator synthesized applications.

Included in this differential design is a low-power standby function and a stable process and temperature biasing operation.

The ISL3084 is housed in a 16 lead QFN package well-suited for PCMCIA and miniPCI board applications.

Pinout

ISL3084 (QFN)
TOP VIEW



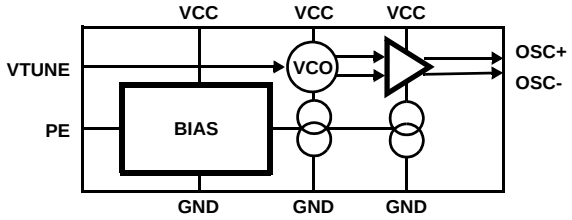
Features

- Single Supply . . . . . 2.7V to 3.3V
- Frequency . . . . . 4.9GHz typical
- Fully Integrated/No External Varactors or Resonators Required
- Isolation Output Buffer/Reduced Load Pulling
- Differential Design/Reduced Spurs
- Digitally Controlled Power Down Mode
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile

Applications

- Systems Targeting IEEE802.11b, 11Mbps Standard
- Only required VCO function for Intersil PRISM®3 chip set
- WLAN Applications.
- PCMCIA Wireless Transceivers
- TDMA Packet Protocol Radios

Simplified Block Diagram



Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL3084IR	-40 to 85	16 Ld QFN	L16.4x4
ISL3084IR-TK	-40 to 85	Tape and Reel	

Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	VTUNE	Input tuning voltage from loop filter. Sensitivity to external injected noise to KVCO. Careful noise-free layout recommended.
2, 6, 12	VCC	Supply pins. Requires high quality capacitor RF decoupling. Phase noise behavior proportional to supply pushing specifications. Use good quality, low-frequency decoupling/filtering techniques.
5	PE	Power enable control pin: VCO enabled high.
10	OSC-	Differential VCO output. Terminate into 100Ω differential impedance. Terminate one end into 50Ω when single end output with equivalent loss of power.
11	OSC+	
15	FILTER CAP1	Use high quality .68µF filter capacitor to ground.
16	FILTER CAP2	Use high quality .68µF filter capacitor to VCC.
3, 4, 7, 8, 9, 13, 14	GND	Ground
Paddle	N/A	Floating paddle. Grounding is recommended.

Absolute Maximum Ratings

Supply Voltage 3.6V
Voltage on Any Other Pin . . . . . -0.3 to V_{CC} +0.3V
V_{CC} to V_{CC} Decouple . . . . . -0.3 to +0.3V
Any GND to GND . . . . . -0.3 to +0.3V

Operating Conditions

Temperature Range . . . . . -40^{o} to 85^{o}C
Supply Voltage Range . . . . . 2.7V to 3.3V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
QFN Package	47	9

Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
For recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC}, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

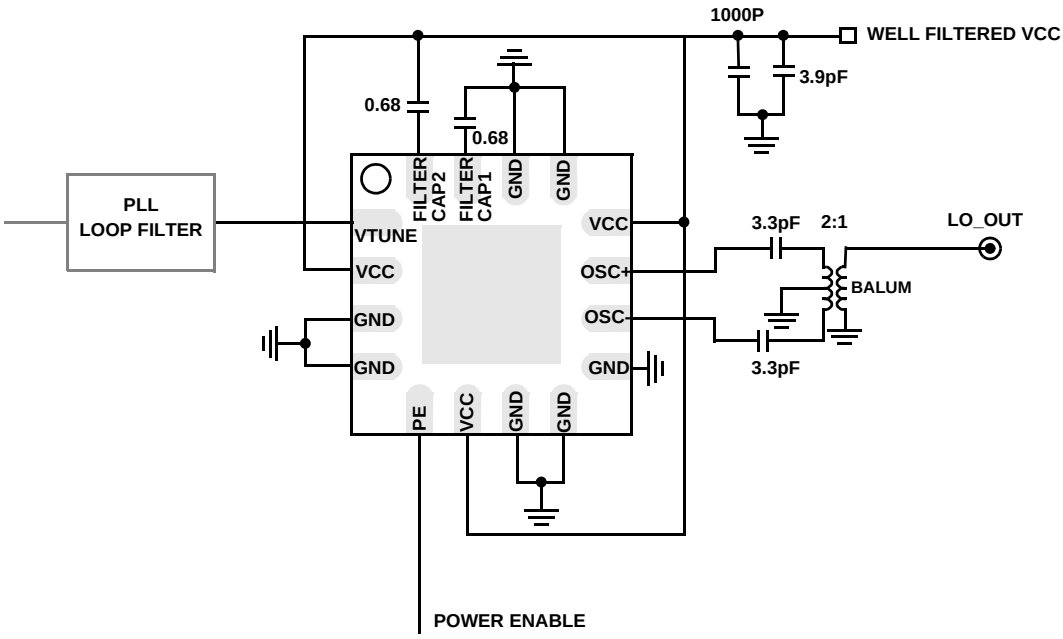
General DC Electrical Specifications TA = 25^{o}C

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage	2.7	-	3.0	V
Supply Current @ 3.3V	-	-	20	mA
Power Down Supply Current	-	-	100	µA
Power Up Time, Filtering dependent	-	50	-	µs
Power Down Time	-	-	1	µs
CMOS Low-Level Input Voltage	-	-	0.3*VCC	V
CMOS High-Level Input Voltage	0.7*V_{CC}	-	-	V
CMOS High- or Low-Level Input Current	-10	-	10	µA

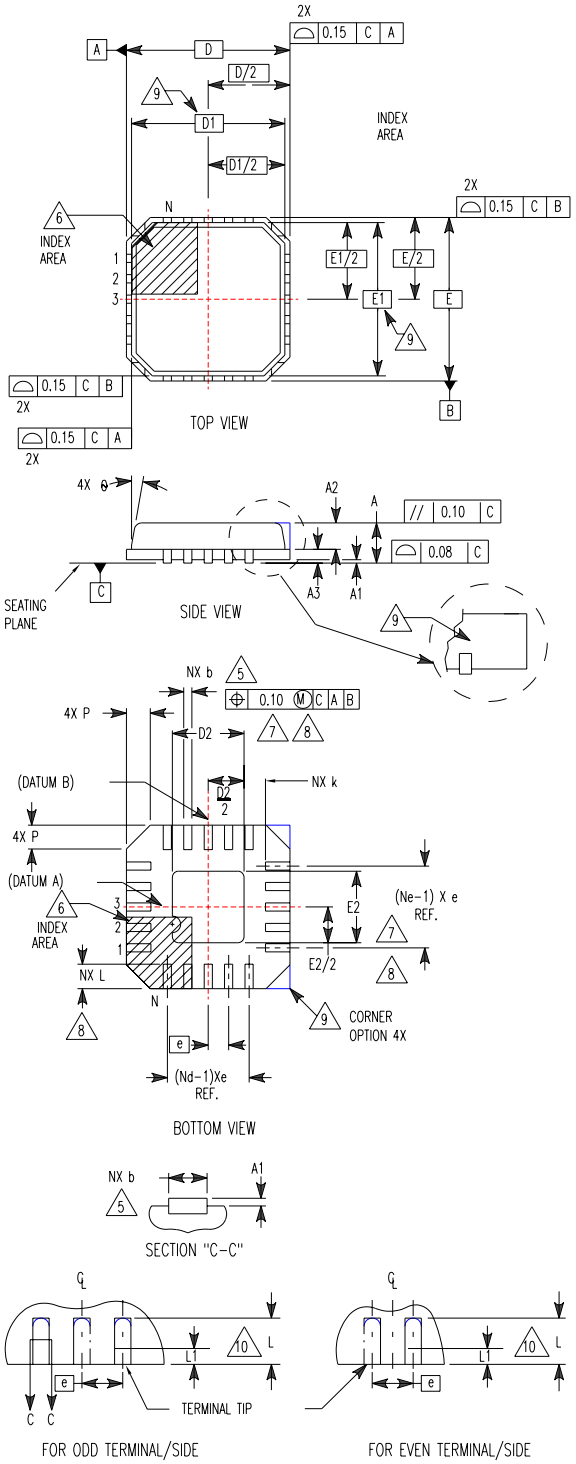
AC Electrical Specifications VCC = 2.7 to 3.3V, Vtune operation from 0.5 to 2.2V, TA = 25^{o}C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Ranges	Vtune = 0.5V	-	4.67	4.79	GHz
	Vtune = 1.35V	-	4.92	-	GHz
	Vtune = 2.2V	5.0	5.19	-	GHz
Tuning Voltage Temperature Coefficient	Vtune = 1.35V, -40 to 85^{o}C	-	40	-	MHz
Tuning Pin Input Leakage	Vtune = 2.0V	-	-	2	µA
VCO Gain	Vtune = 1.35V	250	300	350	MHz/V
VCO Gain Temperature Coefficient	Vtune = 1.35V, -40 to 85^{o}C	-	20	-	MHz/V
Phase Noise	Offset 10kHz	65	70	-	dBc/Hz
	Offset 100kHz	-	95	-	dBc/Hz
Phase Noise Temperature Coefficient	Offset @ 10kHz, 0 to 85^{o}C	-	1	4	dB
Integrated Phase Noise @ 5GHz.	10kHz to 1MHz	-	1.6	-	deg_rms
Output Power	Differential into 100Ω	-9	-4	-	dBm
Supply Pushing	VCC = 2.7V–3.3V, across Vtune range	-3	+2	+10	MHz
Load Pulling	VSWR = 2:1	-	1.8	-	MHz
Output VSWR	2:1 BALUM	-	1.3:1	-	-

Typical Application



Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.