

# ISL3084

Data Sheet

### July 2003

# 5GHz VCO



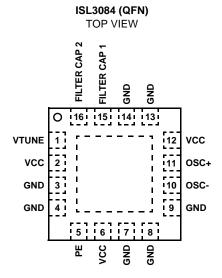
The ISL3084 is a 5GHz SiGe monolithic VCO circuit designed to simplify and reduce the cost and size of miniature wireless transceivers.

A fully integrated VCO requiring no external elements such as inductors and varactors greatly simplifies low cost local oscillator synthesized applications.

Included in this differential design is a low-power standby function and a stable process and temperature biasing operation.

The ISL3084 is housed in a 16 lead QFN package well-suited for PCMCIA and miniPCI board applications.

## Pinout



# Pin Descriptions

#### PIN NUMBER NAME DESCRIPTION VTUNE Input tuning voltage from loop filter. Sensitivity to external injected noise to KVCO. Careful noise-free 1 lavout recommended. VCC Supply pins. Requires high quality capacitor RF decoupling. Phase noise behavior proportional to supply 2, 6, 12 pushing specifications. Use good quality, low-frequency decoupling/filtering techniques. 5 ΡE Power enable control pin: VCO enabled high. Differential VCO output. Terminate into $100\Omega$ differential impedance. Terminate one end into $50\Omega$ when 10 OSCsingle end output with equivalent loss of power. 11 OSC+ 15 FILTER CAP1 Use high quality .68µF filter capacitor to ground. **FILTER CAP2** 16 Use high quality .68µF filter capacitor to VCC. 3, 4, 7, 8, 9, 13, 14 GND Ground Paddle N/A Floating paddle. Grounding is recommended.

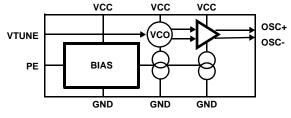
# Features

- Single Supply ..... 2.7V to 3.3V
- Frequency ...... 4.9GHz typical
- Fully Integrated/No External Varactors or Resonators Required
- Isolation Output Buffer/Reduced Load Pulling
- Differential Design/Reduced Spurs
- Digitally Controlled Power Down Mode
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile

## Applications

- Systems Targeting IEEE802.11b, 11Mbps Standard
- Only required VCO function for Intersil PRISM®3 chip set
- WLAN Applications.
- PCMCIA Wireless Transceivers
- TDMA Packet Protocol Radios

## Simplified Block Diagram



# **Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL3084IR	-40 to 85	16 Ld QFN	L16.4x4
ISL3084IR-TK	-40 to 85	Tape and Reel	

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CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. 1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc. Copyright © Intersil Americas Inc. 2003. All Rights Reserved. All other trademarks mentioned are the property of their respective owners. PRISM® is a registered trademark of Intersil Americas Inc. PRISM and design is a trademark of Intersil Americas Inc.

#### **Absolute Maximum Ratings**

Supply Voltage	/
Voltage on Any Other Pin0.3 to V <sub>CC</sub> +0.3	/
V <sub>CC</sub> to V <sub>CC</sub> Decouple	/
Any GND to GND	/

#### **Operating Conditions**

Temperature Range	40 <sup>o</sup> to 85 <sup>o</sup> C
Supply Voltage Range	

#### **Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( <sup>o</sup> C/W)	$\theta_{JC}$ (°C/W)
QFN Package	47	9
Junction Temperature (Plastic Package)		150 <sup>0</sup> C
Maximum Storage Temperature Range .		5 <sup>o</sup> C to 150 <sup>o</sup> C
For recommended soldering conditions se	ee Tech Brief	TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ<sub>JA</sub> is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ<sub>JC</sub>, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

#### **General DC Electrical Specifications** TA = 25°C

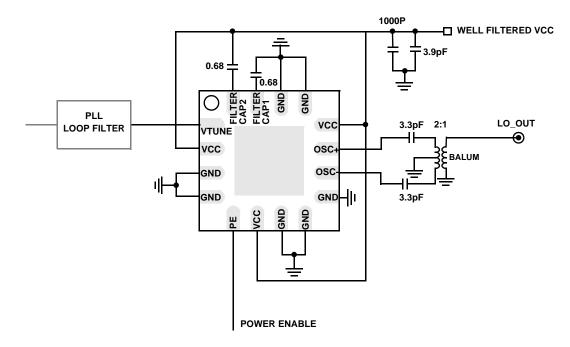
PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage	2.7	-	3.0	V
Supply Current @ 3.3V	-	-	20	mA
Power Down Supply Current	-	-	100	μA
Power Up Time, Filtering dependent	-	50	-	μS
Power Down Time	-	-	1	μS
CMOS Low-Level Input Voltage	-	-	0.3*VCC	V
CMOS High-Level Input Voltage	0.7*V <sub>CC</sub>	-	-	V
CMOS High- or Low-Level Input Current	-10	-	10	μA

#### AC Electrical Specifications VCC = 2.7 to 3.3V, Vtune operation from 0.5 to 2.2V, TA = 25°C

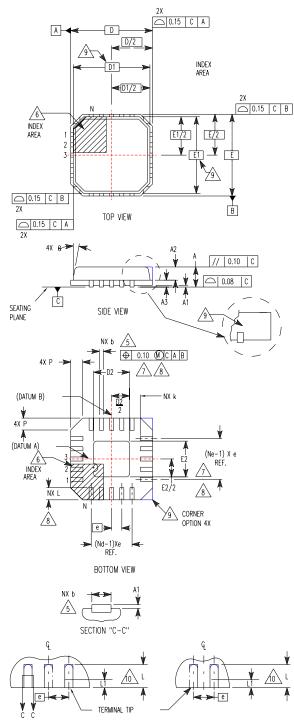
TEST CONDITIONS	MIN	TYP	MAX	UNITS
Vtune = 0.5V	-	4.67	4.79	GHz
Vtune = 1.35V	-	4.92	-	GHz
Vtune = 2.2V	5.0	5.19	-	GHz
Vtune = 1.35V, -40 to 85 <sup>o</sup> C	-	40	-	MHz
Vtune = 2.0V	-	-	2	μΑ
Vtune = 1.35V	250	300	350	MHz/V
Vtune = 1.35V, -40 to 85 <sup>o</sup> C	-	20	-	MHz/V
Offset 10kHz	65	70	-	dBc/Hz
Offset 100kHz	-	95	-	dBc/Hz
Offset @ 10kHz, 0 to 85 <sup>0</sup> C	-	1	4	dB
10kHz to 1MHz	-	1.6	-	deg_rms
Dutput Power Differential into 100Ω		-4	-	dBm
pply Pushing VCC = 2.7V–3.3V, across Vtune range		+2	+10	MHz
d Pulling VSWR = 2:1		1.8	-	MHz
2:1 BALUM	-	1.3:1	-	-
	Vtune = $0.5V$ Vtune = $1.35V$ Vtune = $2.2V$ Vtune = $1.35V$ , -40 to $85^{\circ}C$ Vtune = $2.0V$ Vtune = $1.35V$ Vtune = $1.35V$ Vtune = $1.35V$ Offset 10kHz         Offset 100kHz         Offset $00kHz$ Offset $00kHz$ Differential into $100\Omega$ VCC = $2.7V-3.3V$ , across Vtune range         VSWR = $2:1$	Vtune = $0.5V$ -           Vtune = $1.35V$ -           Vtune = $2.2V$ $5.0$ Vtune = $1.35V$ , -40 to $85^{\circ}C$ -           Vtune = $2.0V$ -           Vtune = $1.35V$ , -40 to $85^{\circ}C$ -           Vtune = $1.35V$ 250           Vtune = $1.35V$ , -40 to $85^{\circ}C$ -           Offset 10kHz         65           Offset 100kHz         -           Offset $@ 10kHz$ , 0 to $85^{\circ}C$ -           I0kHz to 1MHz         -           Differential into $100\Omega$ -9           VCC = $2.7V$ - $3.3V$ , across Vtune range         -3           VSWR = $2:1$ -	Vtune = $0.5V$ -       4.67         Vtune = $1.35V$ -       4.92         Vtune = $2.2V$ 5.0       5.19         Vtune = $1.35V$ , -40 to $85^{\circ}C$ -       40         Vtune = $2.0V$ -       -         Vtune = $1.35V$ , -40 to $85^{\circ}C$ -       40         Vtune = $1.35V$ , -40 to $85^{\circ}C$ -       20         Vtune = $1.35V$ , -40 to $85^{\circ}C$ -       20         Offset $10kHz$ 65       70         Offset $10kHz$ 65       70         Offset $10kHz$ -       95         Offset $00kHz$ , 0 to $85^{\circ}C$ -       1         10kHz to $1MHz$ -       1.6         Differential into $100\Omega$ -9       -4         VCC = $2.7V$ - $3.3V$ , across Vtune range       -3       +2         VSWR = 2:1       -       1.8	Vtune = $0.5V$ - $4.67$ $4.79$ Vtune = $1.35V$ - $4.92$ -Vtune = $2.2V$ $5.0$ $5.19$ -Vtune = $1.35V, -40$ to $85^{\circ}C$ - $40$ -Vtune = $1.35V, -40$ to $85^{\circ}C$ - $40$ -Vtune = $1.35V, -40$ to $85^{\circ}C$ - $250$ $300$ $350$ Vtune = $1.35V, -40$ to $85^{\circ}C$ - $20$ -Offset $10kHz$ $65$ $70$ -Offset $10kHz$ - $95$ -Offset $0 thHz, 0$ to $85^{\circ}C$ - $1$ $4$ $10kHz$ to $1MHz$ - $1.6$ -Differential into $100\Omega$ -9 $-4$ -VCC = $2.7V-3.3V$ , across Vtune range $-3$ $+2$ $+10$ VSWR = $2:1$ - $1.8$ -

2

# **Typical Application**



3



# Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)

#### FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE

#### L16.4x4

#### 16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

(COMPLIANT	IO JEDEC	MO-220-VGGC I	550E C)	
	MILLIMETERS			
SYMBOL	MIN	NOMINAL	MAX	NOTES
А	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		4.00 BSC		-
D1	3.75 BSC		9	
D2	1.95	2.10	2.25	7, 8
E	4.00 BSC		-	
E1	3.75 BSC		9	
E2	1.95	2.10	2.25	7, 8
е	0.65 BSC		-	
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
Ν	16		2	
Nd	4		3	
Ne	4		3	
Р	-	-	0.60	9
θ	-	-	12	9
			F	Rev. 4 10/02

#### NOTES:

- 1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
- 2. N is the number of terminals.
- 3. Nd and Ne refer to the number of terminals on each D and E.
- 4. All dimensions are in millimeters. Angles are in degrees.
- 5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- 6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
- 7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
- 8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
- 9. Features and dimensions A2, A3, D1, E1, P & 0 are present when Anvil singulation method is used and not present for saw singulation.
- Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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