

**MJE1320**

*Designer's™ Data Sheet*  
**NPN Silicon Power Transistor**  
**Switchmode Series**

This transistor is designed for high-voltage, power switching in inductive circuits where RBSOA and breakdown voltage are critical. They are particularly suited for line-operated switchmode applications.

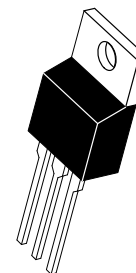
**Typical Applications:**

- Fluorescent Lamp Ballasts
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

**Features:**

- High  $V_{CEV}$  Capability (1800 Volts)
- Low Saturation Voltage
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

**POWER TRANSISTOR**  
**2 AMPERES**  
**900 VOLTS**  
**80 WATTS**



**CASE 221A-06**  
**TO-220AB**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	900	Vdc
Collector-Emitter Voltage	$V_{CEV}$	1800	Vdc
Emitter Base Voltage	$V_{EB}$	9	Vdc
Collector Current — Continuous	$I_C$	2	Adc
Peak(1)	$I_{CM}$	5	
Base Current — Continuous	$I_B$	1.5	Adc
Peak(1)	$I_{BM}$	2.5	
Total Power Dissipation @ $T_C = 25^\circ C$	$P_D$	80	Watts
@ $T_C = 100^\circ C$		32	
Derate above 25°C		0.64	W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

SWITCHMODE is a trademark of Motorola, Inc.

# MJE1320

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 50\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	900	—	—	Vdc
Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$I_{CEV}$	—	—	0.25 2.5	mAdc
Emitter Cutoff Current ( $V_{EB} = 9\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	0.25	mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			

## ON CHARACTERISTICS(1)

DC Current Gain ( $V_{CE} = 5\text{ Vdc}$ )	$I_C = 2\text{ Adc}$ $I_C = 1\text{ Adc}$	$h_{FE}$	2.5 3	4.5 7	— —	— —
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 1\text{ Adc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )		$V_{CE(sat)}$	— — —	0.18 0.3 0.3	1 2.5 1.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 1\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 1\text{ Adc}$ ) ( $I_C = 1\text{ Adc}$ , $I_B = 0.5\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )		$V_{BE(sat)}$	— — —	0.2 0.9 0.15	1.5 2.8 1.5	Vdc

## DYNAMIC CHARACTERISTICS

Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	—	80	—	pF
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## SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$V_{CC} = 250\text{ Vdc}$ , $I_C = 1\text{ A}$ $I_{B1} = I_{B2} = 0.5\text{ Adc}$ $t_p = 25\text{ }\mu\text{s}$ , Duty Cycle $\leq 2\%$	$t_d$	—	0.1	—	$\mu\text{s}$	
Rise Time		$t_r$	—	0.8	—	$\mu\text{s}$	
Storage Time		$t_s$	—	4	—	$\mu\text{s}$	
Fall Time		$t_f$	—	0.8	—	$\mu\text{s}$	
Inductive Load, Clamped (Table 2)							
Storage Time	$I_C = 1\text{ A}$ , $V_{clamp} = 400\text{ Vdc}$ , $V_{BE(off)} = 2\text{ Vdc}$ , $I_{B1} = 0.5\text{ Adc}$	$T_C = 25^\circ\text{C}$	$t_{sv}$	—	2.8	—	$\mu\text{s}$
Crossover Time			$t_c$	—	2.2	—	$\mu\text{s}$
Storage Time		$T_C = 100^\circ\text{C}$	$t_{sv}$	—	3.7	10.5	$\mu\text{s}$
Crossover Time			$t_c$	—	3.5	10	$\mu\text{s}$
Fall Time							

(1) Pulse Test: Pulse Width = 300  $\mu\text{s}$ . Duty Cycle  $\leq 2\%$ .

TYPICAL STATIC CHARACTERISTICS

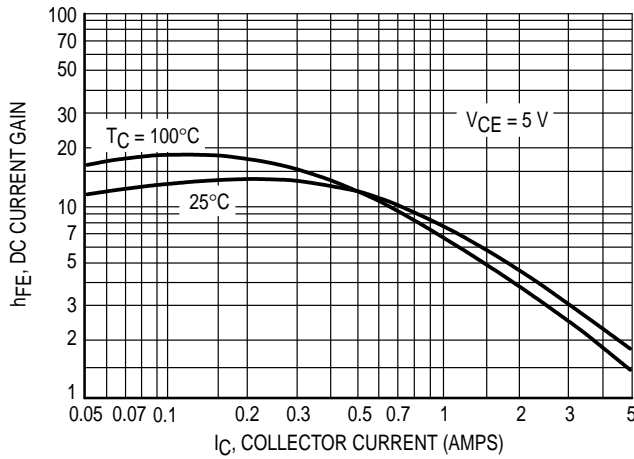


Figure 1. DC Current Gain

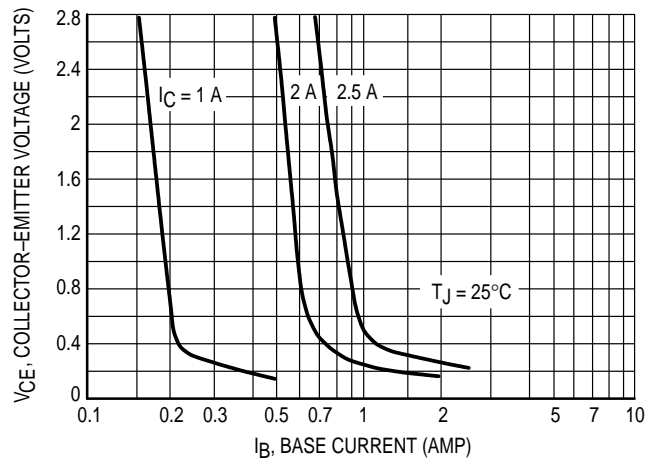


Figure 2. Collector Saturation Region

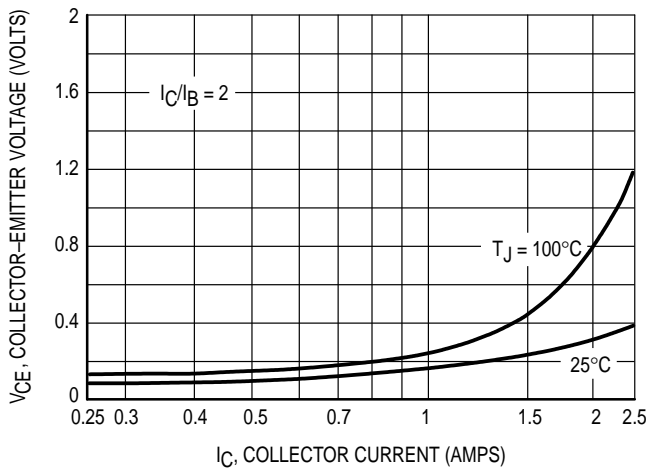


Figure 3. Collector-Emitter Saturation Voltage

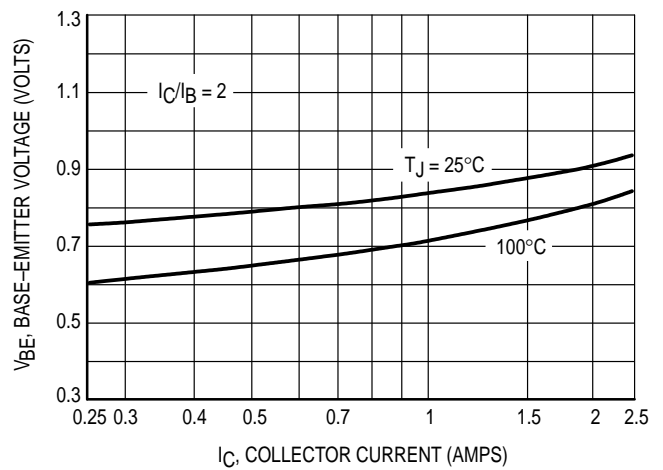


Figure 4. Base-Emitter Saturation Voltage

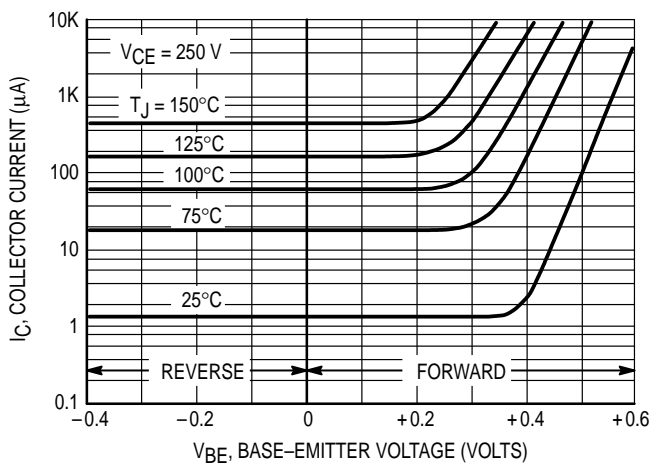


Figure 5. Collector Cutoff Region

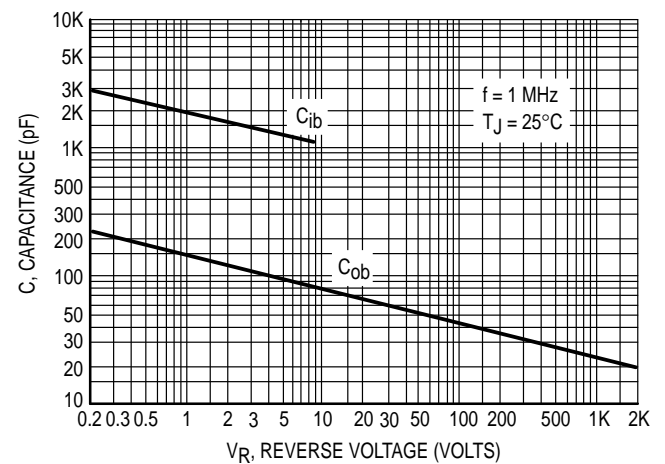


Figure 6. Capacitance Variation

TYPICAL DYNAMIC CHARACTERISTICS

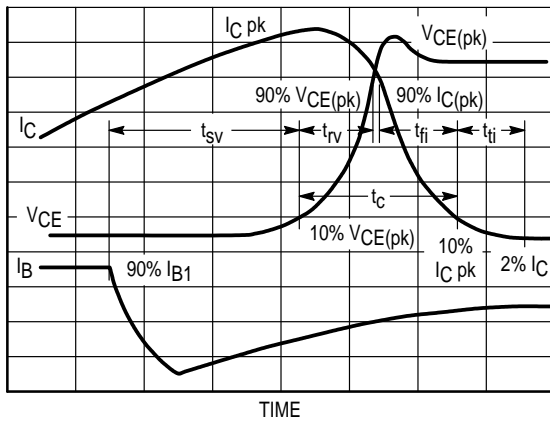


Figure 7. Inductive Switching Measurements

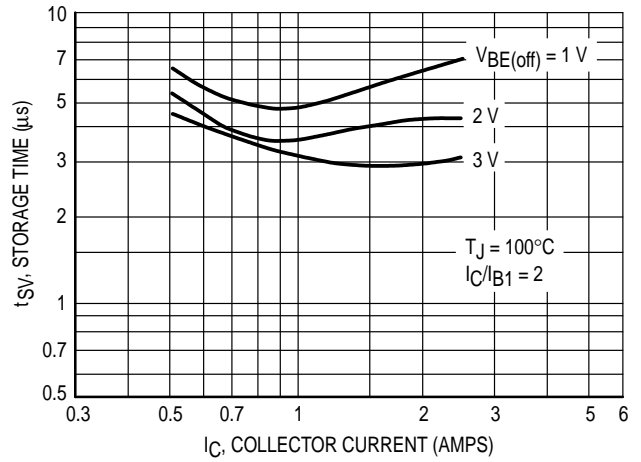


Figure 8. Inductive Storage Time

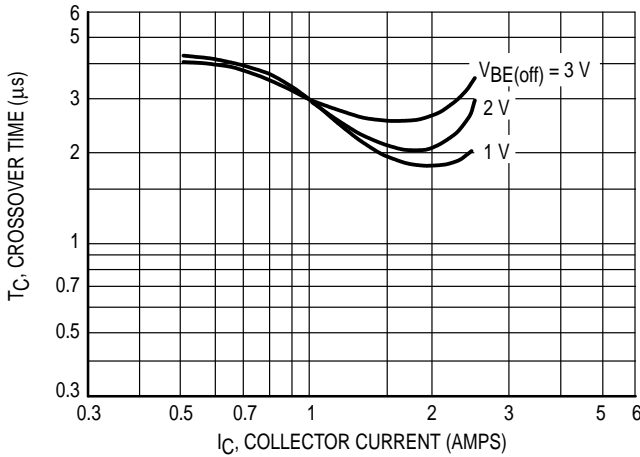


Figure 9. Inductive Crossover Time

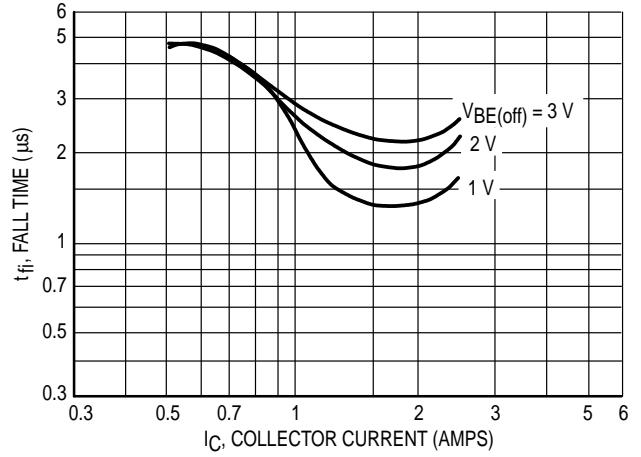
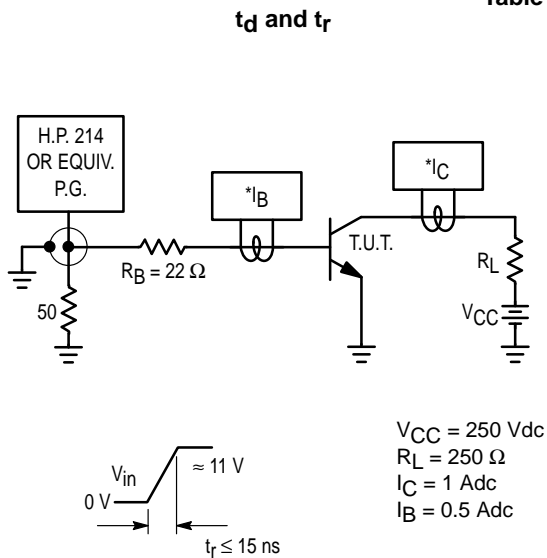


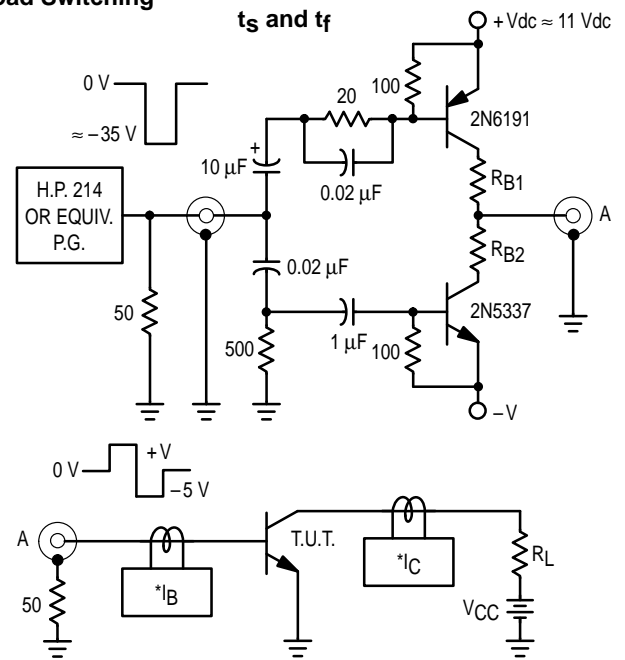
Figure 10. Inductive Fall Time

Table 1. Resistive Load Switching



$V_{CC} = 250 \text{ Vdc}$   
 $R_L = 250 \Omega$   
 $I_C = 1 \text{ Adc}$   
 $I_B = 0.5 \text{ Adc}$

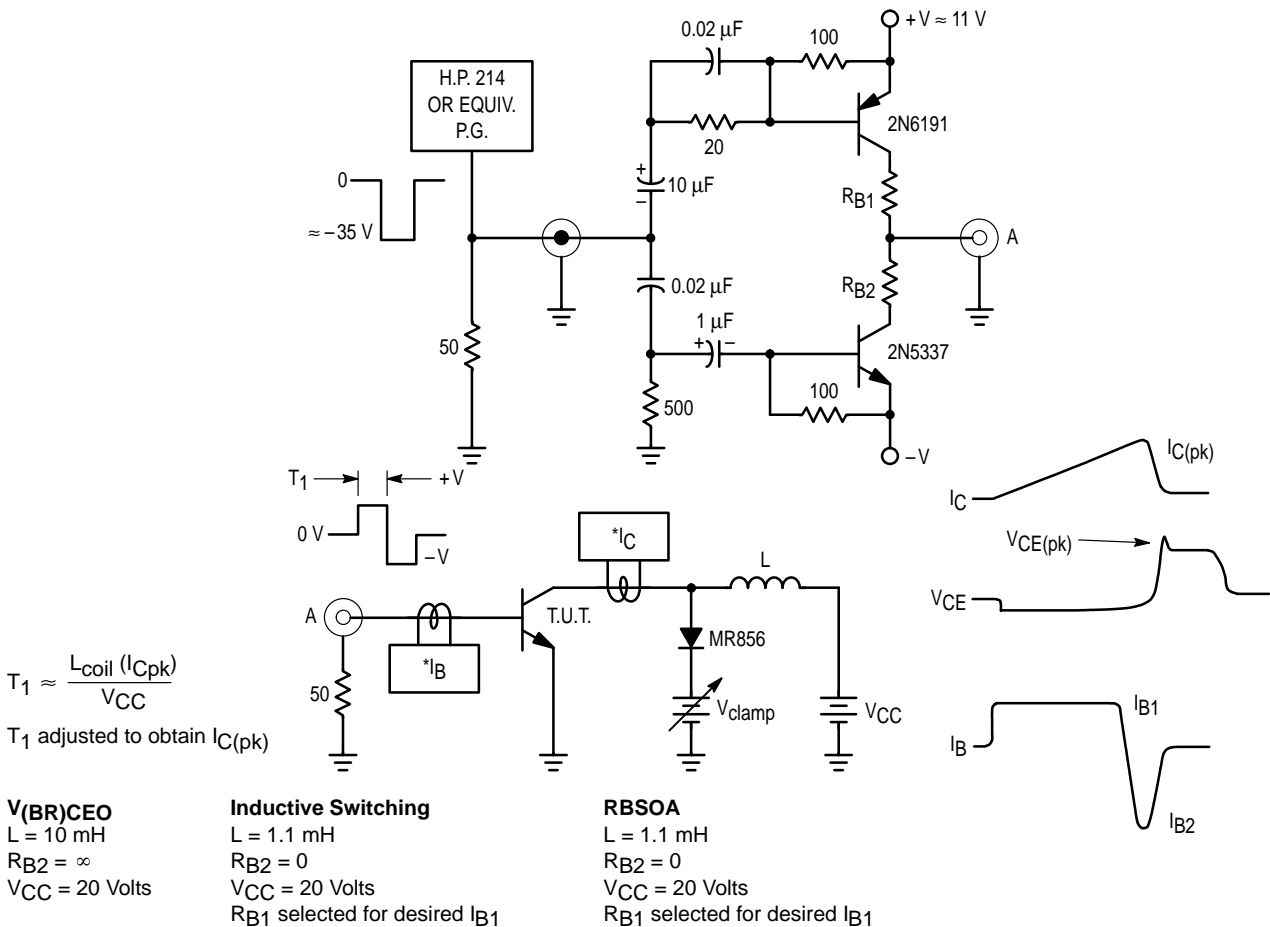
\*Tektronix AM503  
 P6302 or Equivalent



$V_{CC} = 250 \text{ Vdc}$      $I_{B1} = 0.5 \text{ Adc}$      $R_{B1} = 22 \Omega$   
 $R_L = 250 \Omega$      $I_{B2} = 0.5 \text{ Adc}$      $R_{B2} = 10 \Omega$   
 $I_C = 1 \text{ Adc}$     For  $V_{BE(off)} = 5 \text{ V}$      $R_{B2} = 0 \Omega$

Note: Adjust -V to obtain desired  $V_{BE(off)}$  at Point A.

Table 2. Inductive Load Switching



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T<sub>1</sub> adjusted to obtain I<sub>C(pk)</sub>

**V(BR)CEO**  
 L = 10 mH  
 R<sub>B2</sub> = ∞  
 V<sub>CC</sub> = 20 Volts

**Inductive Switching**  
 L = 1.1 mH  
 R<sub>B2</sub> = 0  
 V<sub>CC</sub> = 20 Volts  
 R<sub>B1</sub> selected for desired I<sub>B1</sub>

**RBSOA**  
 L = 1.1 mH  
 R<sub>B2</sub> = 0  
 V<sub>CC</sub> = 20 Volts  
 R<sub>B1</sub> selected for desired I<sub>B1</sub>

\*Tektronix  
 P-6042 or  
 Equivalent

Scope — Tektronix  
 7403 or  
 Equivalent

Note: Adjust -V to obtain desired V<sub>BE(off)</sub> at Point A.

**SAFE OPERATING AREA INFORMATION**

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I<sub>C</sub> - V<sub>CE</sub> limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T<sub>C</sub> = 25°C; T<sub>J(pk)</sub> is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T<sub>C</sub> ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 11.

T<sub>J(pk)</sub> may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the

power that can be handled to values less than the limitations imposed by second breakdown.

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA

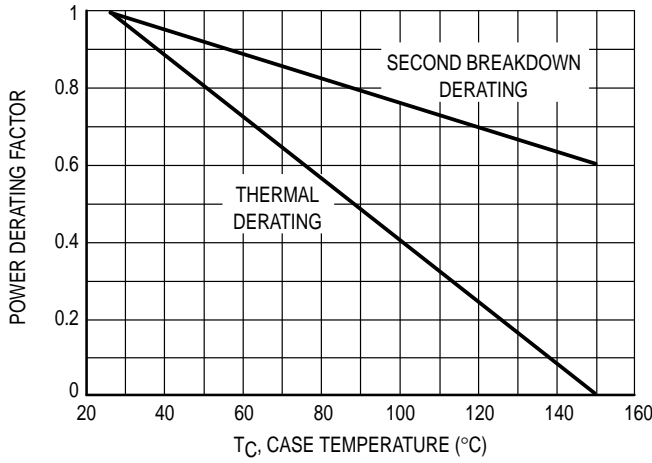


Figure 11. Power Derating

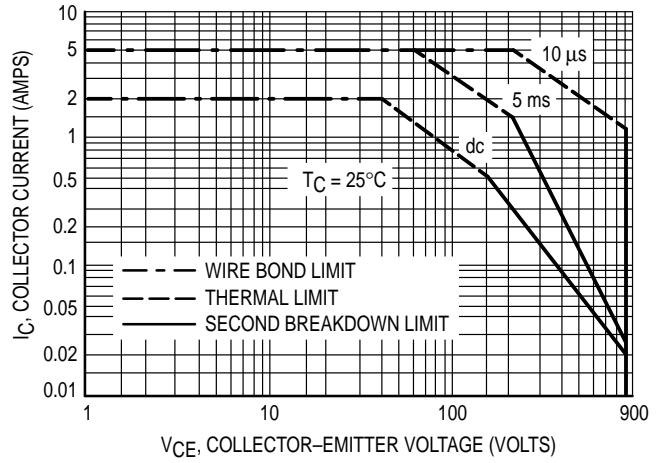


Figure 12. Maximum Rated Forward Bias Safe Operating Area

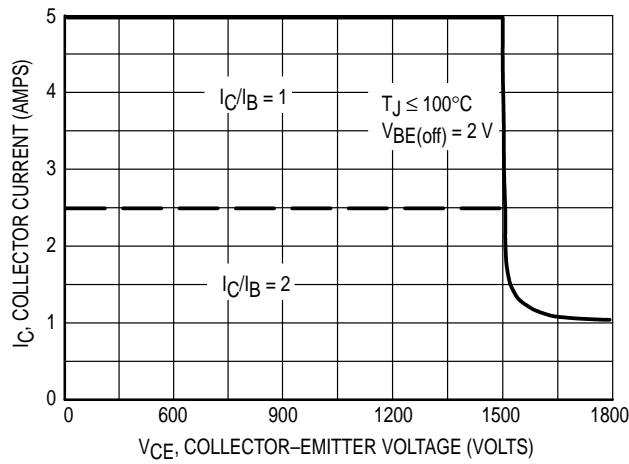


Figure 13. Maximum Rated Reverse Bias Safe Operating Area

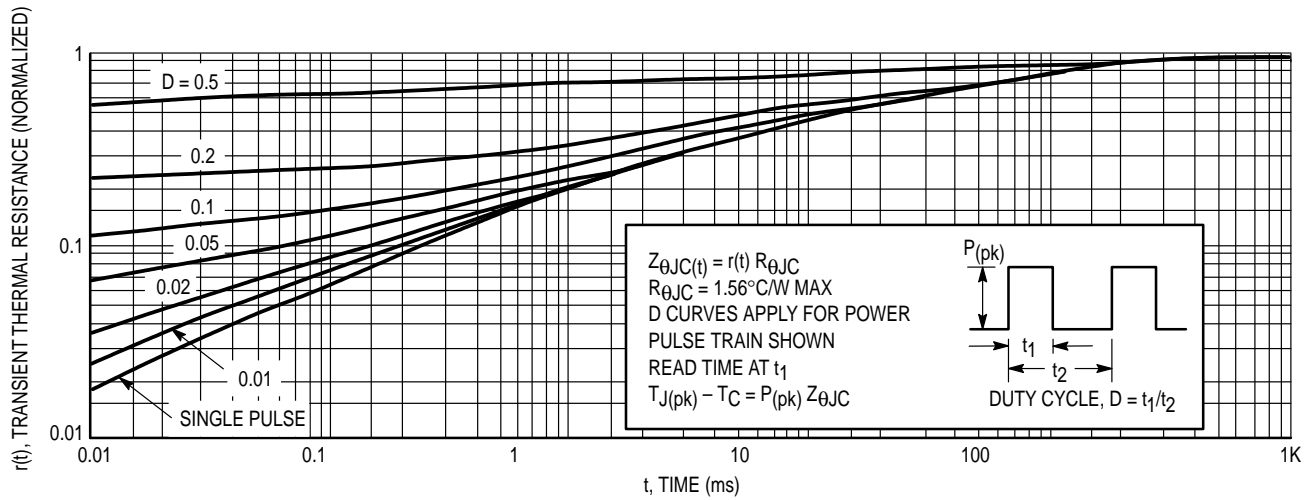
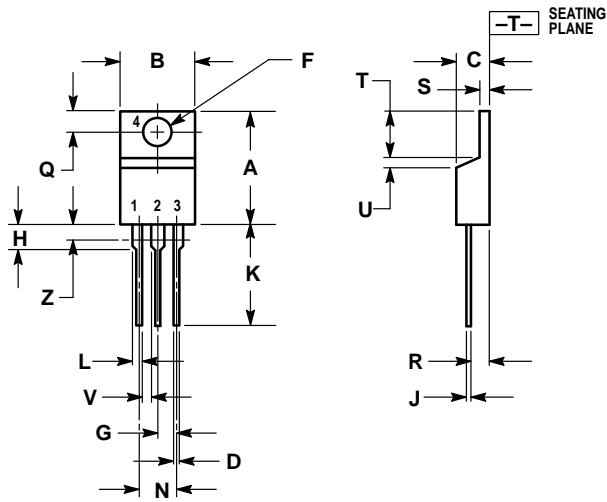


Figure 14. Thermal Response

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

- STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

CASE 221A-06  
 TO-220AB  
 ISSUE Y

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**MJE1320/D**