

SSTUH32866

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1.8 V high output drive 25-bit 1 : 1 or 14-bit 1 : 2 configurable registered buffer with parity for DDR2 RDIMM applications

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Product data sheet

1. General description

The SSTUH32866 is a 1.8 V configurable register specifically designed for use on DDR2 memory modules requiring a parity checking function. It is defined in accordance with the JEDEC JESD82-7 standard for the SSTU32864 registered buffer, while adding the parity checking function in a compatible pinout. The JEDEC standard for SSTUH32866 is pending publication. The register is configurable (using configuration pins C0 and C1) to two topologies: 25-bit 1 : 1 or 14-bit 1 : 2, and in the latter configuration can be designated as Register A or Register B on the DIMM.

The SSTUH32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain \overline{QERR} pin (active LOW). The convention is even parity, that is, valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

The SSTUH32866 is packaged in a 96-ball, 6 × 16 grid, 0.8 mm ball pitch LFBGA package (13.5 mm × 5.5 mm).

The SSTUH32866 is identical to SSTU32866 in function and performance, with higher-drive outputs optimized to drive heavy load nets (for example, stacked DRAMs) while maintaining speed and signal integrity.

2. Features

- Configurable register supporting DDR2 Registered DIMM applications
- Higher output drive strength version of SSTU32866 optimized for high-capacitive load nets
- Configurable to 25-bit 1 : 1 mode or 14-bit 1 : 2 mode
- Controlled output impedance drivers enable optimal signal integrity and speed
- Exceeds JESD82-7 speed performance (1.8 ns max. single-bit switching propagation delay; 2.0 ns max. mass-switching)
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports SSTL_18 data inputs
- Checks parity on the DIMM-independent data inputs
- Partial parity output and input allows cascading of two SSTUH32866s for correct parity error processing
- Differential clock (CK and \overline{CK}) inputs

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- Supports LVCMOS switching levels on the control and $\overline{\text{RESET}}$ inputs
- Single 1.8 V supply operation
- Available in 96-ball, 13.5 mm × 5.5 mm, 0.8 mm ball pitch LFBGA package

3. Applications

- DDR2 registered DIMMs desiring parity checking functionality
- Stacked or planar high-DRAM count registered DIMMs

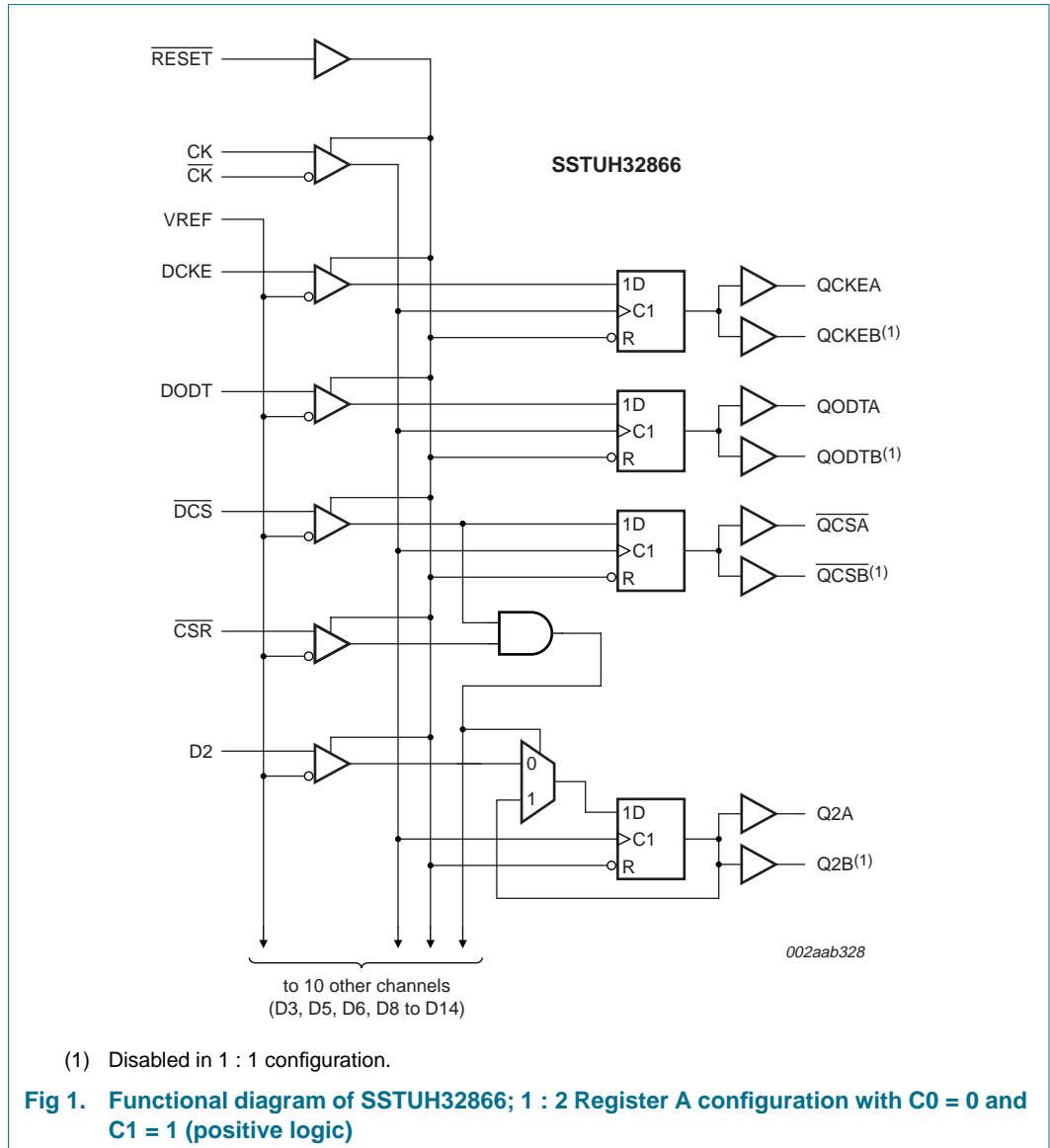
4. Ordering information

Table 1: Ordering information

$T_{amb} = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$.

| Type number | Solder process | Package | | |
|----------------|---------------------------------------|---------|---|----------|
| | | Name | Description | Version |
| SSTUH32866EC/G | Pb-free (SnAgCu solder ball compound) | LFBGA96 | plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm | SOT536-1 |
| SSTUH32866EC | SnPb solder ball compound | LFBGA96 | plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm | SOT536-1 |

5. Functional diagram



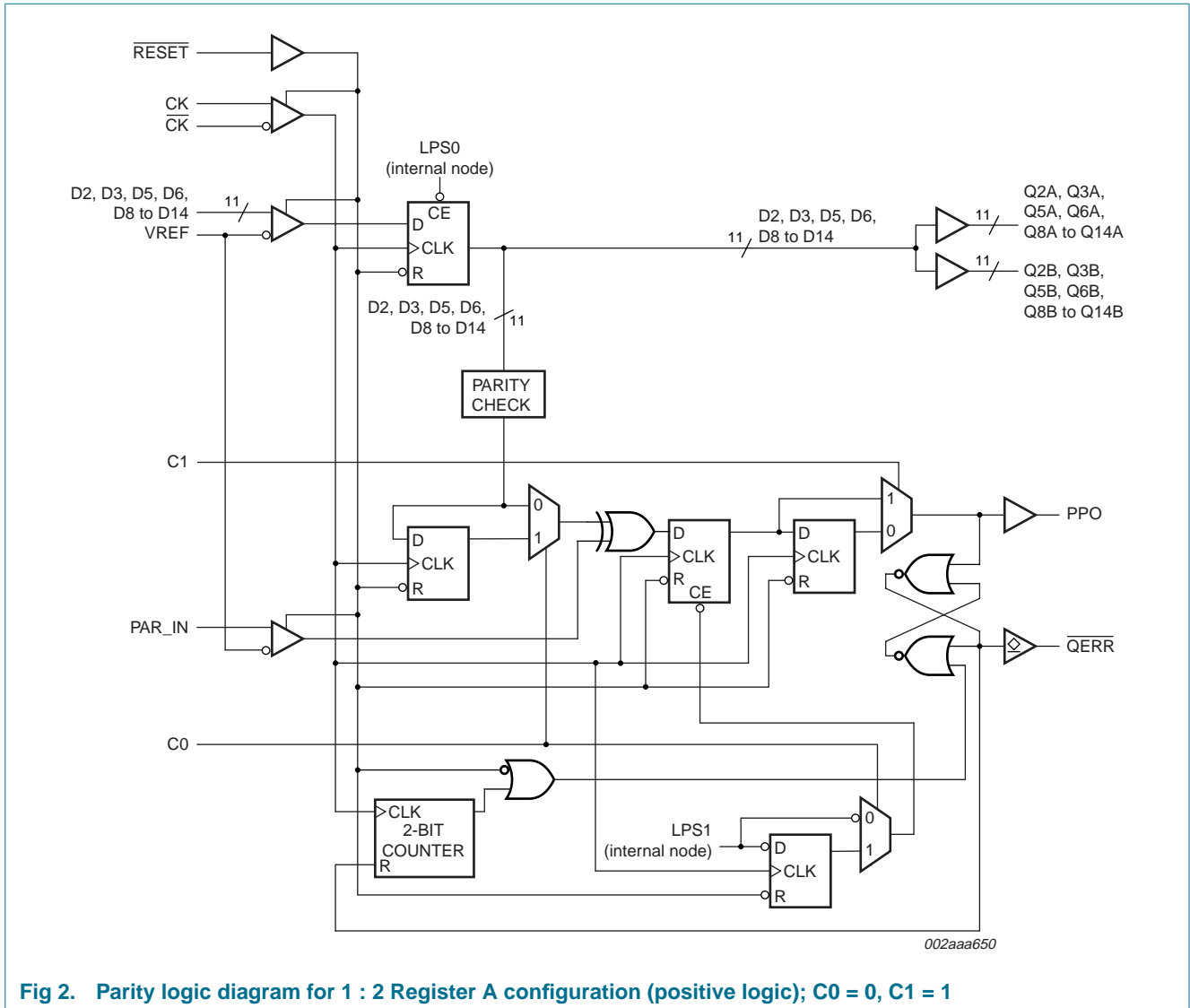
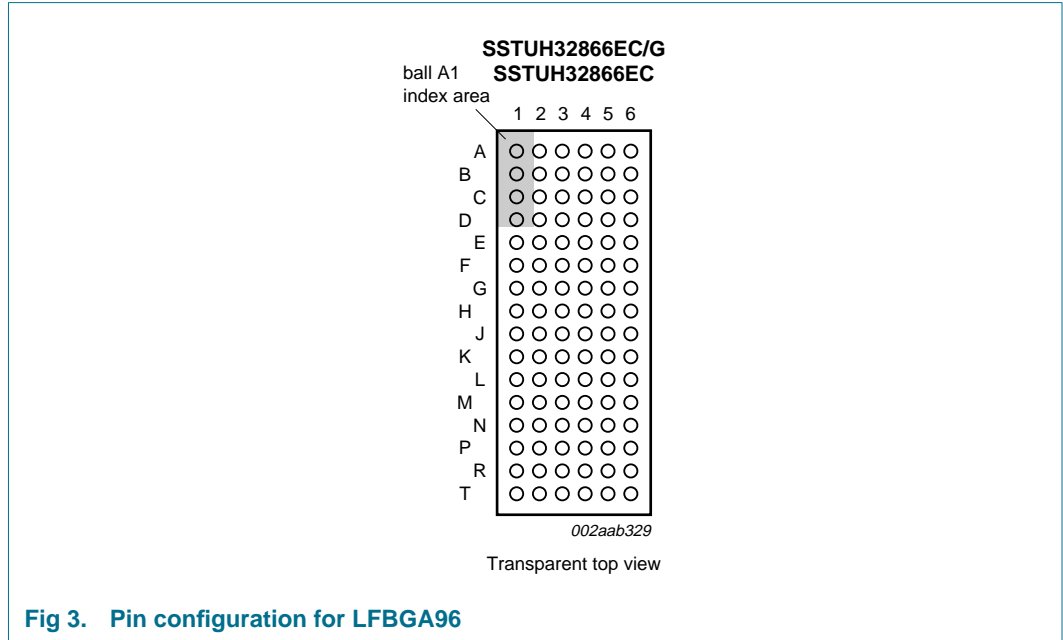


Fig 2. Parity logic diagram for 1 : 2 Register A configuration (positive logic); C0 = 0, C1 = 1

6. Pinning information

6.1 Pinning



| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----------------|--------------------|-----------------|-----------------|------------------|------|
| A | DCKE | PPO | VREF | V _{DD} | QCKE | DNU |
| B | D2 | D15 | GND | GND | Q2 | Q15 |
| C | D3 | D16 | V _{DD} | V _{DD} | Q3 | Q16 |
| D | DODT | \overline{QERR} | GND | GND | QODT | DNU |
| E | D5 | D17 | V _{DD} | V _{DD} | Q5 | Q17 |
| F | D6 | D18 | GND | GND | Q6 | Q18 |
| G | PAR_IN | \overline{RESET} | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | \overline{DCS} | GND | GND | \overline{QCS} | DNU |
| J | \overline{CK} | \overline{CSR} | V _{DD} | V _{DD} | n.c. | n.c. |
| K | D8 | D19 | GND | GND | Q8 | Q19 |
| L | D9 | D20 | V _{DD} | V _{DD} | Q9 | Q20 |
| M | D10 | D21 | GND | GND | Q10 | Q21 |
| N | D11 | D22 | V _{DD} | V _{DD} | Q11 | Q22 |
| P | D12 | D23 | GND | GND | Q12 | Q23 |
| R | D13 | D24 | V _{DD} | V _{DD} | Q13 | Q24 |
| T | D14 | D25 | VREF | V _{DD} | Q14 | Q25 |

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Fig 4. Ball mapping, 1 : 1 register (C0 = 0, C1 = 0)

1.8 V high-drive DDR2 configurable registered buffer with parity

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----------------|--------------------|-----------------|-----------------|-------------------|-------------------|
| A | DCKE | PPO | VREF | V _{DD} | QCKEA | QCKEB |
| B | D2 | DNU | GND | GND | Q2A | Q2B |
| C | D3 | DNU | V _{DD} | V _{DD} | Q3A | Q3B |
| D | DODT | \overline{QERR} | GND | GND | QODTA | QODTB |
| E | D5 | n.c. | V _{DD} | V _{DD} | Q5A | Q5B |
| F | D6 | n.c. | GND | GND | Q6A | Q6B |
| G | PAR_IN | \overline{RESET} | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | \overline{DCS} | GND | GND | \overline{QCSA} | \overline{QCSB} |
| J | \overline{CK} | \overline{CSR} | V _{DD} | V _{DD} | n.c. | n.c. |
| K | D8 | DNU | GND | GND | Q8A | Q8B |
| L | D9 | DNU | V _{DD} | V _{DD} | Q9A | Q9B |
| M | D10 | DNU | GND | GND | Q10A | Q10B |
| N | D11 | DNU | V _{DD} | V _{DD} | Q11A | Q11B |
| P | D12 | DNU | GND | GND | Q12A | Q12B |
| R | D13 | DNU | V _{DD} | V _{DD} | Q13A | Q13B |
| T | D14 | DNU | VREF | V _{DD} | Q14A | Q14B |

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Fig 5. Ball mapping, 1 : 2 Register A (C0 = 0, C1 = 1)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----------------|--------------------|-----------------|-----------------|-------------------|-------------------|
| A | D1 | PPO | VREF | V _{DD} | Q1A | Q1B |
| B | D2 | DNU | GND | GND | Q2A | Q2B |
| C | D3 | DNU | V _{DD} | V _{DD} | Q3A | Q3B |
| D | D4 | \overline{QERR} | GND | GND | Q4A | Q4B |
| E | D5 | DNU | V _{DD} | V _{DD} | Q5A | Q5B |
| F | D6 | DNU | GND | GND | Q6A | Q6B |
| G | PAR_IN | \overline{RESET} | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | \overline{DCS} | GND | GND | \overline{QCSA} | \overline{QCSB} |
| J | \overline{CK} | \overline{CSR} | V _{DD} | V _{DD} | n.c. | n.c. |
| K | D8 | DNU | GND | GND | Q8A | Q8B |
| L | D9 | DNU | V _{DD} | V _{DD} | Q9A | Q9B |
| M | D10 | DNU | GND | GND | Q10A | Q10B |
| N | DODT | DNU | V _{DD} | V _{DD} | QODTA | QODTB |
| P | D12 | DNU | GND | GND | Q12A | Q12B |
| R | D13 | DNU | V _{DD} | V _{DD} | Q13A | Q13B |
| T | DCKE | DNU | VREF | V _{DD} | QCKEA | QCKEB |

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Fig 6. Ball mapping, 1 : 2 Register B (C0 = 1, C1 = 1)

6.2 Pin description

Table 2: Pin description

| Symbol | Pin | Type | Description |
|--|---|--------------------------|--|
| GND | B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4 | ground input | ground |
| V _{DD} | A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4 | 1.8 V nominal | power supply voltage |
| VREF | A3, T3 | 0.9 V nominal | input reference voltage |
| CK | H1 | Differential input | positive master clock input |
| $\overline{\text{CK}}$ | J1 | Differential input | negative master clock input |
| C0 | G6 | LVC MOS inputs | Configuration control inputs; Register A or Register B and 1 : 1 mode or 1 : 2 mode select. |
| C1 | G5 | | |
| $\overline{\text{RESET}}$ | G2 | LVC MOS input | Asynchronous reset input (active LOW). Resets registers and disables VREF data and clock. |
| $\overline{\text{CSR}}$ | J2 | SSTL ₁₈ input | Chip select inputs (active LOW). Disables D1 to D25 [2] outputs switching when both inputs are HIGH. |
| $\overline{\text{DCS}}$ | H2 | | |
| D1 to D25 | [1] | SSTL ₁₈ input | Data input. Clocked in on the crossing of the rising edge of CK and the falling edge of CK. |
| DODT | [1] | SSTL ₁₈ input | The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control. |
| DCKE | [1] | SSTL ₁₈ input | The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control. |
| PAR_IN | G1 | SSTL ₁₈ input | Parity input. Arrives one clock cycle after the corresponding data input. |
| Q1 to Q25, Q2A to Q14A, Q1B to Q14B | [1] | 1.8 V CMOS outputs | Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control [3] . |
| PPO | A2 | 1.8 V CMOS output | Partial parity out. Indicates odd parity of inputs D1 to D25 [2] . |
| $\overline{\text{QCS}}$, $\overline{\text{QCSA}}$, $\overline{\text{QCSB}}$ | [1] | 1.8 V CMOS output | Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control. |
| QODT, QODTA, QODTB | [1] | 1.8 V CMOS output | Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control. |
| QCKE, QCKEA, QCKEB | [1] | 1.8 V CMOS output | Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control. |

Table 2: Pin description ...continued

| Symbol | Pin | Type | Description |
|-------------------|-----|-------------------|--|
| \overline{QERR} | D2 | open-drain output | Output error bit (active LOW). Generated one clock cycle after the corresponding data output |
| n.c. | [1] | - | Not connected. Ball present but no internal connection to the die. |
| DNU | [1] | - | Do not use. Inputs are in standby-equivalent mode and outputs are driven LOW. |

[1] Depends on configuration. See [Figure 4](#), [Figure 5](#), and [Figure 6](#) for ball number.

[2] Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[3] Data outputs = Q2, Q3, Q5, Q6, Q8 to Q25 when C0 = 0 and C1 = 0.
Data outputs = Q2, Q3, Q5, Q6, Q8 to Q14 when C0 = 0 and C1 = 1.
Data outputs = Q1 to Q6, Q8 to Q10, Q12, Q13 when C0 = 1 and C1 = 1.

7. Functional description

The SSTUH32866 is a 25-bit 1 : 1 or 14-bit 1 : 2 configurable registered buffer with parity, designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control and reset (\overline{RESET}) inputs are LVCMOS. All data outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load, and meet SSTL_18 specifications. The error (\overline{QERR}) output is 1.8 V open-drain driver.

The SSTUH32866 operates from a differential clock (CK and \overline{CK}). Data are registered at the crossing of CK going HIGH, and CK going LOW.

The C0 input controls the pinout configuration for the 1 : 2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1 : 1 (when LOW) to 14-bit 1 : 2 (when HIGH).

The SSTUH32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain \overline{QERR} pin (active LOW). The convention is even parity, that is, valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

When used as a single device, the C0 and C1 inputs are tied LOW. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. The partial-parity-out (PPO) and \overline{QERR} signals are produced three cycles after the corresponding data inputs.

When used in pairs, the C0 input of the first register is tied LOW and the C0 input of the second register is tied HIGH. The C1 input of both registers are tied HIGH. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the first device. The PPO and \overline{QERR} signals are produced on the second device three clock cycles after the corresponding data inputs. The PPO output of the first register is

cascaded to the PAR_IN of the second register. The \overline{QERR} output of the first register is left floating and the valid error information is latched on the \overline{QERR} output of the second register.

If an error occurs and the \overline{QERR} output is driven LOW, it stays latched LOW for two clock cycles or until \overline{RESET} is driven LOW. The DIMM-dependent signals (DCKE, \overline{DCS} , DODT, and \overline{CSR}) are not included in the parity check computation.

The device supports low-power standby operation. When \overline{RESET} is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when \overline{RESET} is LOW all registers are reset, and all outputs are forced LOW. The LVC MOS \overline{RESET} input must always be held at a valid logic HIGH or LOW level.

The device also supports low-power active operation by monitoring both system chip select (\overline{DCS} and \overline{CSR}) inputs and will gate the Qn and PPO outputs from changing states when both \overline{DCS} and \overline{CSR} inputs are HIGH. If either \overline{DCS} or \overline{CSR} input is LOW, the Qn and PPO outputs will function normally. The \overline{RESET} input has priority over the \overline{DCS} and \overline{CSR} control and when driven LOW will force the Qn and PPO outputs LOW, and the \overline{QERR} output HIGH. If the \overline{DCS} control functionality is not desired, then the \overline{CSR} input can be hard-wired to ground, in which case, the setup time requirement for \overline{DCS} would be the same as for the other Dn data inputs. To control the low-power mode with \overline{DCS} only, then the \overline{CSR} input should be pulled up to V_{DD} through a pull-up resistor.

To ensure defined outputs from the register before a stable clock has been supplied, \overline{RESET} must be held in the LOW state during power-up.

In the DDR2 RDIMM application, \overline{RESET} is specified to be completely asynchronous with respect to CK and \overline{CK} . Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the Qn outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of \overline{RESET} until the input receivers are fully enabled, the design of the SSTUH32866 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

7.1 Function table

Table 3: Function table (each flip-flop)

L = LOW voltage level; H = HIGH voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition

| Inputs | | | | | | Outputs [1] | | |
|--------|---------------|---------------|---------------|---------------|------------------|----------------|----------------|----------------|
| RESET | DCS | CSR | CK | CK̄ | Dn, DODTn, DCKEn | Qn | QCS | QODT, QCKE |
| H | L | L | ↑ | ↓ | L | L | L | L |
| H | L | L | ↑ | ↓ | H | H | L | H |
| H | L | L | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | L | H | ↑ | ↓ | L | L | L | L |
| H | L | H | ↑ | ↓ | H | H | L | H |
| H | L | H | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | H | L | ↑ | ↓ | L | L | H | L |
| H | H | L | ↑ | ↓ | H | H | H | H |
| H | H | L | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | H | H | ↑ | ↓ | L | Q ₀ | H | L |
| H | H | H | ↑ | ↓ | H | Q ₀ | H | H |
| H | H | H | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| L | X or floating | X or floating | X or floating | X or floating | X or floating | L | L | L |

[1] Q₀ is the previous state of the associated output.

Table 4: Parity and standby function table

L = LOW voltage level; H = HIGH voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition

| Inputs | | | | | | | Outputs [1] | |
|--------|---------------|---------------|---------------|---------------|-----------------------------|---------------|------------------|-------------------|
| RESET | DCS | CSR | CK | CK̄ | Σ of inputs = H (D1 to D25) | PAR_IN [2] | PPO [3] | QERR [4] |
| H | L | X | ↑ | ↓ | even | L | L | H |
| H | L | X | ↑ | ↓ | odd | L | H | L |
| H | L | X | ↑ | ↓ | even | H | H | L |
| H | L | X | ↑ | ↓ | odd | H | L | H |
| H | H | L | ↑ | ↓ | even | L | L | H |
| H | H | L | ↑ | ↓ | odd | L | H | L |
| H | H | L | ↑ | ↓ | even | H | H | L |
| H | H | L | ↑ | ↓ | odd | H | L | H |
| H | H | H | ↑ | ↓ | X | X | PPO ₀ | QERR ₀ |
| H | X | X | L or H | L or H | X | X | PPO ₀ | QERR ₀ |
| L | X or floating | X or floating | X or floating | X or floating | X or floating | X or floating | L | H |

[1] PPO₀ is the previous state of output PPO; QERR₀ is the previous state of output QERR.

[2] Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[3] PAR_IN arrives one clock cycle (C0 = 0), or two clock cycles (C0 = 1), after the data to which it applies.

[4] This condition assumes QERR is HIGH at the crossing of CK going HIGH and CK̄ going LOW. If QERR is LOW, it stays latched LOW for two clock cycles or until RESET is driven LOW.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---|---|----------|--------------------|------|
| V_{DD} | supply voltage | | -0.5 | +2.5 | V |
| V_I | receiver input voltage | | -0.5 [1] | +2.5 [2] | V |
| V_O | driver output voltage | | -0.5 [1] | $V_{DD} + 0.5$ [2] | V |
| I_{IK} | input clamp current | $V_I < 0\text{ V}$ or $V_I > V_{DD}$ | - | -50 | mA |
| I_{OK} | output clamp current | $V_O < 0\text{ V}$ or $V_O > V_{DD}$ | - | ± 50 | mA |
| I_O | continuous output current | $0\text{ V} < V_O < V_{DD}$ | - | ± 50 | mA |
| I_{CCC} | continuous current through each V_{DD} or GND pin | | - | ± 100 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| V_{esd} | electrostatic discharge voltage | Human Body Model (HBM); 1.5 k Ω ; 100 pF | 2 | - | kV |
| | | Machine Model (MM); 0 Ω ; 200 pF | 200 | - | V |

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

[2] This value is limited to 2.5 V maximum.

9. Recommended operating conditions

Table 6: Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---------------------------------|---|--------------------------|----------------------|----------------------|------|
| V_{DD} | supply voltage | | 1.7 | - | 1.9 | V |
| V_{ref} | reference voltage | | $0.49 \times V_{DD}$ | $0.50 \times V_{DD}$ | $0.51 \times V_{DD}$ | V |
| V_{TT} | termination voltage | | $V_{ref} - 0.040$ | V_{ref} | $V_{ref} + 0.040$ | V |
| V_I | input voltage | | 0 | - | V_{DD} | V |
| $V_{IH(AC)}$ | AC HIGH-level input voltage | data (Dn), \overline{CSR} , and PAR_IN inputs | $V_{ref} + 0.250$ | - | - | V |
| $V_{IL(AC)}$ | AC LOW-level input voltage | data (Dn), \overline{CSR} , and PAR_IN inputs | - | - | $V_{ref} - 0.250$ | V |
| $V_{IH(DC)}$ | DC HIGH-level input voltage | data (Dn), \overline{CSR} , and PAR_IN inputs | $V_{ref} + 0.125$ | - | - | V |
| $V_{IL(DC)}$ | DC LOW-level input voltage | data (Dn), \overline{CSR} , and PAR_IN inputs | - | - | $V_{ref} - 0.125$ | V |
| V_{IH} | HIGH-level input voltage | \overline{RESET} , Cn | [1] $0.65 \times V_{DD}$ | - | - | V |
| V_{IL} | LOW-level input voltage | \overline{RESET} , Cn | [1] - | - | $0.35 \times V_{DD}$ | V |
| V_{ICR} | common mode input voltage range | CK, \overline{CK} | [2] 0.675 | - | 1.125 | V |
| V_{ID} | differential input voltage | CK, \overline{CK} | [2] 600 | - | - | mV |

Table 6: Recommended operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------------|-----------------------|-----|-----|-----|------|
| I_{OH} | HIGH-level output current | | - | - | -12 | mA |
| I_{OL} | LOW-level output current | | - | - | 12 | mA |
| T_{amb} | ambient temperature | operating in free air | 0 | - | +70 | °C |

[1] The \overline{RESET} and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation.

[2] The differential inputs must not be floating, unless \overline{RESET} is LOW.

10. Characteristics

Table 7: Characteristics

At recommended operating conditions (see Table 6), unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--|---|-----|-----|---------|---------|
| V_{OH} | HIGH-level output voltage | $I_{OH} = -12$ mA; $V_{DD} = 1.7$ V | 1.2 | - | - | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 12$ mA; $V_{DD} = 1.7$ V | - | - | 0.5 | V |
| I_I | input current | all inputs; $V_I = V_{DD}$ or GND; $V_{DD} = 1.9$ V | - | - | ± 5 | μ A |
| I_{DD} | static standby current | $\overline{RESET} = GND$; $I_O = 0$ mA; $V_{DD} = 1.9$ V | - | - | 100 | μ A |
| | static operating current | $\overline{RESET} = V_{DD}$; $I_O = 0$ mA; $V_{DD} = 1.9$ V; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ | - | - | 40 | mA |
| I_{DDD} | dynamic operating current per MHz, clock only | $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and \overline{CK} switching at 50 % duty cycle. $I_O = 0$ mA; $V_{DD} = 1.8$ V | - | 16 | - | μ A |
| | dynamic operating current per MHz, per each data input, 1 : 1 mode | $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and \overline{CK} switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. $I_O = 0$ mA; $V_{DD} = 1.8$ V | - | 11 | - | μ A |
| | dynamic operating current per MHz, per each data input, 1 : 2 mode | $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and \overline{CK} switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. $I_O = 0$ mA; $V_{DD} = 1.8$ V | - | 19 | - | μ A |
| C_i | input capacitance, data and \overline{CSR} inputs | $V_I = V_{ref} \pm 250$ mV; $V_{DD} = 1.8$ V | 2.5 | - | 3.5 | pF |
| | input capacitance, CK and \overline{CK} inputs | $V_{ICR} = 0.9$ V; $V_{i(p-p)} = 600$ mV; $V_{DD} = 1.8$ V | 2 | - | 3 | pF |
| | input capacitance, \overline{RESET} input | $V_I = V_{DD}$ or GND; $V_{DD} = 1.8$ V | 3 | - | 4 | pF |

Table 8: Timing requirementsAt recommended operating conditions (see [Table 6](#)), unless otherwise specified. See [Figure 2](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--|--|--------|-----|-----|------|
| f_{clock} | clock frequency | | - | - | 450 | MHz |
| t_{W} | pulse duration, CK, $\overline{\text{CK}}$ HIGH or LOW | | 1 | - | - | ns |
| t_{ACT} | differential inputs active time | | [1][2] | - | 10 | ns |
| t_{INACT} | differential inputs inactive time | | [1][3] | - | 15 | ns |
| t_{su} | setup time | DCS before CK \uparrow , $\overline{\text{CK}}$ \downarrow , CSR HIGH; CSR before CK \uparrow , $\overline{\text{CK}}$ \downarrow , DCS HIGH | 0.7 | - | - | ns |
| | | $\overline{\text{DCS}}$ before CK \uparrow , $\overline{\text{CK}}$ \downarrow , $\overline{\text{CSR}}$ LOW | 0.5 | - | - | ns |
| | | DODT, DCKE and data (Dn) before CK \uparrow , $\overline{\text{CK}}$ \downarrow | 0.5 | - | - | ns |
| | | PAR_IN before CK \uparrow , $\overline{\text{CK}}$ \downarrow | 0.5 | - | - | ns |
| t_{h} | hold time | DCS, DODT, DCKE and data (Dn) after CK \uparrow , $\overline{\text{CK}}$ \downarrow | 0.5 | - | - | ns |
| | | PAR_IN after CK \uparrow , $\overline{\text{CK}}$ \downarrow | 0.5 | - | - | ns |

[1] This parameter is not necessarily production tested.

[2] VREF must be held at a valid input voltage level and data inputs must be held LOW for a minimum time of $t_{\text{ACT(max)}}$ after RESET is taken HIGH.[3] VREF, data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{\text{INACT(max)}}$ after RESET is taken LOW.**Table 9: Switching characteristics**At recommended operating conditions (see [Table 6](#)), unless otherwise specified. See [Section 11.1](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|--|--------|------|-----|--------|
| f_{MAX} | maximum input clock frequency | | 450 | - | - | MHz |
| t_{PDM} | propagation delay, single bit switching | from CK \uparrow and $\overline{\text{CK}}$ \downarrow to Qn | [1] | 1.41 | - | 1.8 ns |
| t_{PD} | propagation delay | from CK \uparrow and $\overline{\text{CK}}$ \downarrow to PPO | | 0.5 | - | 1.8 ns |
| t_{LH} | LOW-to-HIGH propagation delay | from CK \uparrow and $\overline{\text{CK}}$ \downarrow to $\overline{\text{QERR}}$ | | 1.2 | - | 3 ns |
| t_{HL} | HIGH-to-LOW propagation delay | from CK \uparrow and $\overline{\text{CK}}$ \downarrow to $\overline{\text{QERR}}$ | | 1 | - | 2.4 ns |
| t_{PDMSS} | propagation delay, simultaneous switching | from CK \uparrow and $\overline{\text{CK}}$ \downarrow to Qn | [1][2] | - | - | 2.0 ns |
| t_{PHL} | HIGH-to-LOW propagation delay | from RESET \downarrow to Qn \downarrow | - | - | 3 | ns |
| | | from RESET \downarrow to PPO \downarrow | - | - | 3 | ns |
| t_{PLH} | LOW-to-HIGH propagation delay | from RESET \downarrow to $\overline{\text{QERR}}$ \uparrow | - | - | 3 | ns |

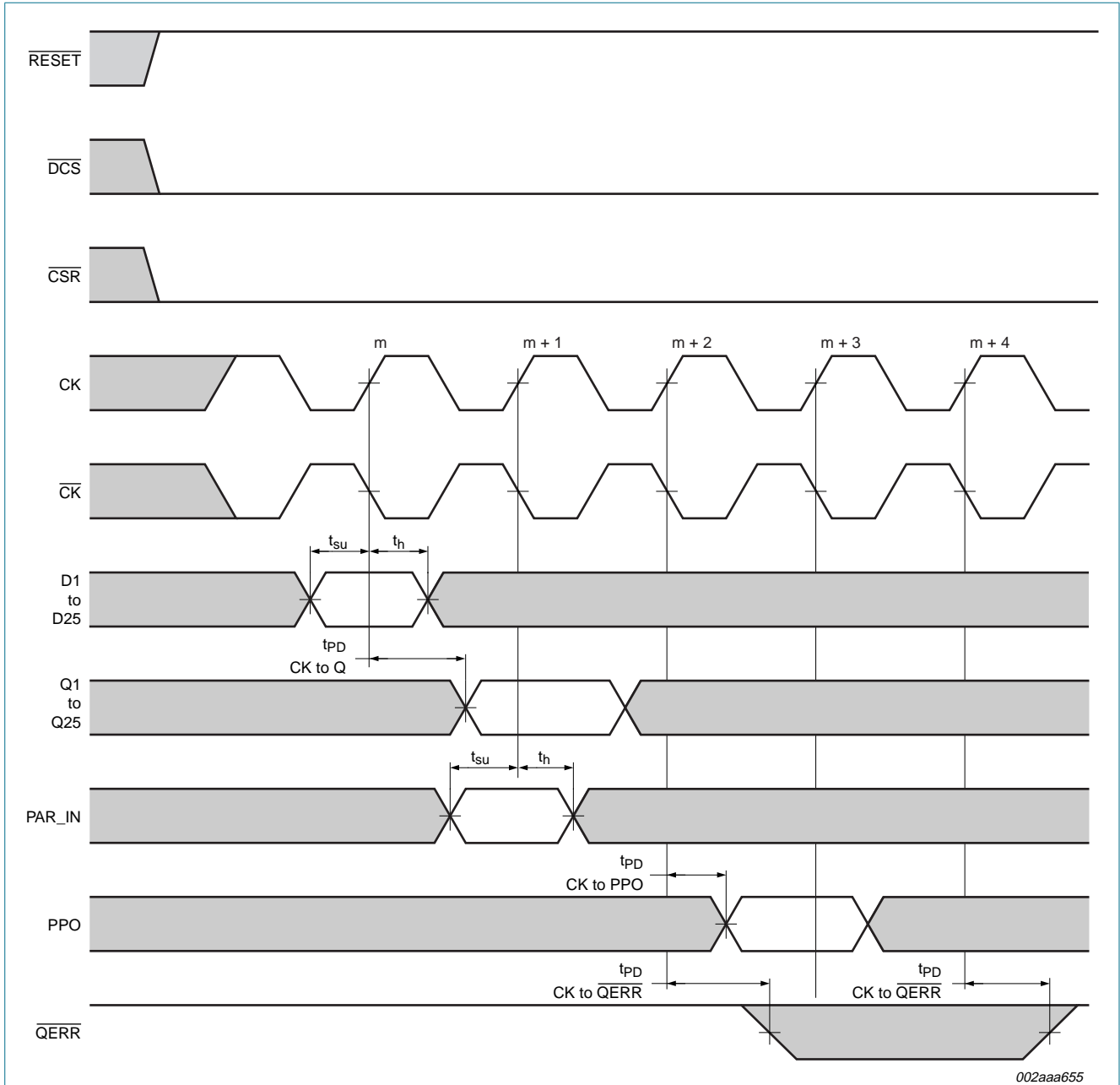
[1] Includes 350 ps of test-load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 10: Data output edge ratesAt recommended operating conditions (see [Table 6](#)), unless otherwise specified. See [Section 11.2](#).

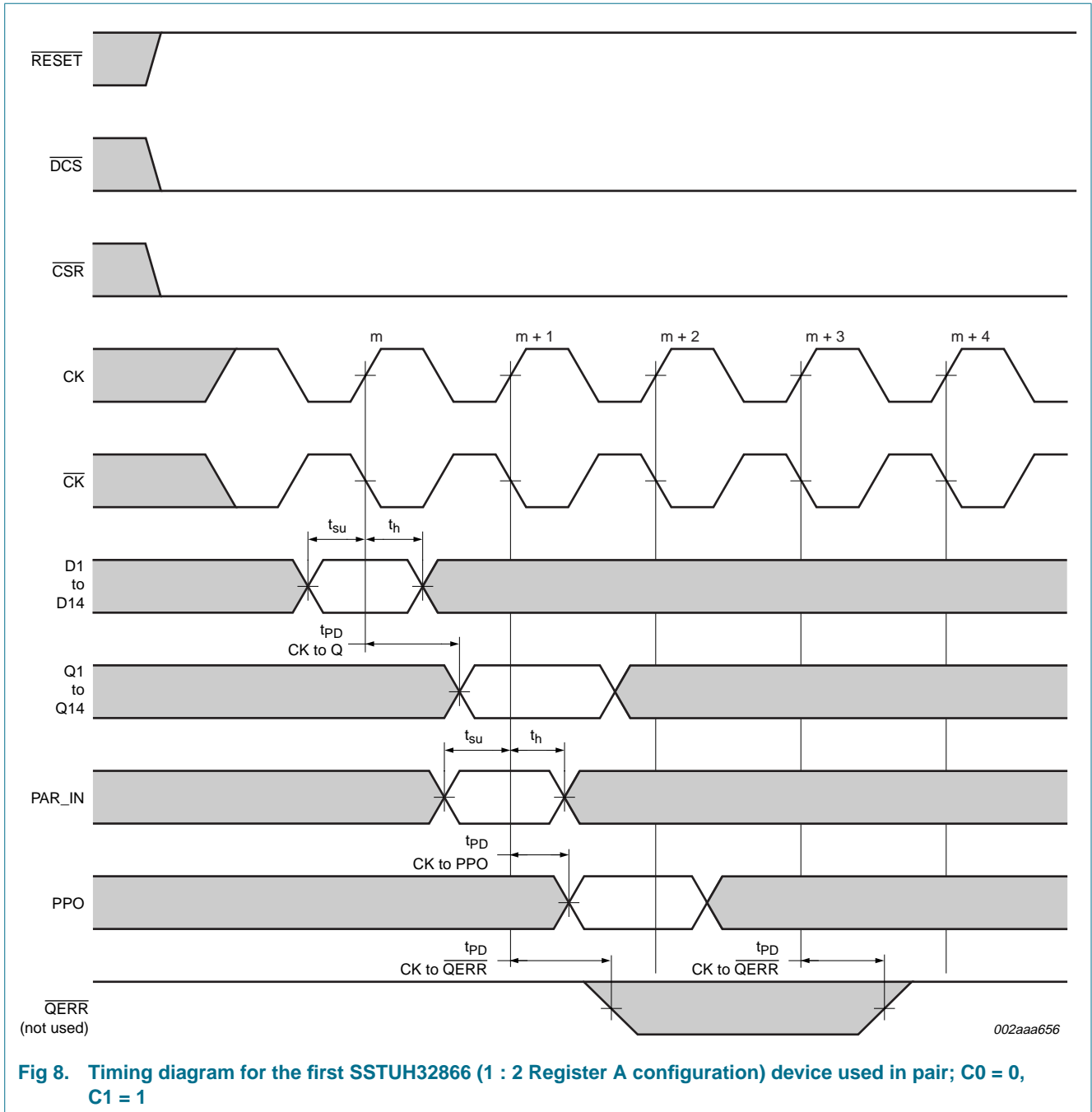
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|-----------------------------------|-----|-----|-----|------|
| dV/dt_{r} | rising edge slew rate | from 20 % to 80 % | 1 | - | 4 | V/ns |
| dV/dt_{f} | falling edge slew rate | from 80 % to 20 % | 1 | - | 4 | V/ns |
| dV/dt_{Δ} | absolute difference between dV/dt_{r} and dV/dt_{f} | from 20 % or 80 % to 80 % or 20 % | - | - | 1 | V/ns |

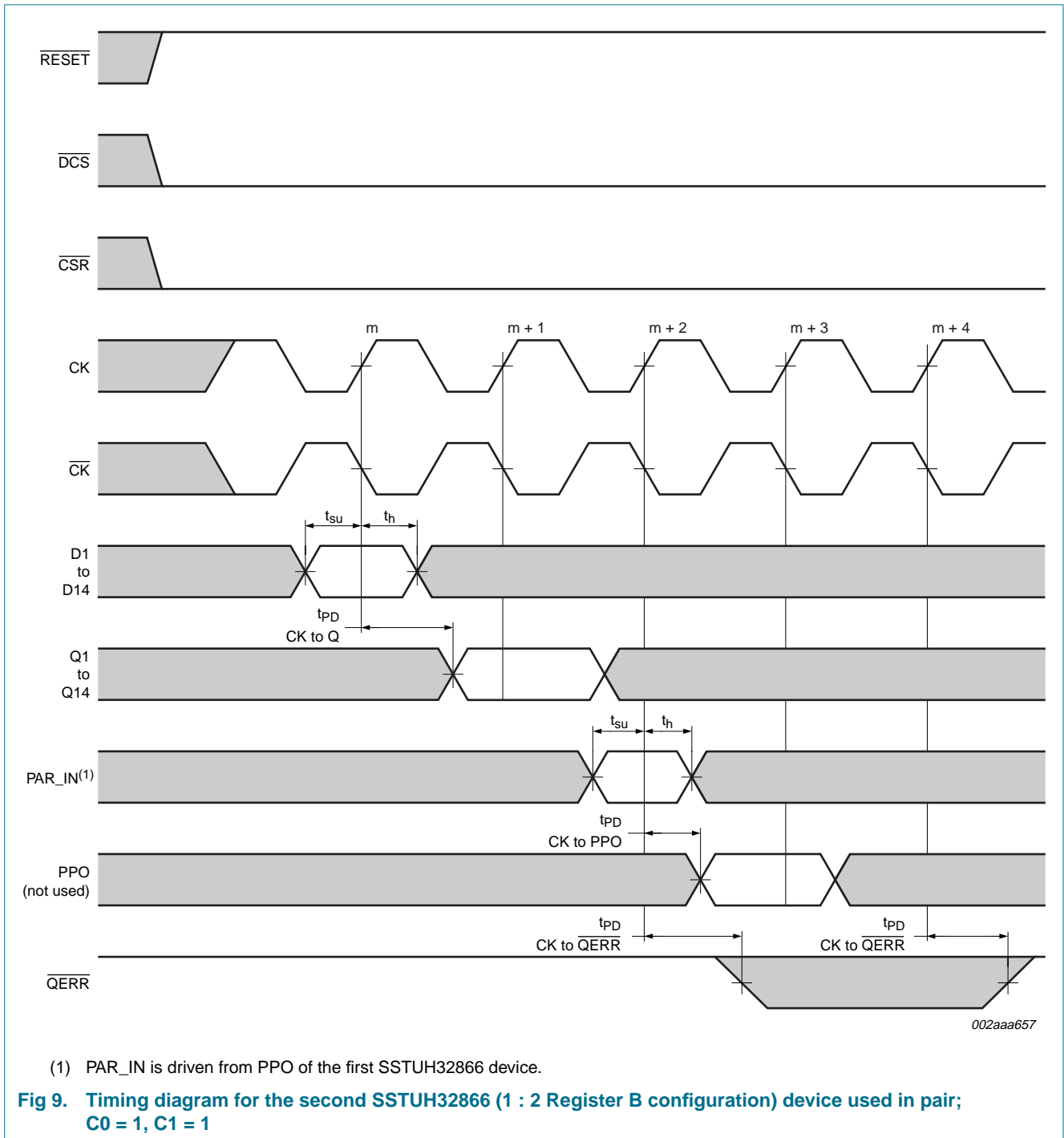
10.1 Timing diagrams



002aaa655

Fig 7. Timing diagram for SSTUH32866 used as a single device; C0 = 0, C1 = 0





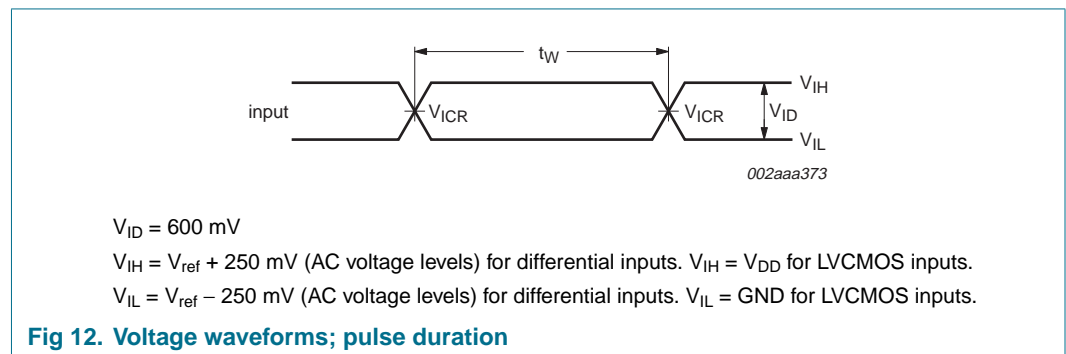
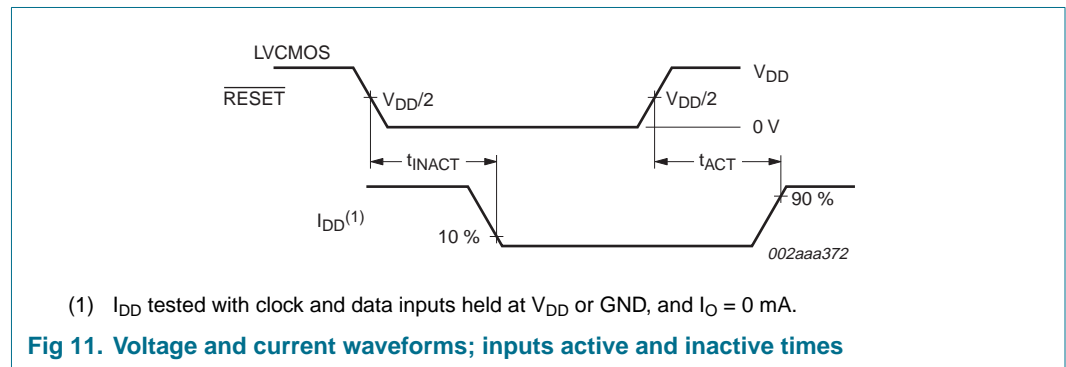
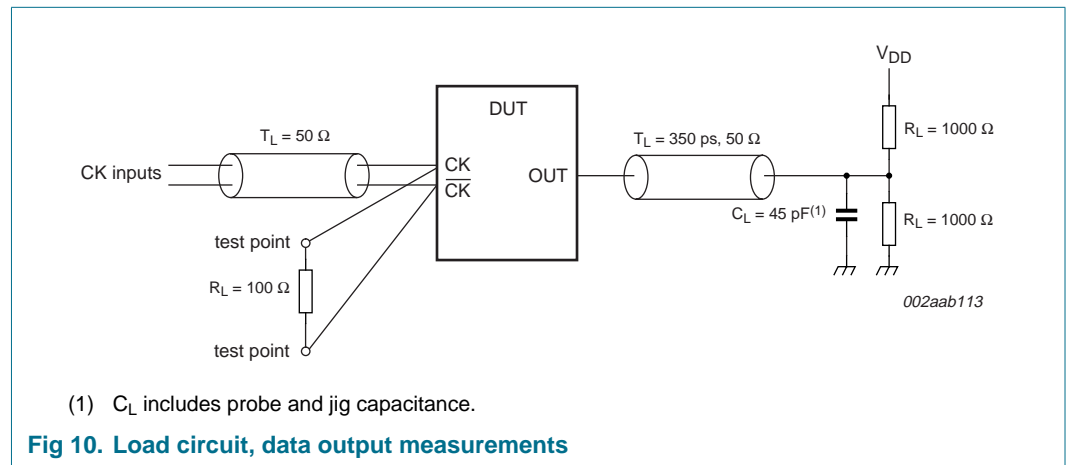
11. Test information

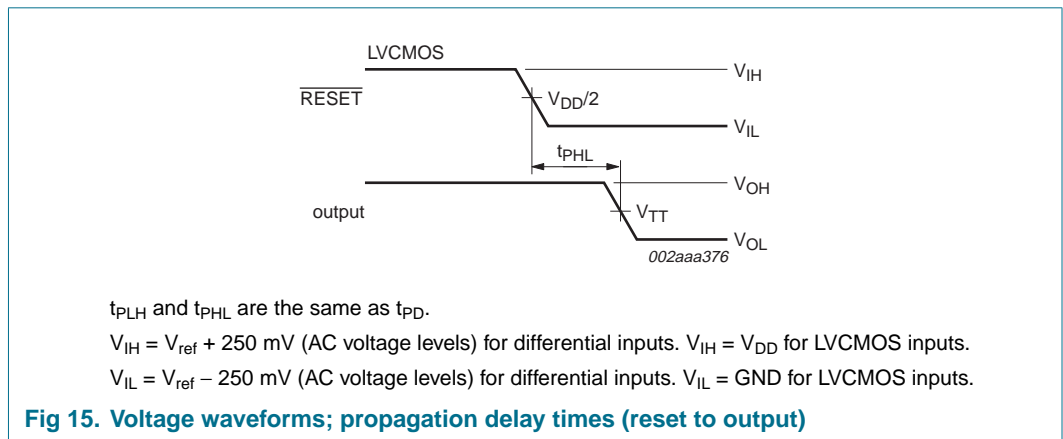
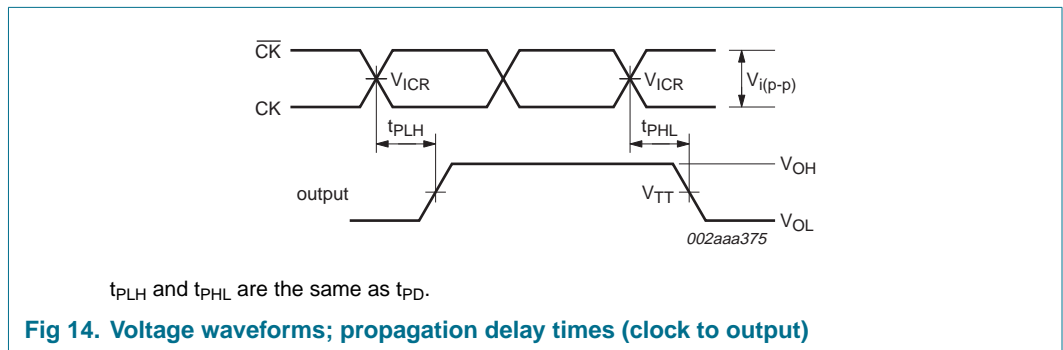
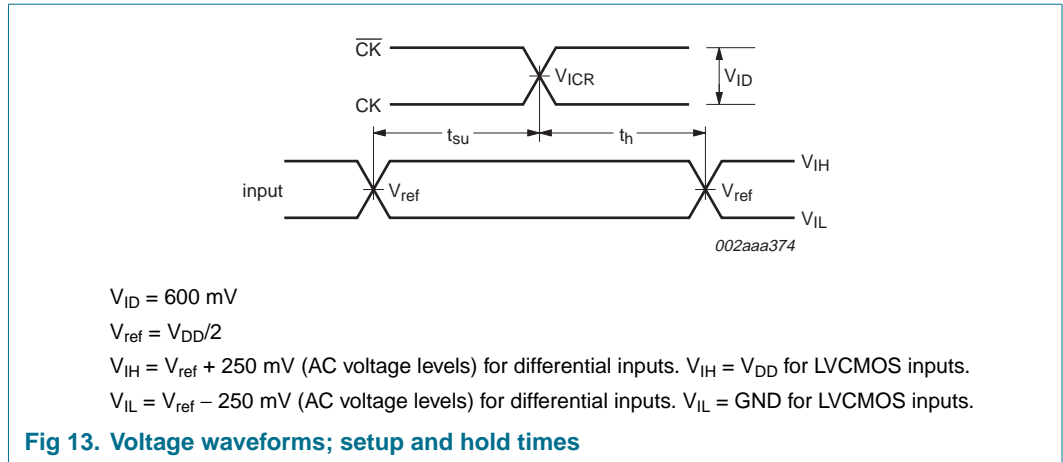
11.1 Parameter measurement information for data output load circuit

$V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$.

All input pulses are supplied by generators having the following characteristics:
 PRR $\leq 10 \text{ MHz}$; $Z_0 = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20 \%$, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

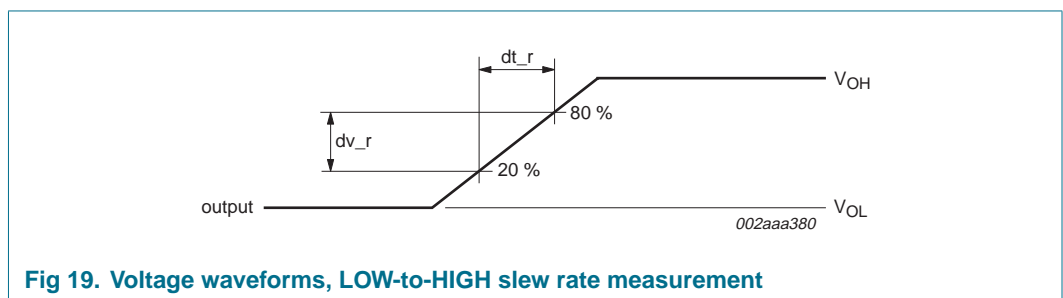
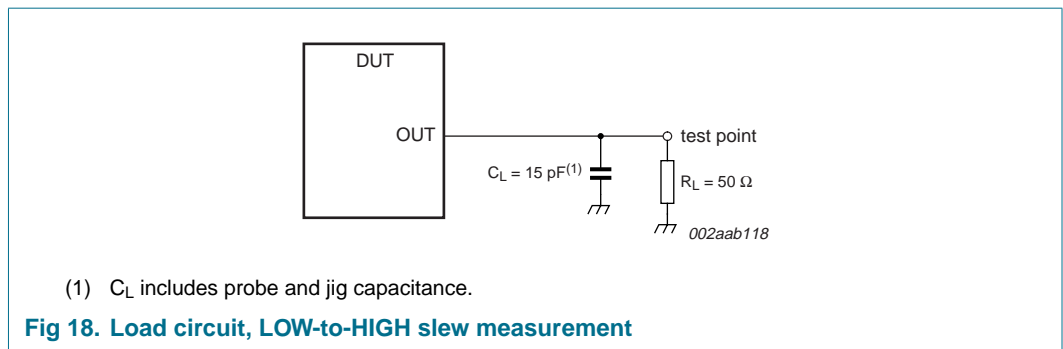
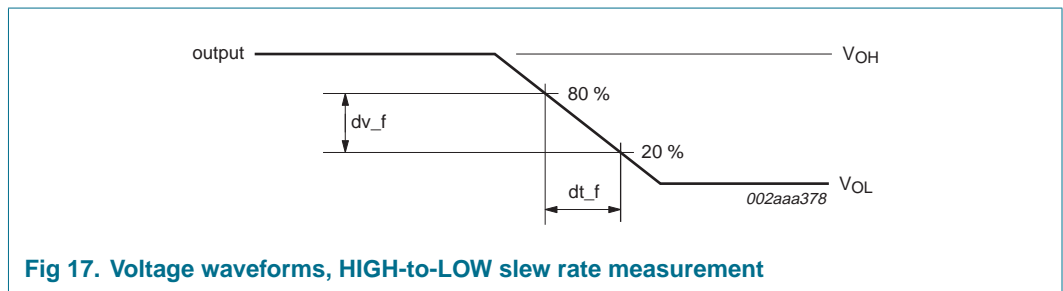
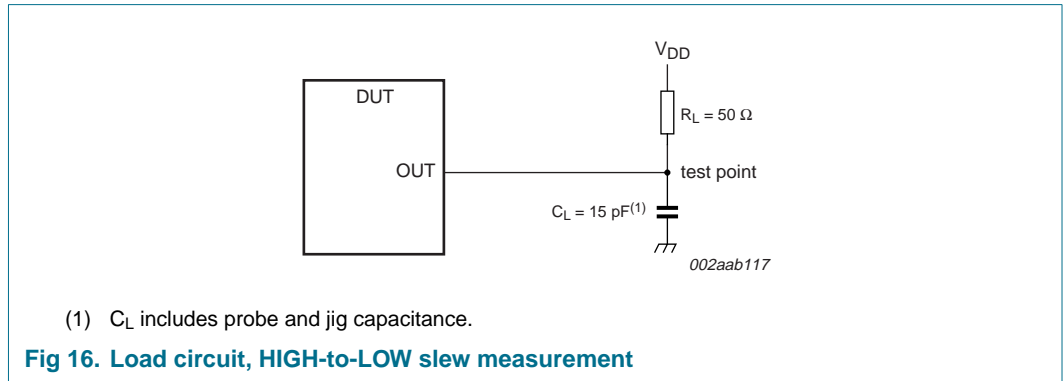




11.2 Data output slew rate measurement information

$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$.

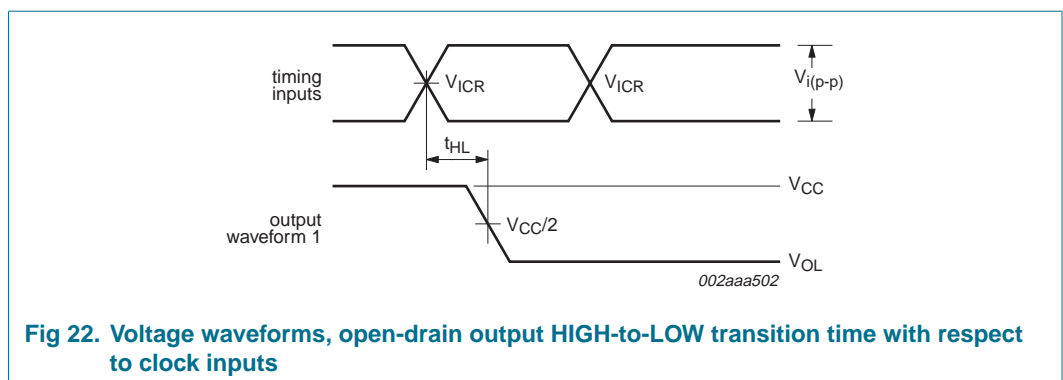
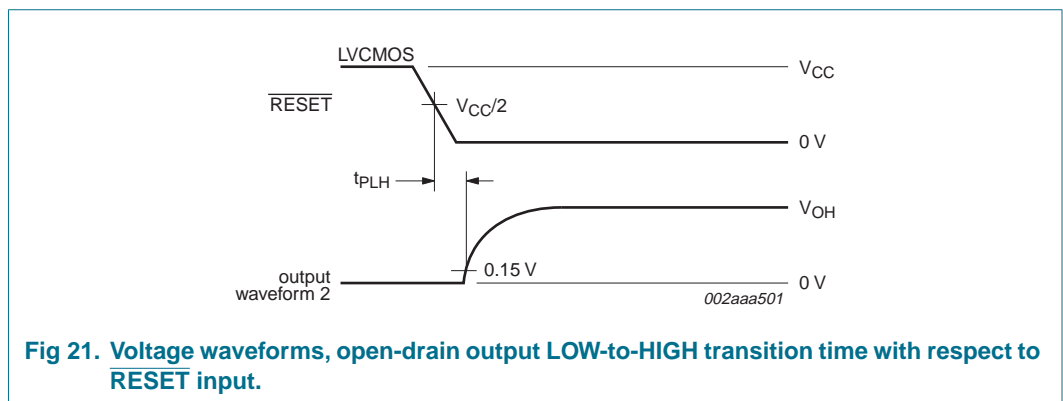
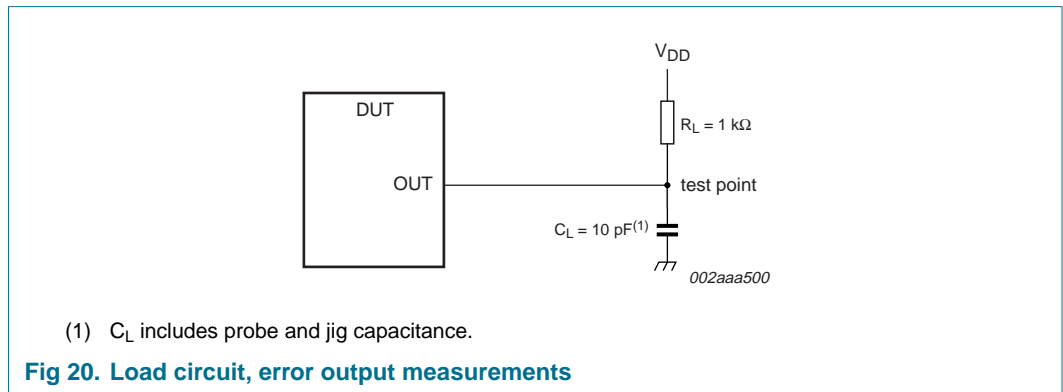
All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10\text{ MHz}$; $Z_0 = 50\ \Omega$; input slew rate = $1\text{ V/ns} \pm 20\%$, unless otherwise specified.



11.3 Error output load circuit and voltage measurement information

$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$.

All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10\text{ MHz}$; $Z_0 = 50\ \Omega$; input slew rate = $1\text{ V/ns} \pm 20\%$, unless otherwise specified.



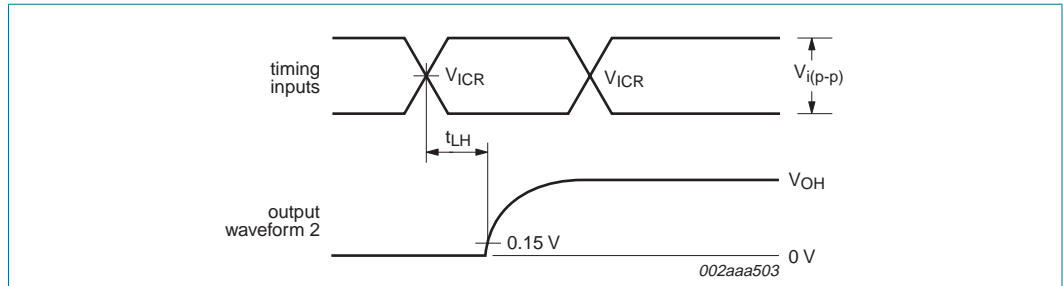


Fig 23. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs

11.4 Partial parity out load circuit and voltage measurement information

$V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$.

All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10 \text{ MHz}$; $Z_0 = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20 \%$, unless otherwise specified.

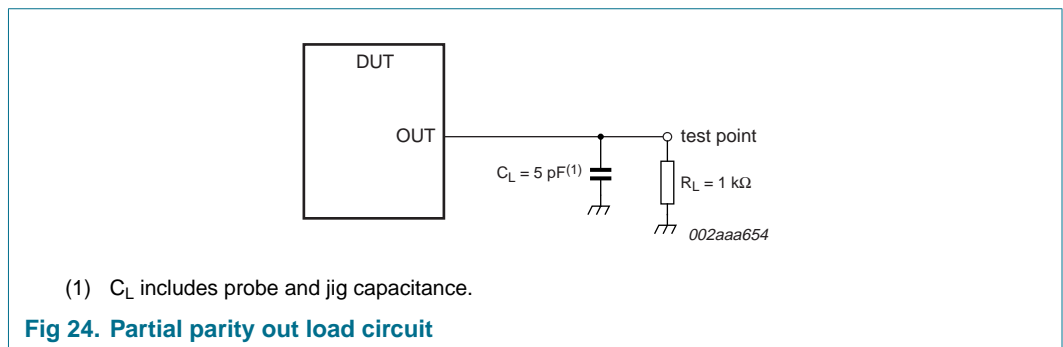


Fig 24. Partial parity out load circuit

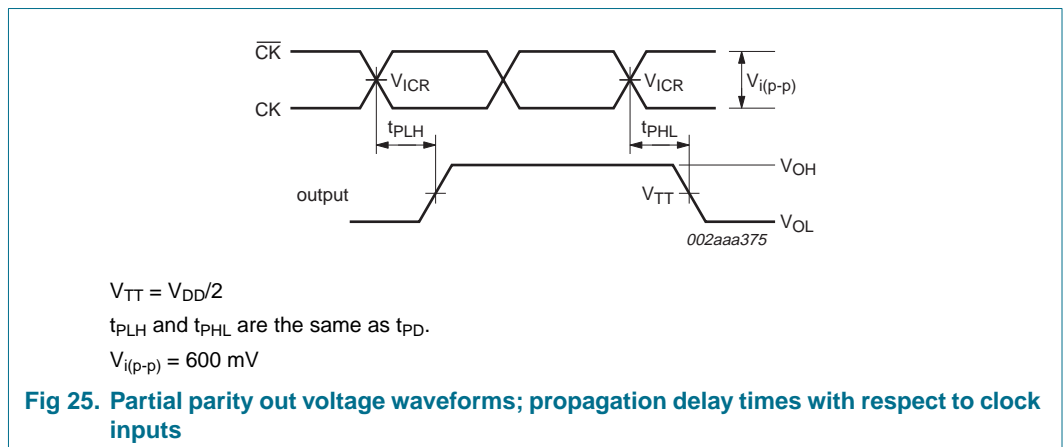
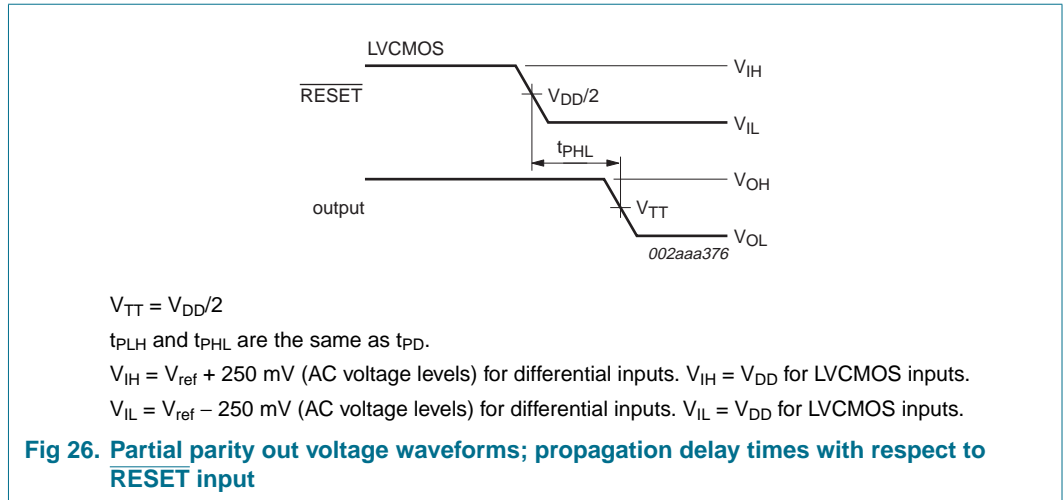


Fig 25. Partial parity out voltage waveforms; propagation delay times with respect to clock inputs



12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

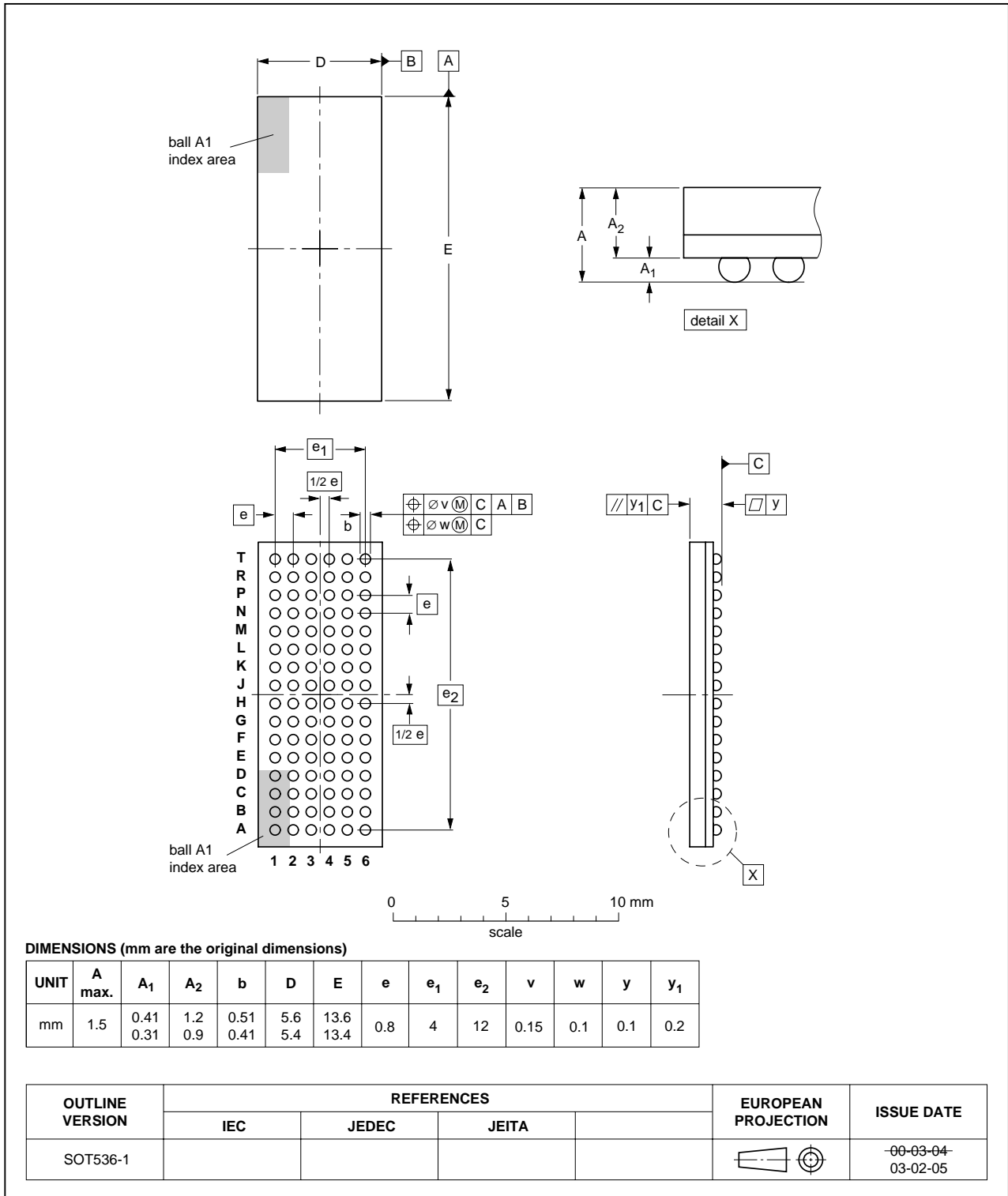


Fig 27. Package outline SOT536-1 (LFBGA96)

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 11: Suitability of surface mount IC packages for wave and reflow soldering methods

| Package [1] | Soldering method | |
|--|-------------------------|--------------|
| | Wave | Reflow [2] |
| BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable [4] | suitable |
| PLCC [5], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended [5] [6] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended [7] | suitable |
| CWQCCN..L [8], PMFP [9], WQCCN..L [8] | not suitable | not suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 12: Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Silicon |
| DDR | Double Data Rate |
| DIMM | Dual In-line Memory Module |
| DRAM | Dynamic Random Access Memory |
| JEDEC | Joint Electron Device Engineering Council |
| LFPGA | Low profile Fine-pitch Ball Grid Array |
| LVCMOS | Low Voltage Complementary Metal Oxide Silicon |
| PPO | Partial Parity Out |
| PRR | Pulse Repetition Rate |
| RDIMM | Registered Dual In-line Memory Module |
| SSTL | Stub Series Terminated Logic |

15. Revision history

Table 13: Revision history

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|--------------|--------------|--------------------|---------------|----------------|------------|
| SSTUH32866_1 | 20050513 | Product data sheet | - | 9397 750 14199 | - |

16. Data sheet status

| Level | Data sheet status ^[1] | Product status ^[2] ^[3] | Definition |
|-------|----------------------------------|--|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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