# SIEMENS

## TV-SAT-PLL with I²C-Bus and Four Chip Addresses

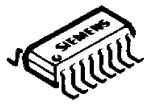
## SDA 6102X

**Preliminary Data**

**Bipolar IC**

### Features

- 1-chip system for MPU control (I²C-bus)
- 4 programmable chip addresses
- Short pull-in time for quick channel switch-over and optimized loop stability
- 5 high-current switch outputs (20 mA)
- Software-compatible with SDA 3302 series
- Oxis III-technology

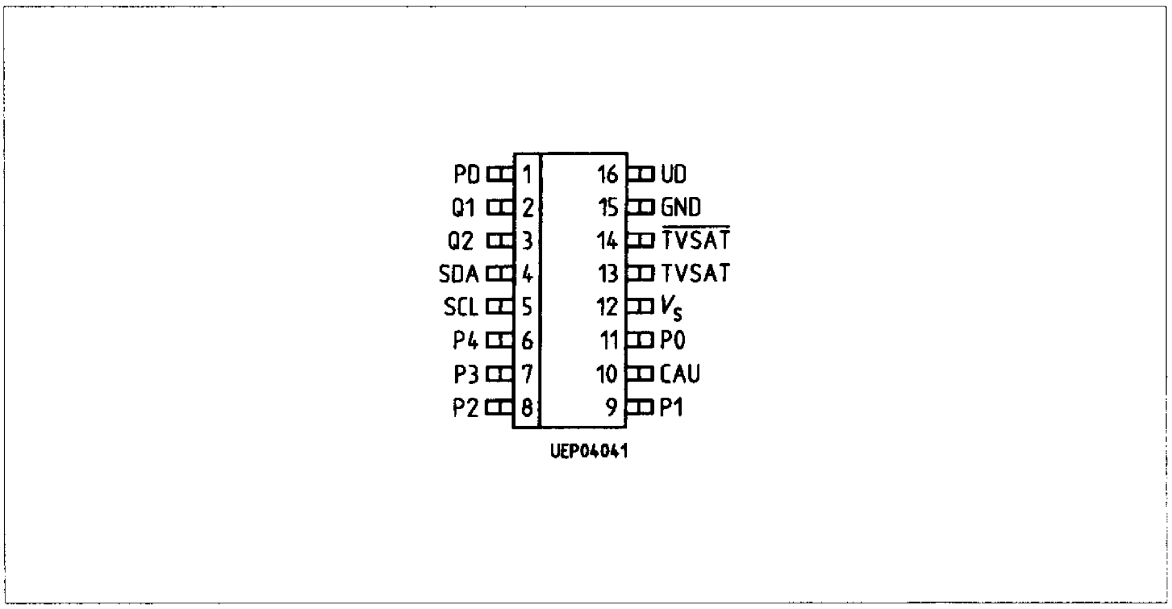


VPS 05119

P-DSO-16

| Type | Ordering Code | Package |
|---|---|---|
| SDA 6102X | Q67000-A5016 | P-DSO-16 (SMD) |

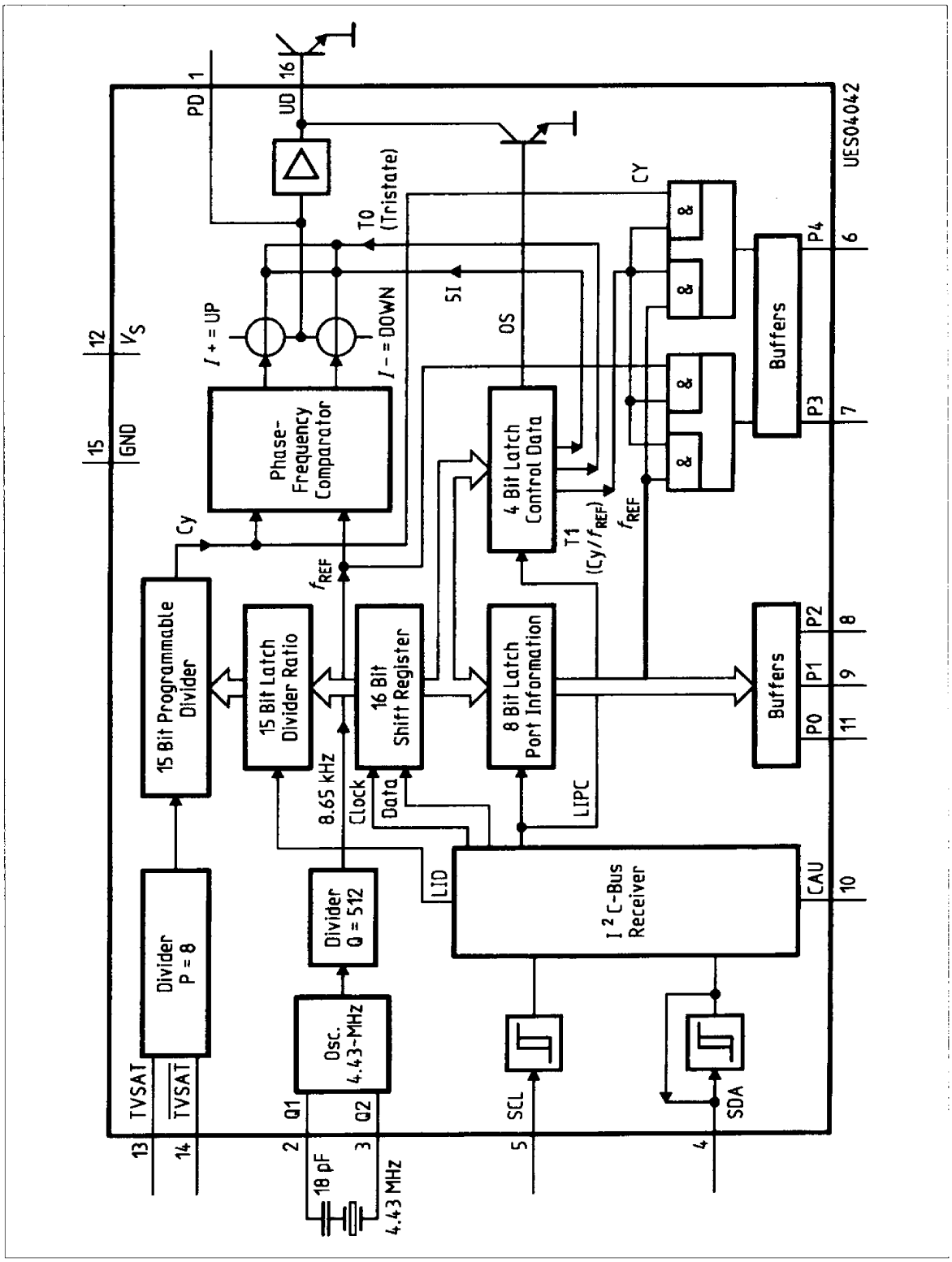
Combined with a VCO (tuner), the SDA 6102X device, with for hard-switched chip addresses, forms a digitally programmable phase-locked loop for use in satellite indoor units. It is compatible with the standard SDA 3202-2 device used in television sets with frequency synthesis tuning. With a 4.43-MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 2.27 GHz in increments of 69.2 kHz. Higher frequencies (up to 2.4 GHz) are possible at the expense of coarser frequency resolution. The tuning process is controlled by a microprocessor via an I²C-bus. The I²C-bus noise immunity has been improved by a factor of 10 compared to the SDA 3302-2, and the new crystal oscillator generates a sinusoidal signal, suppressing the higher-order harmonics, which reduces the moire noise considerably.




**Pin Configuration**
(top view)

**Pin Definitions and Functions**

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | PD | Input active filter / charge pump output |
| 2 | Q1 | Quartz crystal |
| 3 | Q2 | Quartz crystal |
| 4 | SDA | Data input / output for $I^2C$ bus |
| 5 | SCL | Clock input for $I^2C$ bus |
| 6 | P4 | Port output (open collector) |
| 7 | P3 | Port output (open collector) |
| 8 | P2 | Port output (open collector) |
| 9 | P1 | Port output (open collector) |
| 10 | CAU | Address switch input |
| 11 | P0 | Port output (open collector) |
| 12 | $V_S$ | Supply voltage |
| 13 | TVSAT | Non-inverting signal input |
| 14 | $\overline{\text{TVSAT}}$ | Inverting signal input |
| 15 | GND | Ground |
| 16 | UD | Output active filter |




**Block Diagram**

## Circuit Description

### Tuning Section (refer to block diagram)

TVSAT, $\overline{\text{TVSAT}}$ — The tuner signal is capacitively coupled as a differential signal at the TVSAT/$\overline{\text{TVSAT}}$ inputs. Alternatively, the tuner signal is capacitively coupled at the TVSAT-input and the $\overline{\text{TVSAT}}$ input is decoupled to ground using a capacitor of low series inductance.
The signal subsequently passes through an asynchronous divider with a fixed ratio of $P$ = 8, an adjustable divider with ratio $N$ = 256 through 32767, and is then compared in a digital frequency/phase detector to a reference frequency $f_{REF}$ = 8.65 KHz.

Q1, Q2 — This frequency is derived from a balanced, low-impedance 4.43 MHz crystal oscillator (pin Q1, Q2) by dividing its output signal by $Q$ = 512.
The phase detector has two outputs UP and DOWN that drive the two current sources I + and I – of a charge pump. If the negative edge of the divided VCO-signal appears prior to the negative edge of the reference signal, the I + current source pulses for the duration of the phase difference. In the reserve case the I – current source pulses.

PD, UD — If the two signals are in phase, the charge pump output (PD) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external output transistor at UD and external RC-circuity). The charge pump output is also switched into the high-impedance state when the control bit T0 = 1. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of selfdischarge in the peripheral circuity. UD may be switched off by the control bit OS to allow external adjustments.
By means of a control bit 5I the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains in the different TV-bands can be compensated, for example.

P0 ... P4 — The software-switched ports P0 ... P4 are general-purpose 20 mA open-collector outputs and can be used for direct band selection. The test bit T1 = 1 switches the test signals $f_{REF}$ (4.43 MHz/512) and Cy (divided input signal) to P3 and P4 respectively.

CAU — Four different chip addresses can be set by appropriate connection of pin CAU.

### I²C- Bus Interface

Data are exchanged between the processor and the PLL on the I²C-bus.

SCL, SDA — The clock is generated by the processor (input SCL), while pin SDA works as an input or output depending on the direction of the data (open collector; external pull-up resistor).
Both inputs have hysteresis and a low-pass characteristic, which enhances the noise immunity of the I²C-bus.

The data from the processor pass through an I²C-bus control. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are high). Each telegram begins with the start condition and ends with the stop condition. Start condtion: SDA goes low, while SCL remains high.

Stop condition: SDA goes high, while SCL remains high. All further information transfer takes place during SCL = low, and the data is forwarded to the control logic on the positive clock edge.
The table „bit allocation" should be referred to in the following paragraph.
All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA-line to low (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The eighth bit is always low.
In the data portion of the telegram the first bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type or a stop condition has to follow the first byte.

$V_S$, GND When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA-line to low, which would block the bus.

**Circuit Description** (cont'd)

**Bit Allocation**

| | MSB | | | | | | | | A = Acknowledge |
|---|---|---|---|---|---|---|---|---|---|
| Address byte | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 0 | A |
| Prog. divider Byte 1 | 0 | n14 | n13 | n12 | n11 | n10 | n9 | n8 | A |
| Prog. divider Byte 2 | n7 | n6 | n5 | n4 | n3 | n2 | n1 | n0 | A |
| Control info Byte 1 | 1 | 5I | T1 | T0 | 1 | 1 | 1 | OS | A |
| Control info Byte 2 | P4 | P3 | P2 | P1 | X | X | P0 | X | A |

**Divider Ratio**

$N = 16384 \times n14 + 8192 \times n13 + 4096 \times n12 + 2048 \times n11 + 1024 \times n10 + 512 \times n9 + 256 \times n8 + +128 \times n7 + 64 \times n6 + 32 \times n5 + 16 \times n4 + 8 \times n3 + 4 \times n2 + 2 \times n1 + n0$

**Port Switching**

P0 ... P4 = 1 Open-collector output is active.

**Pump Current Programming**

5I = 1 High current

**UD Disable**

OS = 1 UD is disabled

**Test Mode**

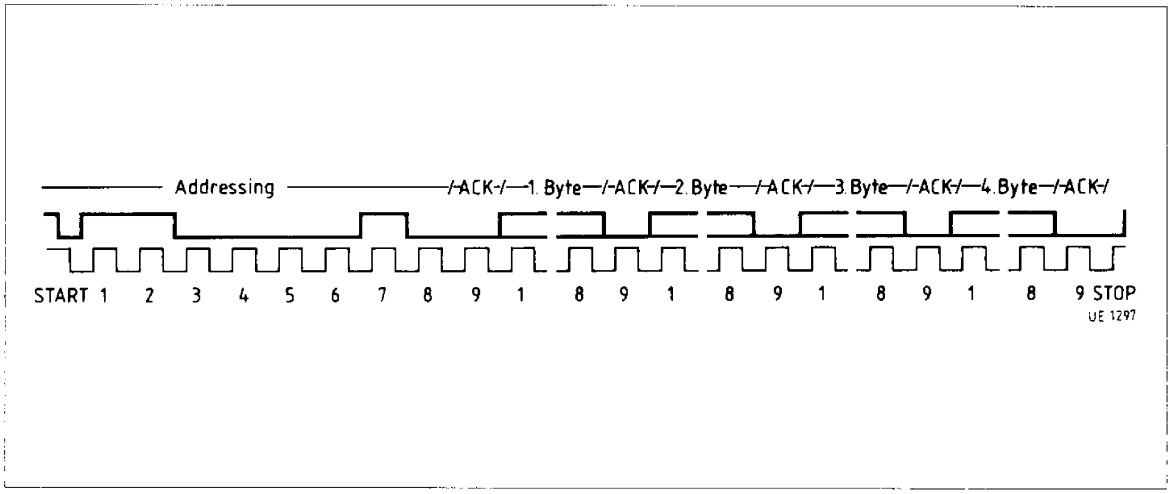
T1, T0 = 0, 0 Normal operation

T1 = 1 P3 = $f_{REF}$, P4 = Cy

T0 = 0 Tristate: charge pump output PD is in high-impedance state.

**Chip Address Switching**

| MA1 | MA0 | Voltage at CAU |
|---|---|---|
| 0 | 0 | (0 ... 0.1) $V_S$ |
| 0 | 1 | open-circuit |
| 1 | 0 | (0.4 ... 0.6) $V_S$ |
| 1 | 1 | (0.9 ... 1) $V_S$ |




**Pulse Diagram**

**Telegram Examples**

Start-Addr-DR1-DR2-CW1-CW2-Stop
Start-Addr-CW1-CW2-DR1-DR2-Stop
Start-Addr-DR1-DR2-CW1-Stop
Start-Addr-CW1-CW2-DR1-Stop
Start-Addr-DR1-DR2-Stop
Start-Addr-CW1-CW2-Stop
Start-Addr-DR1-Stop
Start-Addr-CW1-Stop

Start = start condition
Addr = address
DR1 = divider ratio 1st byte
DR2 = divider ratio 2nd byte
CW1 = control word 1st byte
CW2 = control word 2nd byte
Stop = stop condition

### Absolute Maximum Ratings

$T_A$ = – 20 to 80 °C

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply voltage | $V_S$ | – 0.3 | 6 | V | |
| Output PD | $V_1$ | – 0.3 | $V_S$ | V | |
| Crystal oscillator pins Q1, Q2 | $V_2$ | – 0.3 | $V_S$ | V | |
| Bus input/output SDA | $V_4$ | – 0.3 | 6 | V | |
| Bus input SCL | $V_5$ | – 0.3 | 6 | V | |
| Port outputs P0 ... P4 | $V_6$ | – 0.3 | 16 | V | |
| Chip address switch CAU | $V_{10}$ | – 0.3 | $V_S$ | V | |
| Signal inputs TVSAT, $\overline{\text{TVSAT}}$ | $V_{13}$ | – 0.3 | 0.3 | V | for $V_S$ = 0 V |
| Output active filter UD | $V_{16}$ | – 0.3 | $V_S$ | V | |
| Bus output SDA | $I_{4L}$ | – 1 | 5 | mA | open collector |
| Port outputs P0 ... P4 | $I_{6L}$ | – 1 | 20 | mA | open collector |
| Total port output current | $\Sigma I_L$ | | 25 | mA | |
| Junction temperature | $T_j$ | | 125 | °C | |
| Storage temperature | $T_{stg}$ | – 40 | 125 | °C | |
| Thermal resistance (junction to ambient) | $R_{th\ JA}$ | | 125 | K/W | |

### Operating Range

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | $V_S$ | + 4.5 | 5.5 | V | |
| Ambient temperature | $T_A$ | – 20 | 80 | °C | |
| Input frequency | $f_{13}$ | | 2400 | MHz | (at 25 °C) |
| Crystal frequency | $f_2$ | | 4.69 | MHz | |
| Programmable divider factor | $N$ | 256 | 32767 | | |

### AC/DC-Characteristics

$T_A$ = – 20 to 80 °C; $V_S$ = 4.5 to 5.5 V

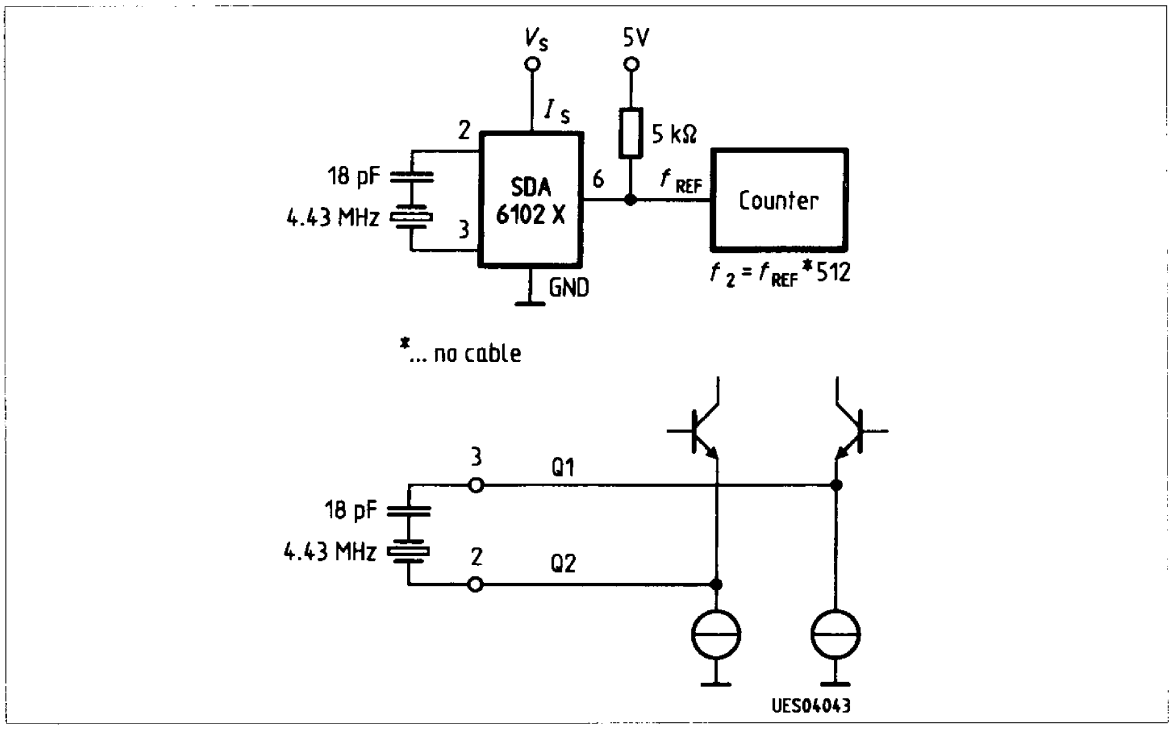
| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |
| Supply current | $I_S$ | | 45 | 59 | mA | $V_S$ = 5 V | 1 |
| Crystal oscillator frequency | $f_2$ | | 4.43 | | MHz | series capacitance18 pF $f_{xtal}$ = 4.43 MHZ | 1 |
| Oscillator amplitude (voltage across crystal)* | | | 2.6 | | V | | |
| Margin from 1st (fundamental) to 2nd and 3rd harmonics* | | | 20 | | dB | | |
| **Signal Input TVSAT/$\overline{\text{TVSAT}}$** | | | | | | | |
| Sensitivity in mVrms into 50 Ω | $a_{13}$ | – 10/ 71 | | 3/315 | dBm | $f_{13}$ = 500 MHz ... 2.4 GHz | 2 |
| **Port Outputs P0 ... P4 (switch with open collector)** | | | | | | | |
| H-input current | $I_{6H}$ | | | 10 | µA | $V_{6H}$ = 13.5 V | 3 |
| L-output voltage | $V_{6L}$ | | | 0.5 | V | $I_{6L}$ = 20 mA | 3 |
| The sum of the currents in ports P0 to P4 may not exceed 25 mA. | | | | | | | |
| **Phase-Detector Output PD ($V_S$ = 5 V)** | | | | | | | |
| Pump current | $I_{1H}$ | ± 90 | ± 220 | ± 300 | µA | 5I = high; $V_1$ = 2 V | 4 |
| Pump current | $I_{1H}$ | ± 22 | ± 50 | ± 75 | µA | 5I = low; $V_1$ = 2 V | 4 |
| Tristate current | $I_{1Z}$ | – 5 | 0 | + 5 | nA | T1 = 1; $V_1$ = 2 V | 4 |
| Output voltage | $V_{1L}$ | 1.0 | | 2.5 | V | locked | 4 |
| **Active Filter Output UD (Test mode T0 = 1; PD = tristate)** | | | | | | | |
| Output current | $-I_{16}$ | 500 | | | µA | $V_{16}$ = 0.8 V; $I_{1H}$ = 90 µA | 4 |
| Output voltage | $V_{16}$ | | | 100 | mV | $V_{1L}$ = 0 V | 4 |
| Output voltage | $V_{16}$ | | | 500 | mV | OS = 1 | 4 |
| **Chip Address Switch CAU** | | | | | | | |
| Input current | $I_{10H}$ | | | 50 | µA | $V_{10H}$ = 5 V | 6 |
| Input current | $-I_{10H}$ | | | 50 | µA | $V_{10H}$ = 0 V | 6 |

* Design note only: no 100% final inspection

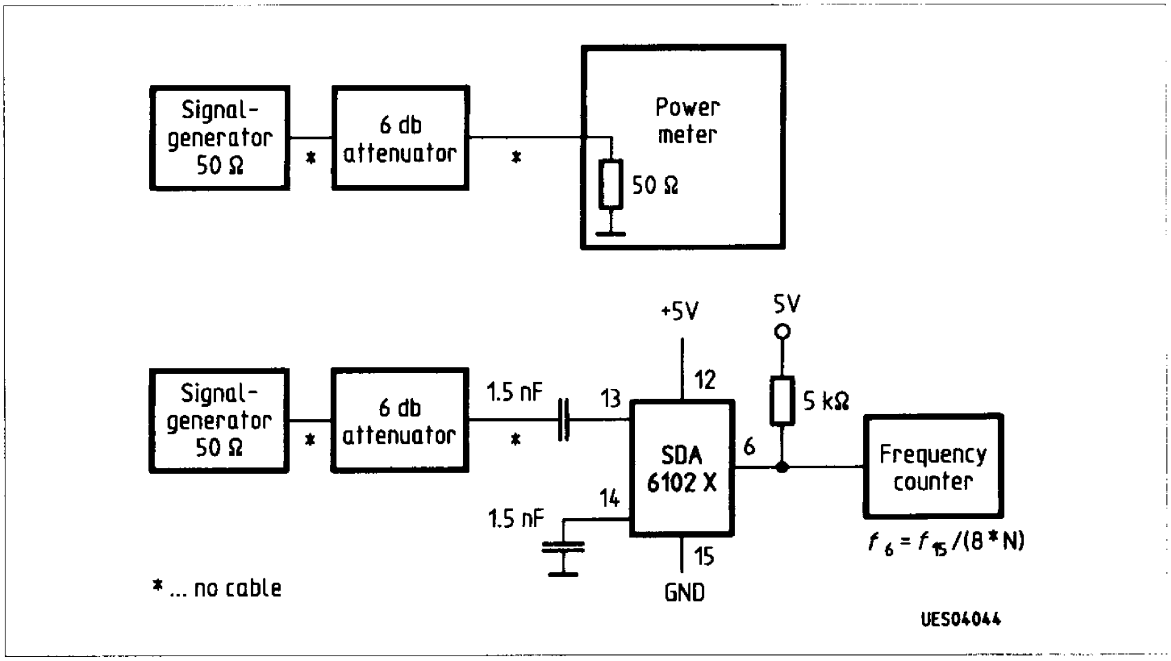
**AC/DC Characteristics** (cont'd)
$T_A$ = – 20 to 80 °C; $V_S$ = 4.5 to 5.5 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |
| **Bus Input SCL, SDA** | | | | | | | |
| H-input voltage | $V_{4IH}$ | 3 | | 5.5 | V | | 5 |
| L-input voltage | $V_{4IL}$ | | | 1.5 | V | | 5 |
| H-input current | $I_{4IH}$ | | | 10 | µA | $V_{4IH} = V_S$ | 5 |
| L-input current | $-I_{4IL}$ | | | 20 | µA | $V_{4IH}$ = 0 V | 5 |
| **Bus Output SDA (open collector)** | | | | | | | |
| H-output current | $I_{4OH}$ | | | 10 | µA | $V_{4H}$ = 5.5 V | 5 |
| L-output voltage | $V_{4OL}$ | | | 0.4 | V | $I_{4L}$ = 3 mA | 5 |
| **Edges SCL, SDA** | | | | | | | |
| Rise time | $t_R$ | | | 1 | µs | | 5 |
| Fall time | $t_F$ | | | 0.3 | µs | | 5 |
| **Shift Clock SCL** | | | | | | | |
| Frequency | $f_5$ | 0 | | 100 | kHz | | 5 |
| H-pulse width | $t_{5H}$ | 4 | | | µs | | 5 |
| L-pulse width | $t_{5L}$ | 4.7 | | | µs | | 5 |
| **Start** | | | | | | | |
| Set-up time | $t_{SUSTA}$ | 4.7 | | | µs | | 5 |
| Hold time | $t_{HDSTA}$ | 4 | | | µs | | 5 |
| **Stop** | | | | | | | |
| Set up time | $t_{SUSTO}$ | 4.7 | | | µs | | 5 |
| Bus free | $t_{BUF}$ | 4.7 | | | µs | | 5 |
| **Data Transfer** | | | | | | | |
| Set-up time | $t_{SUDAT}$ | 0.25 | | | µs | | 5 |
| Hold time | $t_{HDDAT}$ | 0 | | | µs | | 5 |
| Input hysteresis SCL, SDA* | | | 300 | | mV | | |
| Low-pass cutoff frequency SCL, SDA* | | | 500 | | kHz | | |

* Design note only: no 100% final inspection




**Test Circuit 1**

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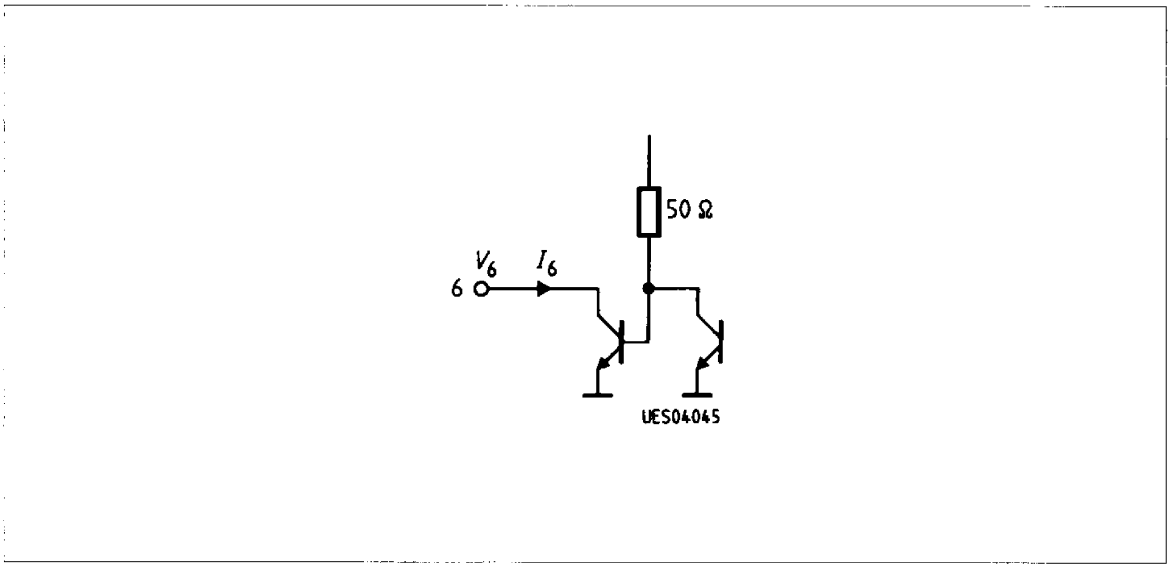
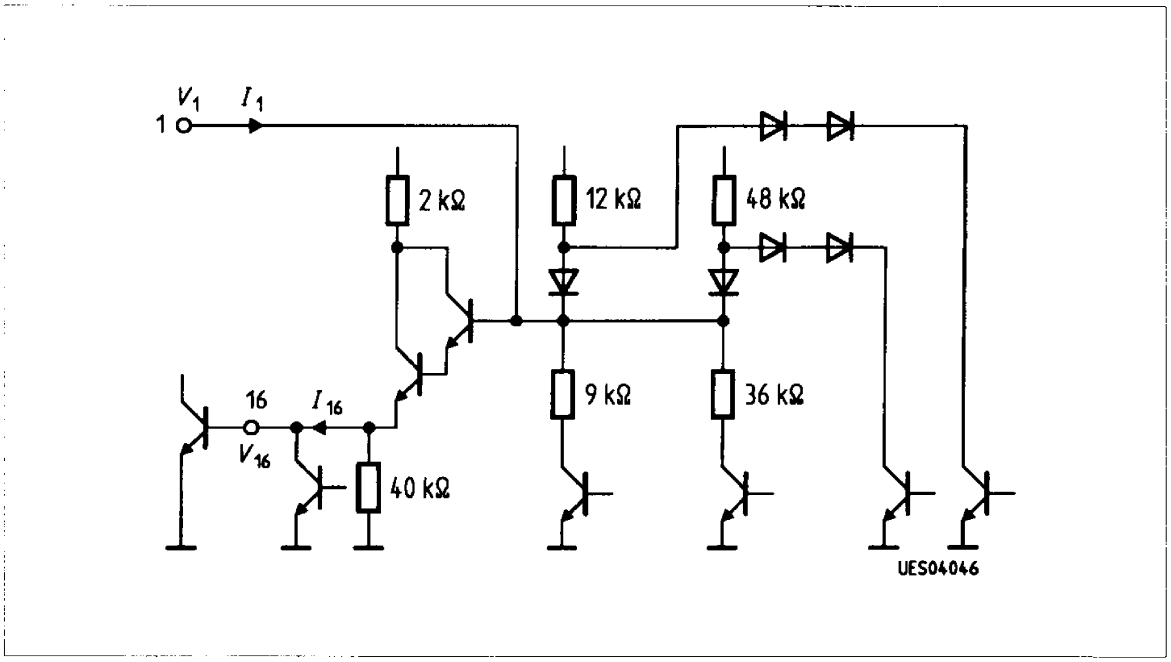
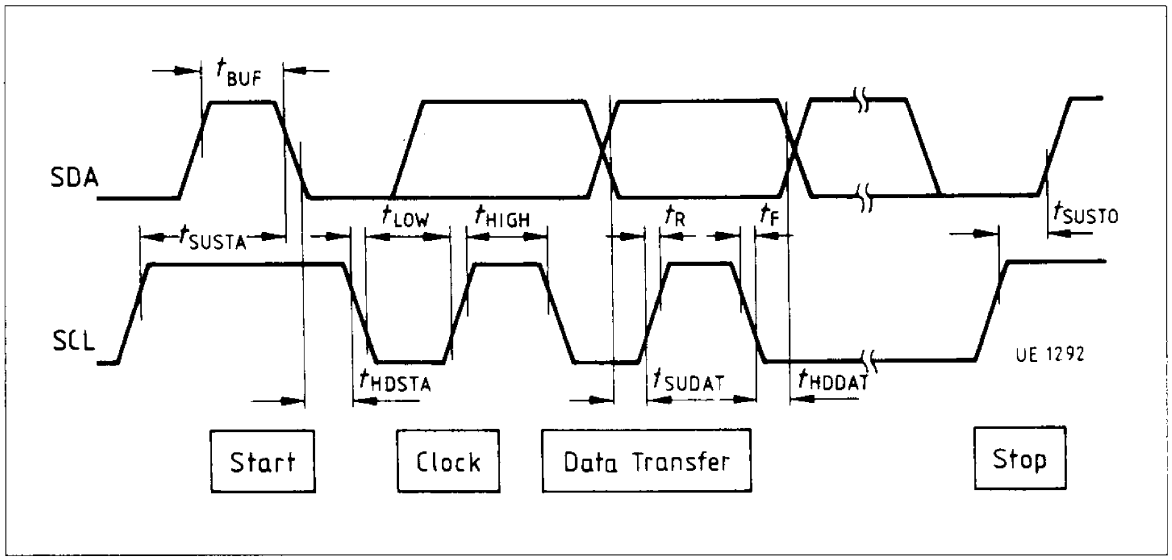



**Test Circuit 3**



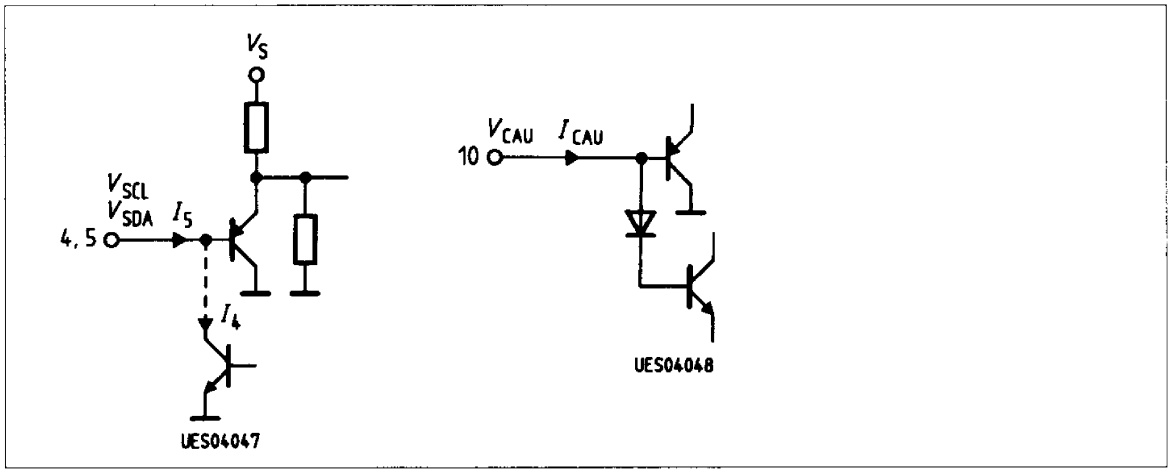

**Test Circuit 4**



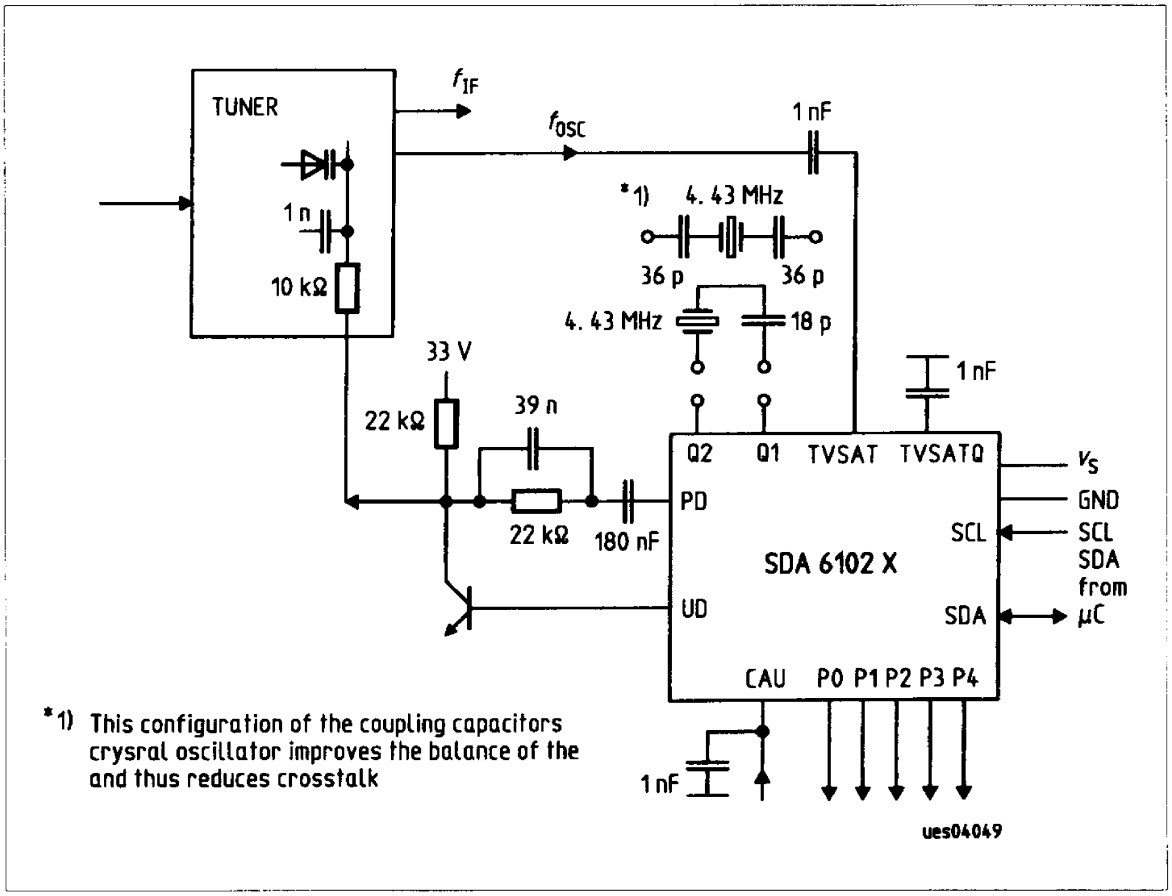

**Test Circuit 5**

| | |
|---|---|
| $t_{SUSTA}$ | Set-up time (start) |
| $t_{HDSTA}$ | Hold time (start) |
| $t_{HIGH}$ | H-pulse width (clock) |
| $t_{LOW}$ | L-pulse width (clock) |
| $t_{SUDAT}$ | Setup time (data transfer) |
| $t_{HDDAT}$ | Hold time (data transfer) |
| $t_{SUSTO}$ | Set-up time (stop) |
| $t_{BUF}$ | Bus free time |
| $t_F$ | Fall time |
| $t_R$ | Rise time |

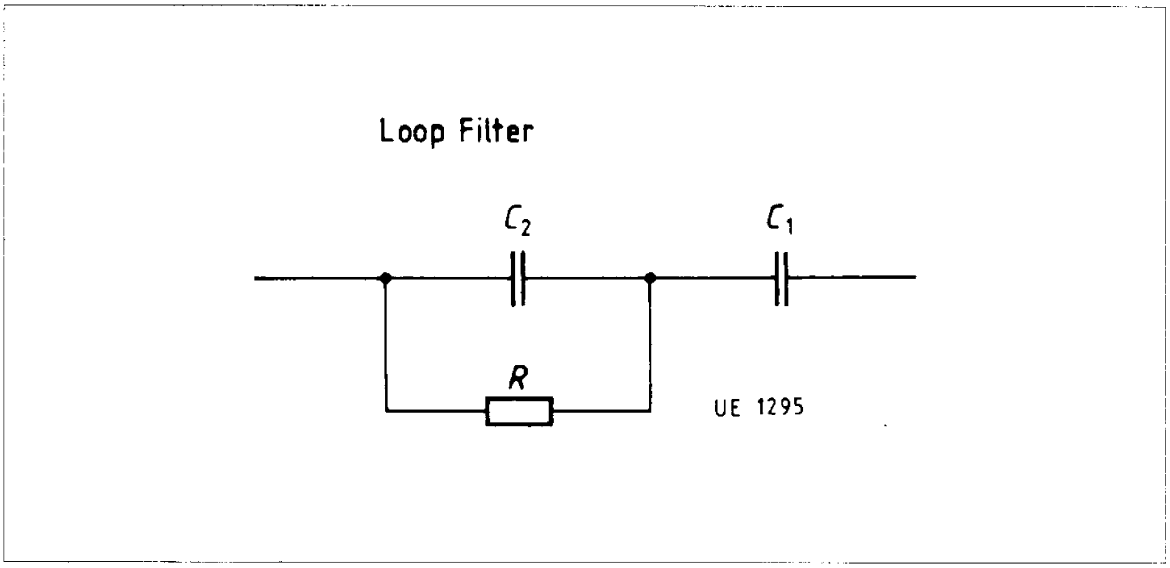
All times related to 10 % and 90 % values




**Test Circuit 6**




**Application Circuit**




**Application Circuit**

### Calculation of loop filter

Loop bandwidth: $\omega_R = \sqrt{(I_P \times K_{VCO}) / (C_1 \times P \times N)}$

Attenuation: $a = 0.5 \times \omega_R \times R \times C_1$

$P$ = prescaler
$N$ = programmable divider
$I_P$ = pump current
$K_{VCO}$ = tuner slope
$R$, $C_1$ = loop filter

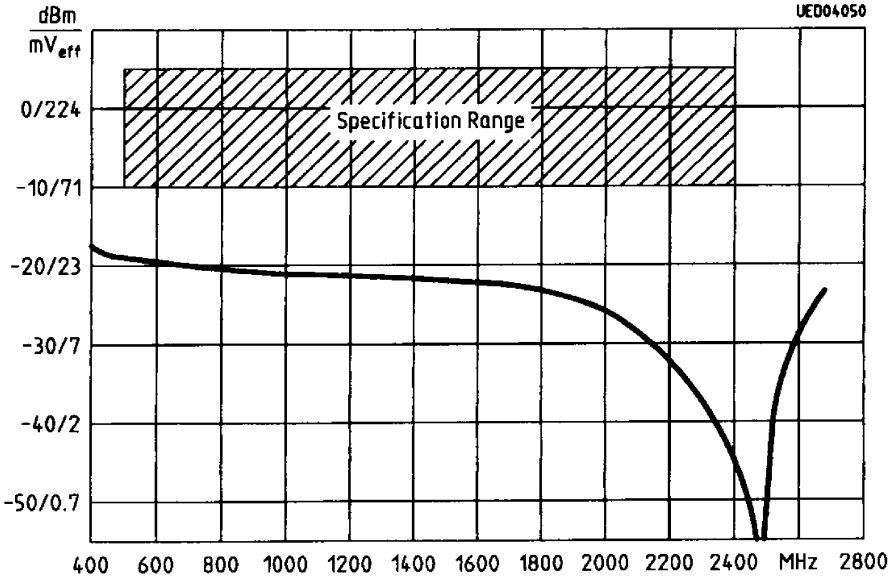
Example

$P$ = 8, $N$ = 11520, $I_P$ = 50 µA; $K_{VCO}$ = 18.7 MHz/V, $R$ = 22 kΩ,
$C_1$ = 180 nF; $\omega_R$ = 237 Hz, $f_r$ = 38 Hz, $a$ = 0.67

**Note**: The high-impedance port outputs and CAU can be decoupled from external noise with a capacitor of 1 nF.

It is important to keep to the I²C-bus specification concerning maximum capacitance and impedance.

**Sensivity at TVSAT/$\overline{\text{TVSAT}}$ Input**
(typical at 25 °C)




**I²C-Bus Noise Immunity**
Sinusoidal Noise Pulses are Applied via a
Coupling Capacitance of 33 pF to the SCL- and SDA-Inputs