128 bit Read/Write Contactless Identification Device with OTP function

Features

- 128 bit EEPROM organized in 8 words of 16 bits
- 64 bit fixed code memory array laser programmed
- OTP feature convert EEPROM words in read only
- Power on Reset sequence
- Power-check for EEPROM write operation
- Data transmission performed by Amplitude Modulation (IC to reader and reader to IC)
- Data encoding : Manchester or BI-Phase (FDX-B)
- Transmission reader to chip: typically 65% AM modulation
- Data rate : 64 or 32 RF field periods per bit
- (2 kBaud or 4 kBaud at 125 kHz)
- 78 pF resonant capacitor integrated on chip
- 100 to 150 kHz frequency range
- On-chip rectifier and voltage limiter
- No external supply buffer capacitor needed
- -40 to +85°C temperature range
- Very low Power consumption

Description

P4069 is a CMOS integrated circuit intended for use in electronic Read/Write RF transponders, with an optional lock function to disable EEPROM write operations.

The IC is powered by picking the energy from a continuous 125 kHz magnetic field via an external coil, which together with the integrated capacitor form a resonant circuit. The IC read out data's from its internal EEPROM or ROM and sends it out by switching on and off a resistive load in parallel to the coil. Commands and EEPROM data updates can be executed by AM modulation of the 125 kHz magnetic field.

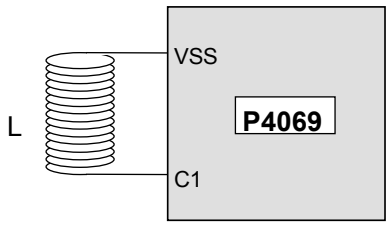
At power–up the P4069 goes in default mode in which it constantly (without any pause) transmits 128 bits from the EEPROM. Upon transmission of a specific command, the 64 bits unique laser code is output. Additional commands for writing and lock data in EEPROM are available.

The P4169 is the same device but with large bumps as indicated on the last page of this data sheet. All specified parameters and descriptions are applicable for the P4169 device.

Applications

- Access Control
- Animal Identification
- Material Logistics

Typical Operating Configuration



Typical value for inductance L is 21.5mH at f_O = 125 KHz

Figure 1

Pin Assignment

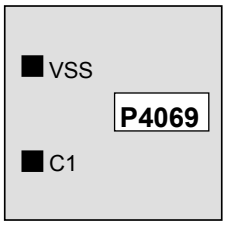


Figure 2

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Conditions
Power supply	V_{DD}	-0.3 to +5.5V
Input Voltage (pads TST, TCP, TIO)	V_{PIN}	- 0.3 to VDD+0.3V
Input current on COIL1	I_{COIL1}	-30 to +30mA
Input voltage on COIL1	V_{COIL1}	-10 to +10V
Storage temperature	T_{STORE}	-55 to +125°C
Electrostatic discharge to MIL-STD-883C method 3015	V_{ESD}	1000V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

Electrical parameters and functionality are not guaranteed when the circuit is exposed to light.

Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_{OP}	-40	+25	+85	°C
AC voltage on coil 1	V_{COIL1}		*		Vpp
Maximum coil current	I_{COIL1}	-10		10	mA
Frequency on coil 1	F_{COIL1}	100	125	150	kHz

Table 2

*) Maximum voltage is defined by forcing 10mA on Coil1 – Vss

Handling Procedures

This device has built-in protection against high static voltages or electric fields. However due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Electrical Characteristics

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{COIL1} = 125 kHz square wave, V_{COIL1} = 1V_{PP}, T_{OP} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Regulated Supply Voltage	V_{DD}	I_{COIL1} = 10mA	3.0	3.5	4.0	V	
Reg. Voltage reading EEPROM	V_{RD}		2.0			V	Note (3)
Supply current in read mode	I_{RD}			3.8	5,5	µA	
Reg. Voltage writing EEPROM	V_{WR}		2.5			V	
Supply current write mode	I_{WR}	V_{DD} = 3.5 V		50	100	µA	
Power Check Voltage	V_{PC}		2.4	2.8	3.15	V	
Modulator ON voltage drop	V_{on1}	I_{COIL1} = ±100µA	1.2	1.45	1.75	V	
Modulator ON voltage drop	V_{on2}	I_{COIL1} = ±1 mA	3	3.6	4.5	V	
POR level	V_{POR}	Rising edge	1.5	1.85	2.20	V	
Clock extractor	V_{COIL1}		0.5			V_{PP}	
Peak detector threshold.	V_{pd}	V_{DD} = 3.3 V	3.2	4	4.6	V_{PP}	
Peak detector hysteresis	V_{pdh}	V_{DD} = 3.3 V	20	100	200	mV	
Resonance capacitor	C_R	32 kHz, 0.3Vpp		78		pF	Note (1)
EEPROM data retention	T_{RET}	T_{OP} = 55°C	10			years	Note (2)
EEPROM write cycles	N_{CY}	V_{DD} = 3.6 V	100000			cycles	

Table 3

Note 1: Value of the resonance capacitor may vary in limits of ± 12%
Statistics show a variation of capacitance within one lot of ± 5%.
These figures are given as information only.

Note 2: Based on 1000 hours at 150°C.

Note 3: V_{RD} must be higher than V_{POR} Level.

Timing Characteristics

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{COIL1} = 125 kHz square wave, V_{COIL1} = 5V, T_{OP} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Option : 64 RF periods per bit						
Read bit period	t_{RDB}			64		RF periods
EEPROM write time	t_{Wee}		20			ms
Synchronization pattern phase 1	t_{S1}		4.1		5.0	ms
Synchronization pattern phase 2	t_{S2}		1.5		2.0	ms
Synchronization pattern phase 3	t_{S3}		1.5		4.0	ms
Option : 32 RF periods per bit						
Read bit period	t_{RDB}			32		RF periods
EEPROM write time	t_{Wee}		20			ms
Synchronization pattern phase 1	t_{S1}		2.1		2.5	ms
Synchronization pattern phase 2	t_{S2}		0.8		1.0	ms
Synchronization pattern phase 3	t_{S3}		0.8		2.0	ms

Table 4

RF periods represent periods of the carrier frequency emitted by the transceiver unit.
See figure 12 for Synchronization pattern phases.

Due to amplitude modulation of the coil-signal, the clock-extractor may miss clocks or add spurious clocks close to the edges of the RF-envelope. This desynchronization will not be larger than ± 3 clocks per bit and must be taken into account when developing reader software.

Block Diagram

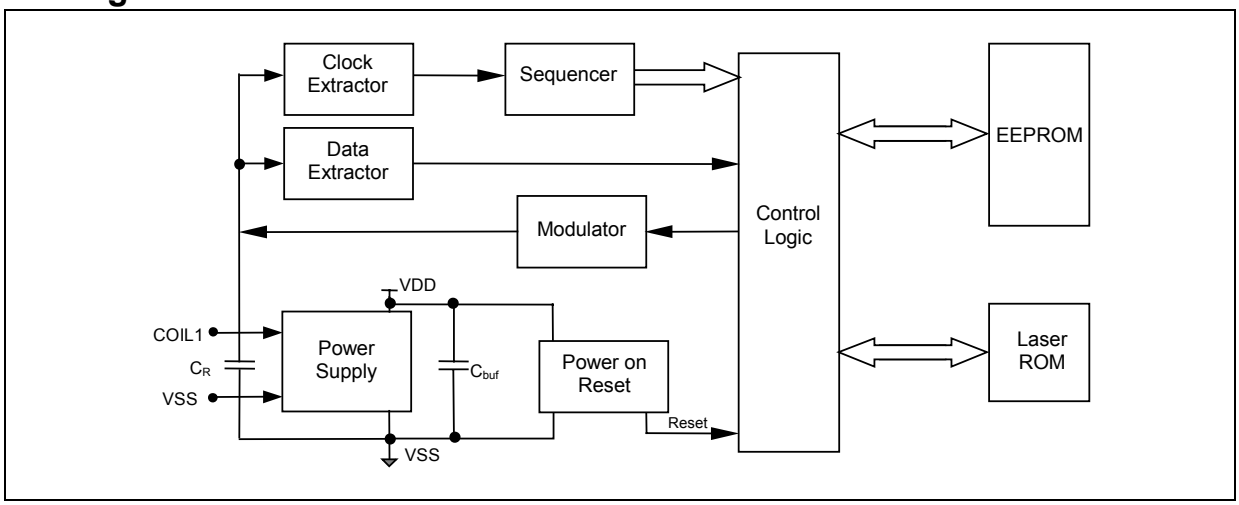


Figure 3

Functional Description

The IC builds its power supply through an integrated rectifier. When it is placed in a magnetic field the DC internal voltage starts to increase.
As long the power supply is lower than the power on reset (POR) threshold, the circuit is in reset mode to prevent unreliable operation. In this mode the modulator switch is off.
After the supply voltage cross the POR threshold, the circuit goes in read mode and transmits periodically the 128 data bits from EEPROM.
The power on reset is designed with a typically 250mV hysteresis. The specified value in the DC electrical characteristic table indicates the high level-switching threshold. Ones the supply voltage had reached this level, the device work in read mode and reenter in reset mode if the supply voltage decrease under the lower threshold (~V_{POR} – 250mV).
In read mode the IC transmits periodically either the 128 data bits from EEPROM or 64 data bits from ROM if command 2 has been sent. The bits are Manchester or BI-phase coded and issued by switching the modulator load in parallel to the coil ON and OFF. The read out process is repeated continuously without any pause as long as power level is greater than the POR threshold low.
While the IC is operating in read mode it checks the coil signal once every bit period. If it detects a certain reader induced amplitude modulation of magnetic field it stops modulating and waits for a command word. In the case the EEPROM write command is detected the contents of selected EEPROM word is modified. Read ROM command will change the output sequence to the data provided by the laser ROM continuously.
The Reset command returns to the initial mode as after a Power on Reset.

Block description

Power On Reset (POR)

When the P4069 with its attached coil enters an electromagnetic field, the built in AC/DC converter will supply the chip. The DC voltage is monitored and a Reset signal is generated to initialise the logic. The Power On Reset is also provided in order to make sure that the chip will start issuing correct data.
Hysteresis is provided to avoid improper operation at the limit level.

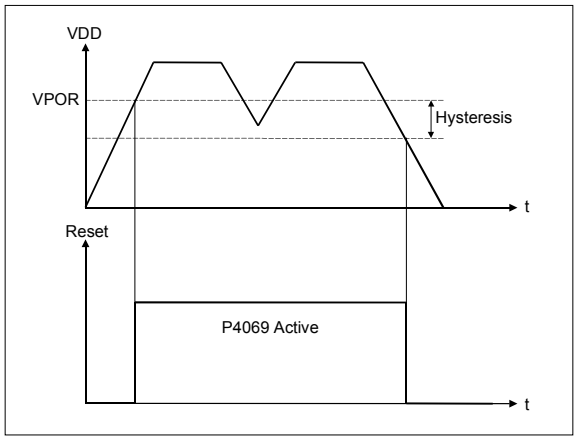


Figure 4

Clock Extractor

The Clock extractor will generate a system clock with a frequency corresponding to the frequency of the RF field. The system clock is used by a sequencer to generate all internal timings.

Data Extractor

The transceiver generated field will be amplitude modulated to transmit data to the P4069. The Data extractor demodulates the incoming signal to generate logic levels, and decodes the incoming data.

Modulator

The Data Modulator is driven by the serial data output from the transceiver. The modulator will draw a large current from both coil terminals, thus amplitude modulating the RF field according to the selected memory data.

AC/DC Converter and Voltage Limiter

The AC/DC converter is fully integrated on chip and will extract the power from the incident RF field. The internal DC voltage will be clamped to avoid high voltage in strong RF fields.

Lock All / Lock Memory Area

The P4069 can be converted to a Read Only chip or be configured to Read/Write and Read Only Areas by programming the protection word. This configuration can be locked by write inhibiting the Write Protection Word. Great care should be taken in doing this operation as there is no further possibility to change the Write Protection Word. The Control Word can also be protected in the same way thus freezing the writing operation.

P4069 Modes of operation

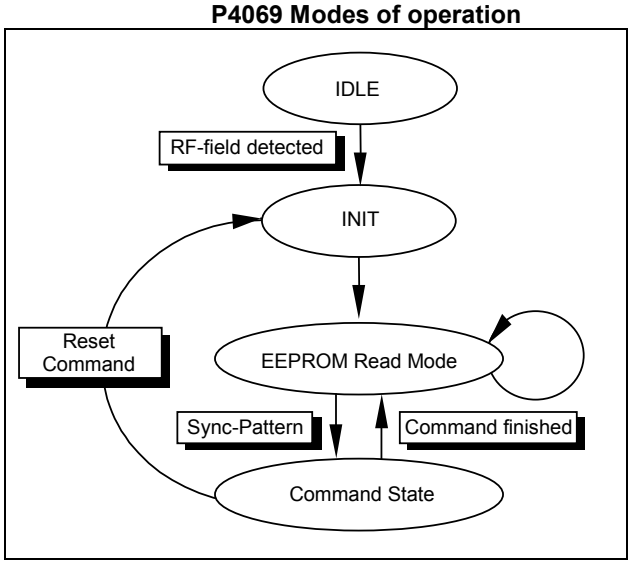


Figure 5

Read Mode

The P4069 holds 128 bits of user EEPROM. These 128 bits are cyclically read out by default. Using the write command, the EEPROM words can be modified. The EEPROM contains an additional configuration word used to protect writing in the EEPROM.

The P4069 additionally holds a unique 64 bit read only identification code, which can be accessed by using the Read ROM command.

Manchester encoding

One bit period lasts 64 (or 32) field frequency periods (512 (or 256) µs at 125 kHz). The Manchester coding shows a transition from ON to OFF or from OFF to ON in the middle of bit period. At the transition from logic bit “1” to logic bit “0” or logic bit “0” to logic bit “1” the phase change. Value "high" of data stream presented below represents modulator switch OFF, "low" represents switch ON (see figure 6a).

Bi-phase encoding

One bit period lasts 64 (or 32) field frequency periods (512 (or 256) µs at 125 kHz). The BI-phase coding shows a transition from ON to OFF or from OFF to ON in the middle of a bit period when the data bit is a logical “0”. A logical bit set to “1” will keep its ON or OFF state for the whole bit period. There is always a transition from ON to OFF or from OFF to ON at the beginning of a bit period. The picture below shows part of a data stream. Value “high” of data stream represents modulator load OFF, “low” represents modulator load ON (see figure 6b).

Manchester encoding

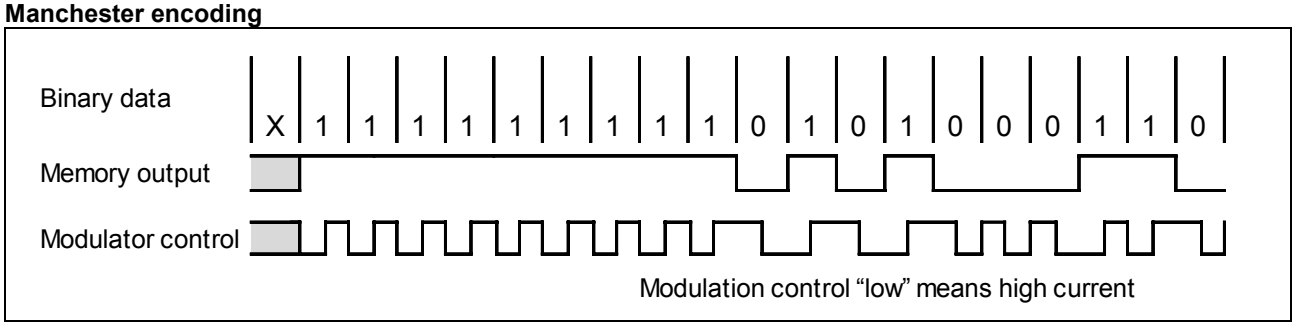


Figure 6a

Bi-phase encoding

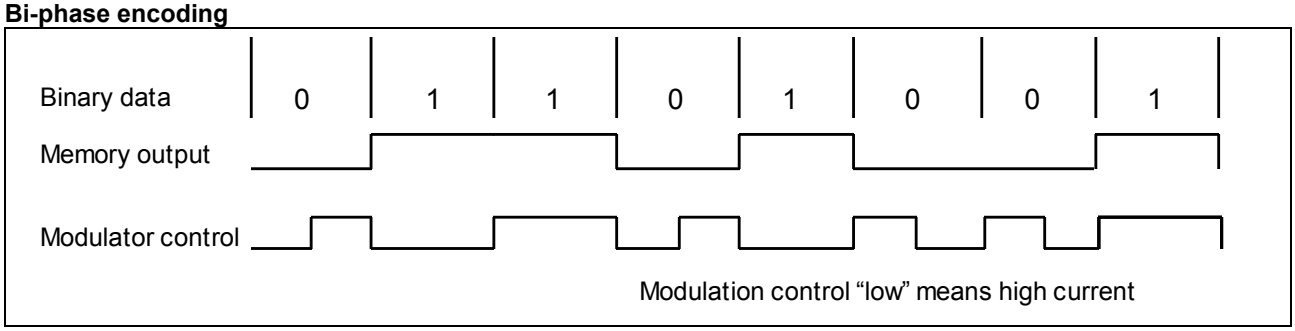


Figure 6b

EEPROM organization

The EEPROM is organized in 8 words of 16 bits. EEPROM words are counted from 0 to 7. Bits in an EEPROM word are counted from 0 to 15. When EEPROM readout is initiated (after POR or after return from command to read mode) read out is started from word 0 and increments to word 7. Readout in a word is started by bit 0 and then increments up to bit 15. After word 7 bit 15 is read readout continues with word 0 bit 0 without any pause. So it is very important to organize data written in EEPROM in a way that reader can detect the position of bits in data stream. For Manchester encoding Word 0 and word 4 are factory programmed and locked (see figure 7a), for BI-phase encoding the 8 words are user free (see figure 7b and 7c). Following tables show how standard versions are factory programmed.

EEPROM Configuration for Manchester encoding (Version 1 and 11)

Word name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
4	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
5	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Configuration	1	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Figure 7a

EEPROM Configuration for BI-phase encoding and 64 RF cycles/bit data rate (Version 21)

Word name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1
2	1	0	1	1	1	0	0	0	1	1	0	0	1	0	0	1
3	0	1	0	0	0	1	0	0	0	1	1	0	0	1	0	1
4	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
5	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	1
6	1	0	1	1	1	0	0	0	1	1	0	0	1	0	0	1
7	0	1	0	0	0	1	0	0	0	1	1	0	0	1	0	1
Configuration	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Figure 7b

EEPROM Configuration for BI-phase encoding and 32 RF cycles /bit data rate (Version 31)

Word name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
4	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
5	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Configuration	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Figure 7c

ROM organization

The ROM is composed of 64 bits divided in a 9-bit header, 10 nibbles of 4 data bits and 1 row even parity bit, 4 column even parity bits, and 1 stop bit. The Read ROM command will output the contents of the ROM, starting with bit-0. When bit-64 is output, the sequence continues with bit-0.
Data in ROM is written by laser programming during manufacturing to form a unique identification code.
Figure below presents the ROM data structure. Bits P0 to P9 are row parity bits and bits PC0 to PC3 are column parity bits. Parity is even so that a 9 bits set to logic one header can not be reproduced in a data stream.

Bit 0	1	1	1	1	1	1	1	1	1	Bit 8	Header
				Bit 9	D00	D01	D02	D03	P0	Bit 13	8 bits customer ID
				Bit 14	D10	D11	D12	D13	P1	Bit 18	
				Bit 19	D20	D21	D22	D23	P2	Bit 23	
				Bit 24	D30	D31	D32	D33	P3	Bit 28	
				Bit 29	D40	D41	D42	D43	P4	Bit 33	Unique
				Bit 34	D50	D51	D52	D53	P5	Bit 38	device
				Bit 39	D60	D61	D62	D63	P6	Bit 43	serial
				Bit 44	D70	D71	D72	D73	P7	Bit 48	number
				Bit 49	D80	D81	D82	D83	P8	Bit 53	
				Bit 54	D90	D91	D92	D93	P9	Bit 58	
				Bit 59	PC0	PC1	PC2	PC3	0	Bit 63	Column parity bits

Figure 8

Customer ID for all standard versions is 01 hex.

Command description

The P4069 operates in different modes. The default following a Power on Reset is Read EEPROM mode, and by means of different commands, the circuit can switch to the following modes :

- read access to ROM
- write access to 16 bits of EEPROM
- write access to configuration word
- read access to configuration word

The reader has to generate the commands, which have to be decoded by the P4069.

Command	Command Short name	Bit pattern	Function
Command 1	rst	1010 0000	Reset and return to EEPROM read
Command 2	rROM	1010 0101	READ 64 bit ROM
Command 3	wr	1100.add.data.crc	WRITE 16 bit EEPROM word
Command 4	wcw	1101 0011.prot.crc	WRITE configuration word
Command 5	rcw	1111 0000	Read configuration word

Table 5

Commands rst, rROM and rcw affect readout. An eight-bit pattern has to be sent to execute them. Write commands are longer since associated address and data have to be sent. The leftmost bit in command bit pattern is transferred first.

Command 1: Reset command

During activation of the transponder a return to default mode is possible from any mode with the reset command.

Command 2 : Read out of ROM 64 Bits

After activation of command 2, the 64 bit ROM data will be read out cyclically. This mode will be active until power down or reset command.

Command 3 : Write 16 Bit EEPROM word

After activation of command 3, a 16-bit EEPROM word can be written. Data transmission will be secured by CRC check information, which has to be calculated by the reader and which will be checked by the P4069.

Command 4 : Write configuration word
Command 4 has the same structure as command 3. The 16-bit configuration word is written by this command. A partial locking (write inhibit) of the 128 bit memory is possible in blocks of 16 bits (16 bit word becomes read-only).
The bits of configuration word are OTP (one time programmable) so once a certain bit in configuration word is set it cannot be reset.

Command 5 : Read configuration word
Read configuration word command is an auxiliary command used to read configuration word. This mode will be active until power down or reset command.
The 8-bit CRC with polynomial $u^8 + u^4 + u^3 + u^2 + u^0$ is used in commands 3 and 4. The CRC is calculated including the Command-Byte.

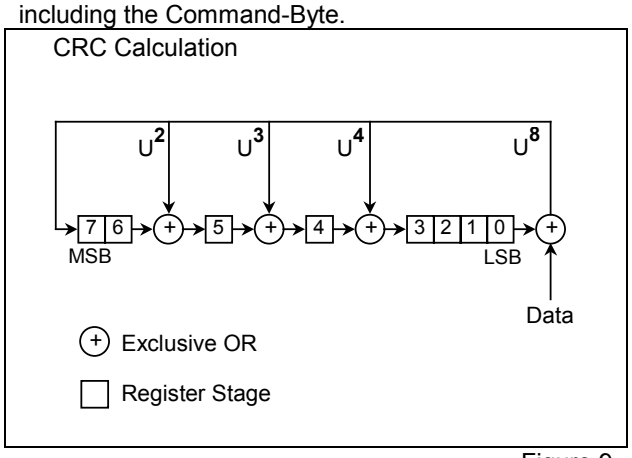


Figure 9

The following table shows the CRC according to some test bytes:

Byte [hex]	**Resulting CRC** [hex]
01	1D
80	26

Table 6

In test above it is supposed that the leftmost bit is the MSB and is transmitted first.

Within 1ms after EEPROM update completion, a further command will be accepted by the P4069 without a new synchronization pattern.
After time-out of this period, the P4069 will return to read out mode.

Write 16 bit EEPROM Word Command
As described in the Command Table an 8-bit pattern has to be sent to execute commands rst, rROM and rcw. Bit pattern of Write Word command is different since word address, 16 bits of data and 8 bit CRC have to be transmitted. The Write command bit pattern is the following:

1100 [4 bit word address] [16 bit data] [8 bit CRC]

Word address:
One of eight EEPROM words is selected. Valid addresses are in range from 0 (0000) to 7 (0111)

Data bits:
During read out bit which is first sent in is first read out (FIFO)

CRC:
Calculated over whole command stream

Example of Write Word command:
C5 D2 2D 20 (hex)
The above command (1100 0101) write to

- Word 5
- hexadecimal data “D2 2D”
- CRC bits are hex 20.

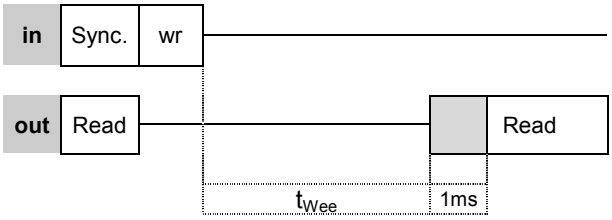


Figure 10

Write Configuration word Command
Configuration word is a special word which is used to lock (protect from writing) EEPROM words. The bits of configuration word are OTP (once programmed at 1 they can not be reprogrammed to 0).

Special care has to be taken when adding lock bits to the protection word that already has some bits set to one. The bits that are already set to one have to be confirmed at a new command in order to allow writing of additional bits. If not, bits that are already locked stay locked, and the new selected bits might not be programmed (see example below).

The bit pattern of the Write configuration word command is compatible to Write Word command:

1101 0011 [8 bits protecting 8 words] [8 bits don't care] [8 bit CRC]

8 bits protecting 8 words:
Bit first sent in is protecting word 0, the second bit protects word 1 and so on.
8 bits don't care:
Any 8-bit pattern, all 0 pattern is not suggested for power supply reasons.

CRC has to be correct including also don't care bits.

Example of Write Configuration Word command:
D3 02 55 2F (hex)
The above command (1101 0011) will protect word 6 (0000 0010) from being written.

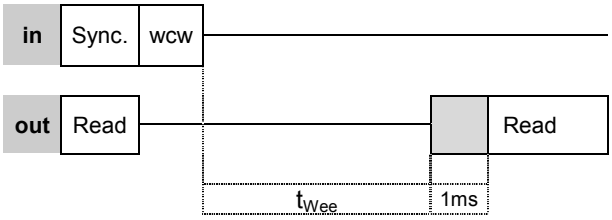


Figure 11

If later on, word 1 has to be protected, the protection bit of already protected word 6 has to be set to logic 1 again. The new command will have to be sent with the following protection bits: 0100 0010.

Read Configuration word Command
To enter this command the IC has to be in default mode (read EEPROM bits). After execution of this command the IC will cyclically read 128 bits.
16 of them will represent the configuration word the rest is 0. It is suggested that don't care bits of configuration word are programmed with some pattern which will be easy to recognize during read out.

Command Timing for 8-bit command
While IC is in Read mode it is sampling the peak level of coil voltage (during the time modulator switch is ON) once every bit period. The peak to peak value is compared with an internal reference in order to get a one-bit information (high field or low field). The measured level is compared with previous samples in order to detect whether there is a reader-induced modulation present on the magnetic field.
Commands are accepted in the range where normal field (100% strength) is higher than internal reference (considered as high field) and modulated field is lower than internal reference (considered as low field). An 65% modulation on the reader signal is proposed (high field 100%, low field 20%).
When the synchronization pattern of modulation on magnetic field is detected (Command Envelope) the P4069 waits for a Start Bit (SB).
If the start bit is detected before t_{S3} time-out is expired, the Command Processing mode is entered.
Eight command bits are serially entered. After the last bit was shifted, the 8-bit pattern is compared to one of the 5 possible commands. In the case one of the commands is recognized the appropriate action is performed otherwise the IC returns in Read mode.

Detection of Command Envelope
The Peak Detector performs the measurement once every bit period. The Peak Detector circuit compares the peak value of voltage on the coil to the internal voltage reference. The result of comparison is one bit of information, which tells to Control Logic whether the field is strong (HIGH field) or weak (LOW field).

The Peak Detector circuit has a built-in hysteresis of typically 100mV which prevents unwanted Envelope detection in field strength which is at the level of the Detector threshold.

Detection of Start Bit (SB) and Command Word
After the Synchronization pattern Envelope was detected, the P4069 is sampling the incoming signal at a T_{RDB} /8 rate. The start bit is accepted as valid when three consecutive samples are LOW.

Duration of start bit (version 64 clocks/bit) and following command bits are expected to be 512 µs (same as one bit period in read mode). In the version 32 clocks/bit, the duration is 256 µs

When the start bit is detected, the Control Logic starts switching Modulator load OFF and ON (First half of bit period OFF and second half of bit period ON) to assure enough power for operation of the IC. Samples of incoming bits are taken during the time the modulator load is ON (connected).

The command, address, data and CRC bits are sent in non coded form (NRZ), reader induced high field (non modulated) corresponds to logic one, low field (modulated) to logic zero.

Modulation of Magnetic Field

The modulation envelope of the magnetic field induced by the reader is observed by the P4069 as shown in the following figure.

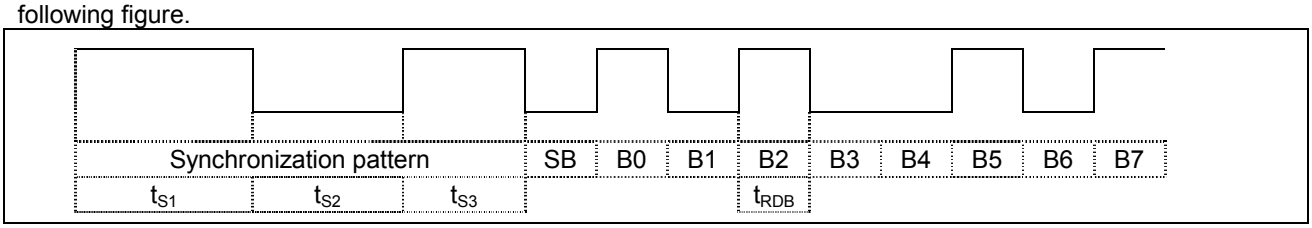


Figure 12

Comment to above timings:

t_{S1} : at least 4 samples of peak detector have to be HIGH. In worst case the distance between samples can be 2 bit periods.

t_{S2} : at least one sample LOW. 2 bit periods + some security since the IC and R/W unit are not synchronized. Duration of 3 bit periods is suggested.

t_{S3} : one sample high to enter Command Processing state defines lower limit. Watchdog timer defines higher limit (8 bits periods) Please note that during this time the Modulator load is permanently on so this is the worst case for Power Supply level. So using shorter times than upper limit is advised. Duration of 3 bit periods is suggested.

Refer to table 4 for timings range.
In the above example, the Read ROM command (1010 0101) is sent.
After successful 8-bit command detection, the P4069 will output continuously the ROM contents.

Reset, Read ROM and Read Configuration Word commands

After detecting these commands the IC returns in read mode and starts reading corresponding block (EEPROM or ROM).

Write Word and Write Configuration Word commands

For Write commands, a total of 32 significant bits have to be transferred from reader to P4069. The 32 bits are transferred in a sequence of 4 bytes. Each byte is headed with start bit at logic 0 (as in normal 8-bit command) and trailed with stop bit at logic 1. The antenna sends an uninterrupted sequence of 40 bits (32 command bits, 4 start bits and 4 stop bits).
This data organization ensures re-synchronization of the P4069 with the reader signal, and avoids that wrong data would be extracted due to missing or spurious clocks from the clock-extractor of the IC.

The IC treats the Write command as follows:

First byte received is treated in the same way as for an 8-bit command. In the case that the processing of the first byte detects a Write Word command, it first puts the modulator load OFF for 1/2 bit period. During this time, the antenna field is High (as stop bit is at logic one) so the internal power supply capacitor can be charged. Next the P4069 transitions to Start Bit Detection State with modulator load ON and waits for start bit at logic 0. The time out value is 2 t_{RDB}. If time out is reached before a start bit is detected, the IC then returns to the read mode. Normally the start bit comes already after 1 t_{RDB} and the P4069 then continues to process the next byte.
After the fourth byte has been detected, the P4069 verifies if the CRC check is OK and if the word, which is addressed for writing, is not protected by the configuration word. Next, power check is performed to determine whether there is enough power available to write EEPROM. This operation lasts 1.5-bit periods. In the case all conditions above are fulfilled (CRC, protection, power check) EEPROM is written. If one of the conditions fails, the P4069 returns in read mode without writing EEPROM.

The Write Configuration word command procedure is the same as above, the only exception is that only CRC verification and power check are done.

Writing to EEPROM lasts 20 ms.

After successful writing of EEPROM the IC sends an acknowledge pattern to confirm the completion of writing. Acknowledge pattern consists of switching the modulator load ON and OFF with a signal period of 256 µs (Option 64 clocks/bit) or 128 µs (Option 32 clocks/bit) representing half a bit period (a quarter of bit period ON, a quarter of bit period OFF). Acknowledge pattern is transmitted during a time equivalent to two bit periods. Pulses of this length do not occur during data readout so the acknowledge pattern is easily recognizable.

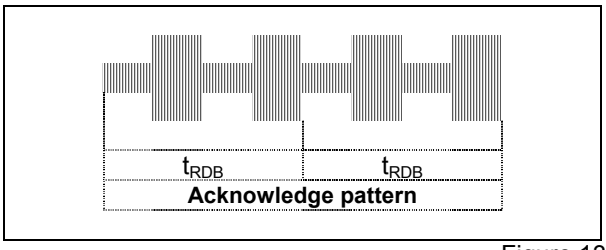


Figure 13

After sending the acknowledge pattern the P4069 transitions to the Start Bit Detection state and waits for the start bit of next command. In this way, several words can be written to EEPROM without returning in read mode after every write. The value of the timer is 2 t_{RDB}.

Disabling of Command Detection
In certain cases the IC logic blocks the detection of the Synchronization pattern Envelope during one complete readout cycle of 128 bits. This is valid in the following cases :

- at power up (after POR)
- after a Reset command
- after a time out occurs in the Start Bit Detection state (only in the case the transition to Start Bit Detection state was done from Read mode)

Details about command timing
Command timing is based on NRZ (non-return to zero) modulation on the magnetic field (as shown in figure 11). NRZ modulation is simple and leads to good results in proximity of the reader. To send a bit-1, the reader does not modulate the signal for a complete bit period, and to send a bit-0, it modulates the carrier frequency during a whole bit period.

Long streams of zeros (in write command data sequence or CRC) reduce writing distance due to drop of supply voltage under POR level, due to the long time the carrier frequency is in LOW field mode.

The writing distance can be improved by using RTO (return to one) modulation coding. Short burst of high field (approximately 1/4 of bit period) during transmission of a bit-0 to P4069, recharge the on-board power supply buffer capacitor. To operate in this way, it is important to be synchronized with the sampling rate of the P4069.
Figure 14 shows the processing of hexadecimal data “96” in the write command string. The following signals are drawn :

P4069 : shows the modulator state. The “low” peak to peak value indicates that the modulator load is connected, and a “high” peak to peak value means that the modulator load is disconnected.

NRZ : Reader generated field. Low field is forced when sending a bit-0 and High field for a bit-1. The field is at the same level for the whole bit duration.

RTO : Reader generated field as NRZ, with a burst of high field during 1/4 period for the transmission of a bit-0.

At the beginning of timing diagram, the P4069 is in start bit detection state, modulator load and peak detector are ON. When the start bit is detected, the logic transitions in command processing state. 3/8 to 1/2 of a bit period after beginning of start bit (T1), P4069 starts putting the modulator load half bit period OFF and half bit period ON. The sample of field strength which gives to the logic the value of bit is taken at the end of ON period.

Assuming that the start bit duration is 1 bit period, the following bit samples are taken 3/8 to 1/2 of bit period after start of each bit period. So during the last quarter of bit period the field can be put high to recharge the P4069 on-board capacitor.
The sampling point can be moved by changing the start bit duration.

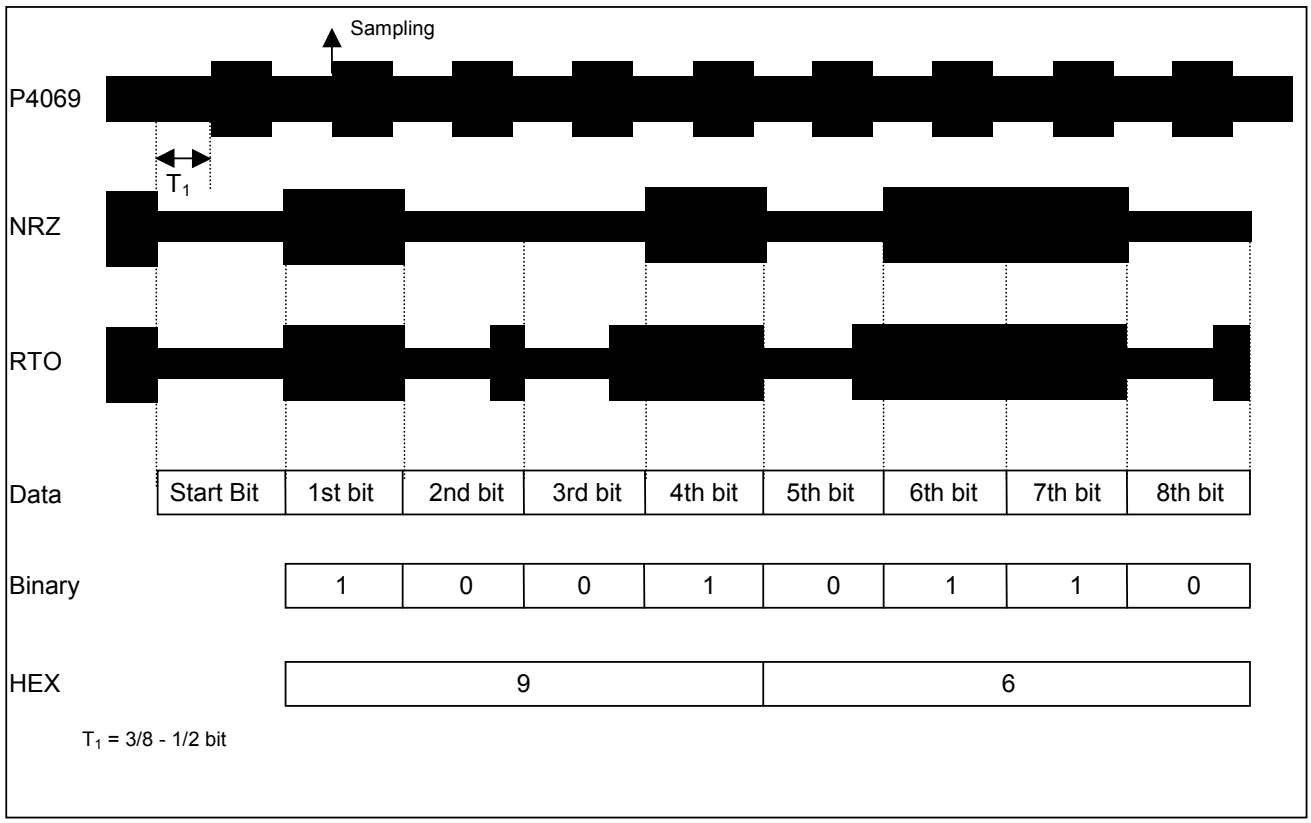


Figure 14

Pad Assignment

Pin	Name	Type	Description
1	C1	Analog	coil connection
2	VSS	supply	coil connection, negative supply
3	VPOS	supply	unregulated positive supply
4	TIO	Input/ Output	Test pad
5	TINC	Input	test pad with pull down
6	TST	Input	test pad with pull down
7	TCP	Input	test pad with pull down
8	VDD	supply	positive supply

Table 7

PCB package

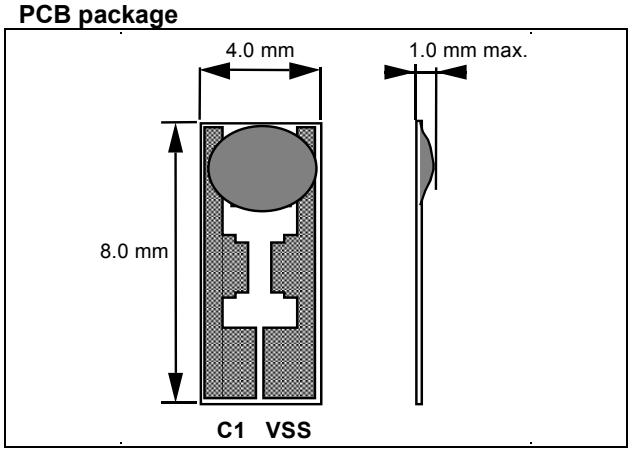
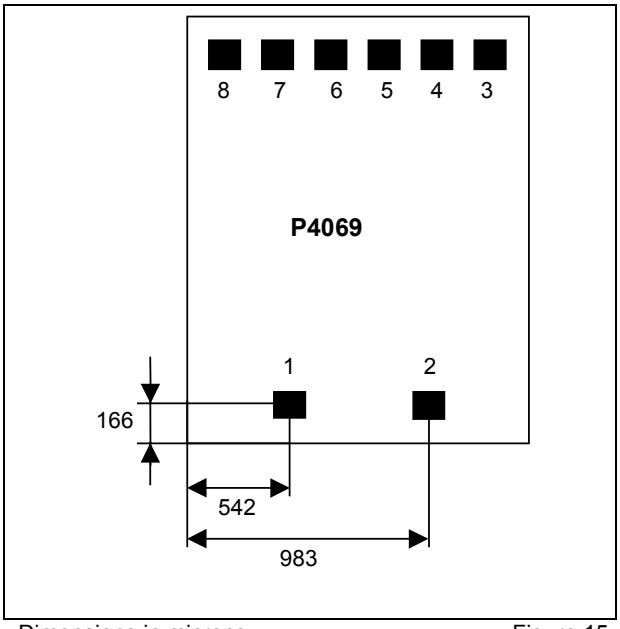


Figure 14

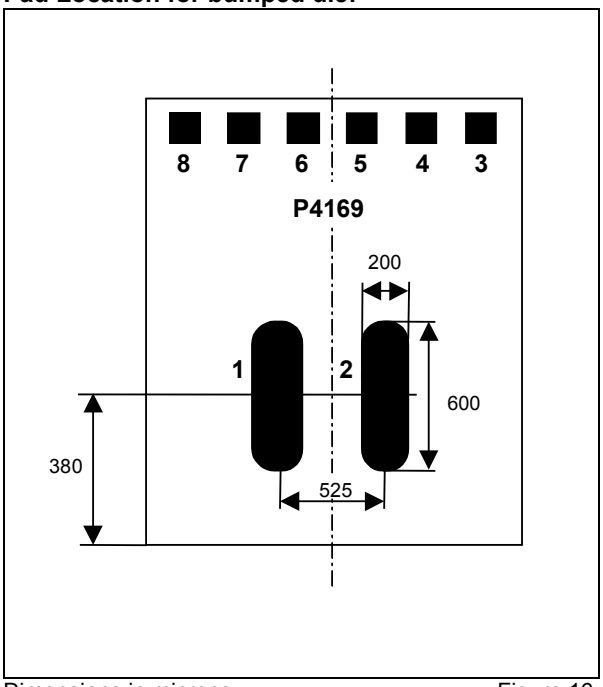
Pad Location:



Dimensions in microns Figure 15

Chip size : 1448 x 2007 µm

Pad Location for bumped die:



Dimensions in microns Figure 16

Chip size : X=1448, Y=2133
Bump height: 17.5µ ± 5µ
Hardness: min. 35, max. 80 vickers

Ordering Information

The P4069 is available in:

Die form	**P4069** <version> **IC**
CIDpack	**P4069** <version> **CID**
PCB package	**P4069** <version> **PCB**
Bumped die	**P4169** <version> **IC**

For Die form, please contact EM Microelectronic-Marin S.A. or an agreed sale office.

Version 01	Manchester coded, 64 RF clocks/bit
Version 11	Manchester coded, 32 RF clocks/bit
Version 21	BI-phase coded, 64 RF clocks/bit
Version 31	BI-phase coded, 32 RF clocks/bit

CID package

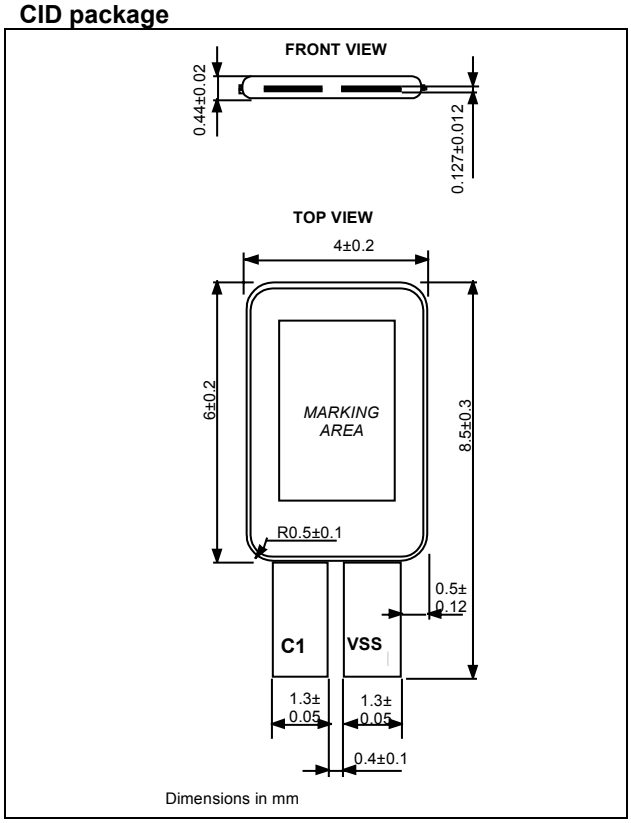


Figure 17