EM MICROELECTRONIC-MARIN SA

A COMPANY OF THE SWATCH GROUP

P4095 Read/Write analog front end for 125kHz RFID Basestation

Features

- Integrated PLL system to achieve self adaptive carrier frequency to antenna resonant frequency
- No external quartz required
- 100 to 150 kHz carrier frequency range
- Direct antenna driving using bridge drivers
- Data transmission by OOK (100% Amplitude Modulation) using bridge driver
- Data transmission by Amplitude Modulation with externally adjustable modulation index using single ended driver
- Multiple transponder protocol compatibility (Ex: H400X, V4050, P4150, V4070, P4170, P4069….)
- Sleep mode 1µA
- USB compatible power supply range
- -40 to +85°C temperature range
- Small outline plastic package SO16 or PSOP2 16

Description

The P4095 chip is a CMOS integrated transceiver circuit intended for use in an RFID basestation to perform the following functions:

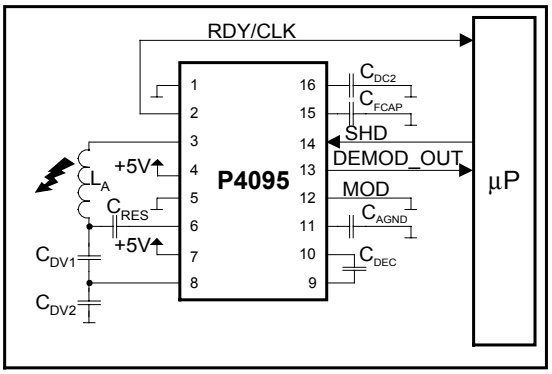
- antenna driving with carrier frequency
- AM modulation of the field for writable transponder
- AM demodulation of the antenna signal modulation induced by the transponder
- communicate with a microprocessor via simple interface.

Applications

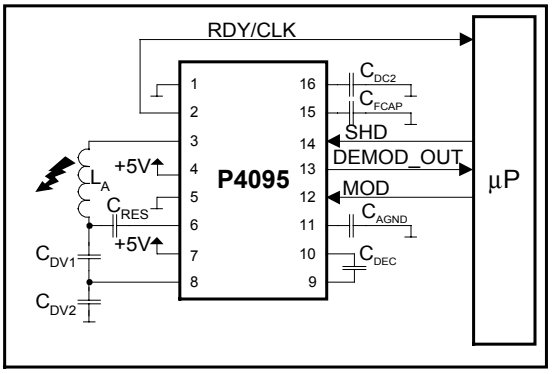
- Car immobiliser
- Hand held reader
- Low cost reader

Typical Operating Configuration

Read Only Mode

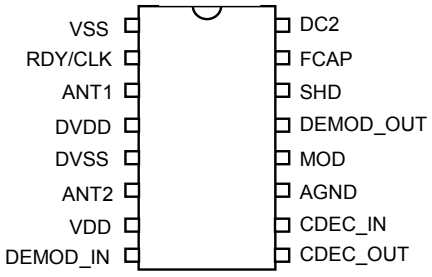


Read / Write Mode



Pin assignment

SO16



Absolute Maximum Ratings

Parameter	Symbol	Conditions
Storage temperature	T_{STO}	-55 to +150°C
Maximum voltage at V_{DD}	V_{DDmax}	V_{SS}+6V
Minimum voltage at V_{DD}	V_{DDmin}	V_{SS}-0.3V
Max. voltage other pads	V_{MAX}	V_{DD}+0.3V
Min. voltage other pads	V_{MIN}	V_{SS}-0.3V
Max. junction temperature	T_{JMAX}	+125°C
Electrostatic discharge max. to MIL-STD-883C method 3015 against V_{SS}	V_{ESD}	4000V
Electrostatic discharge max. to MIL-STD-883C method 3015 (only for pins ANT1 and ANT2) against V_{SS}	V_{ESD_ANT}	10000V
Maximum Input/Output current on all pads except V_{DD}, V_{SS}, DV_{DD}, DV_{SS}, ANT1, ANT2, RDY/CLK	I_{IMAX} I_{OMAX}	10mA
Maximum AC peak current on ANT1 and ANT2 pads 100 kHz duty cycle 50%	I_{ANTmax}	300mA

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component.
Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

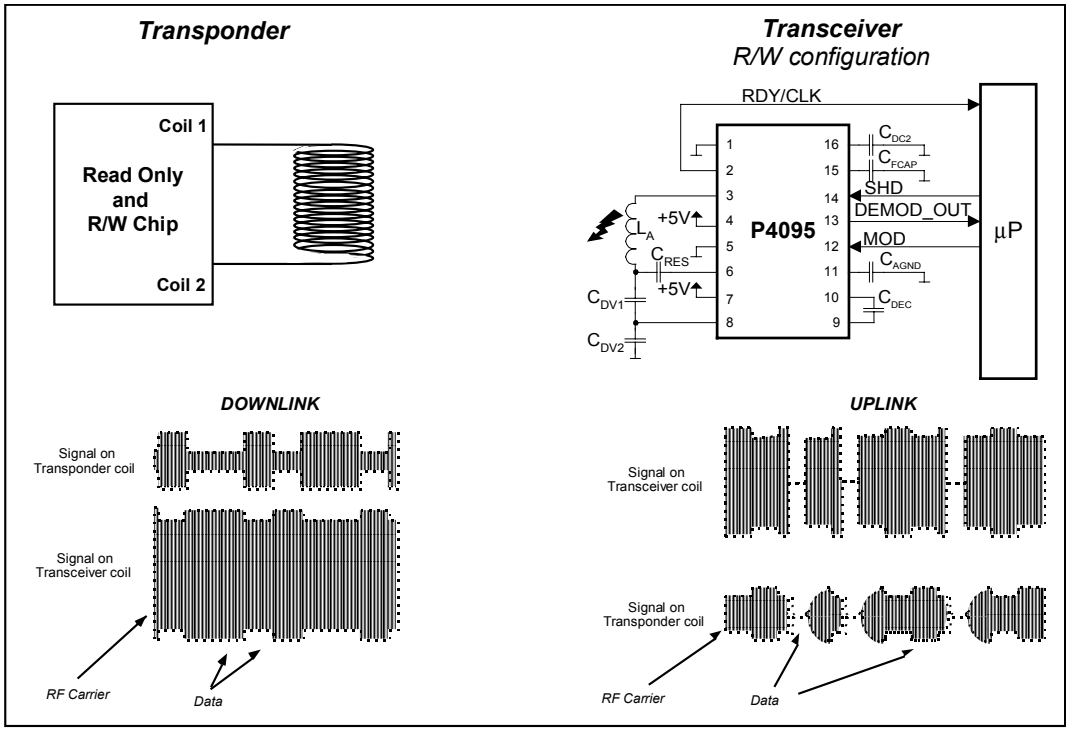
Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating junction temperature	T_J	-40		+110	°C
Supply voltage	V_{DD}	4.1	5	5.5	V
Antenna circuit resonant frequency	F_{RES}	100	125	150	kHz
AC peak current on ANT1 and ANT2 pads	I_{ANT}			250	mA
C_{FCAP}		*	10	*	nF
C_{DEC}		*	100	*	nF
C_{DC2}		*	6.80	*	nF
C_{AGND}		100		220	nF
Package thermal resistor SO16	R_{Th}**	69	70	71	°C/W

* ±10% tolerance capacitors should be used
** According to 1S2P JEDEC test board

Due to antenna driver current the internal junction temperature is higher than ambient temperature. Please calculate ambient temperature range from max. antenna current and package Thermal Resistor. It is the user's responsibility to guarantee that T_J remains below 110°C.
Supply voltage (V_{DD} and DV_{DD} pads) must be blocked by a 100nF capacitor (to V_{SS}) as close as possible to the chip.

System principle



Electrical and Switching Characteristics:

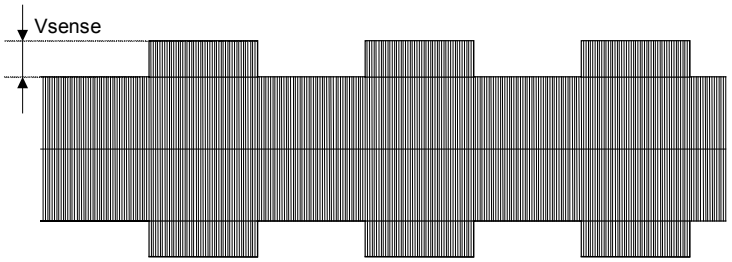
Parameters specified below are valid only in case the device is used according to Operating Conditions defined on previous page.

VSS=DVSS=0V, VDD=DVDD = 5V, Tj = -40 to 110°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply current in sleep mode	$I_{DDsleep}$			1	2	µA
Supply current excluding drivers current	I_{DDon}			5	7	mA
AGND level	V_{AGND}	Note 1	2.35	2.5	2.65	V
Logic signals SHD, MOD, DEMOD_OUT						
Input logic high	V_{IH}		$0.8V_{DD}$			V
Input logic low	V_{IL}				$0.2V_{DD}$	V
Output logic high	V_{OH}	I_{SOURCE}=1mA	$0.9V_{DD}$			V
Output logic low	V_{OL}	I_{SINK}=1mA			$0.1V_{DD}$	V
MOD pull down resistor	R_{PD}	$0.2V_{DD}$	25	50	75	kΩ
SHD pull up resistor	R_{PU}	$0.8V_{DD}$	25	50	75	kΩ
PLL						
Antenna capture frequency range	F_{ANT_C}		100		150	kHz
Antenna locking frequency range	F_{ANT_L}		100		150	kHz
Drivers						
ANT drivers output resistance	R_{AD}	I_{ANT}=100mA		3	9	Ω
RDY/CLK driver output resistance	R_{CL}	$I_{RDY/CLK}$=10mA		12	36	Ω
AM demodulation						
DEMOD_IN common mode range	V_{CM}		V_{SS} + 0.5		V_{DD} - 0.5	V
DEMOD_IN input sensitivity	V_{sense}	Note 2		0.85	2	mVpp

Note 1: AGND is a P4095 internal reference point. Any external connection except specified capacitor to V_{SS} may lead to device malfunction.

Note 2: Modulating signal 2Khz square wave on 125 kHz carrier, total signal inside V_{CM}

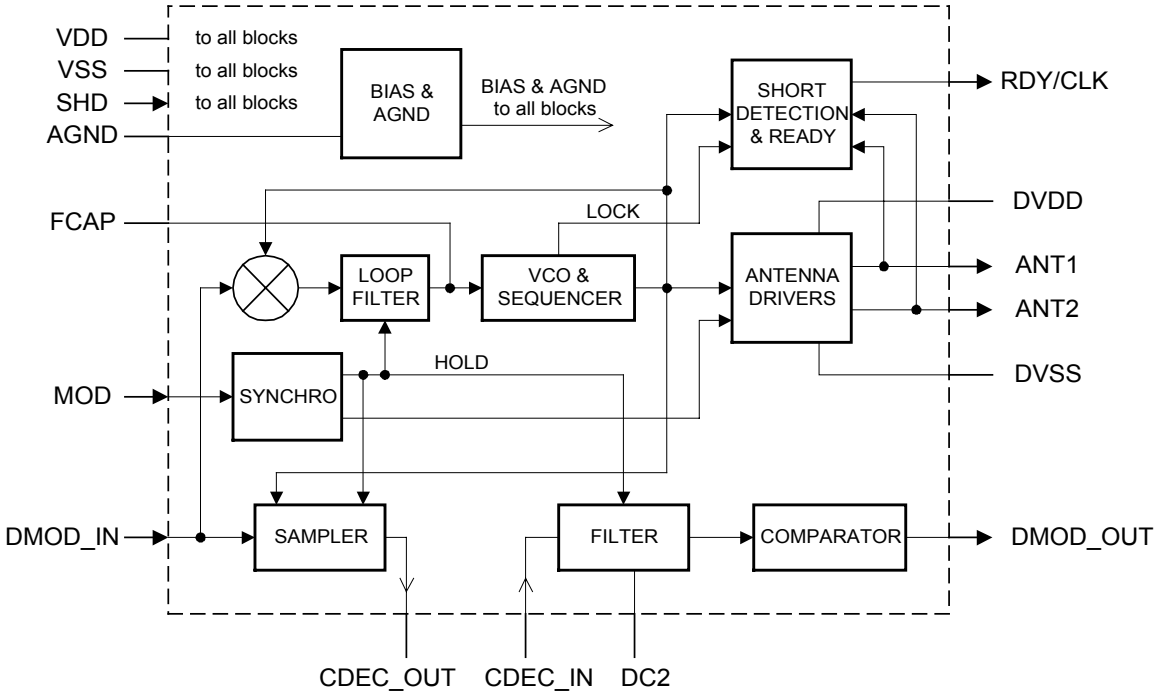


Timing Characteristics:
Parameters specified below are valid only in case the device is used according to Operating Conditions defined on previous page.
VSS=DVSS=0V, VDD=DVDD

Parameter	Symbol	Test Conditions	Typ	Max	Units
Set-up time after a sleep period	T_{set}		25	35	ms
Time from full power to modulation state	T_{mdon}	antenna circuit specifications: Q=15,F_{RES}=125Khz modulation index: 100%		50	µs
AM demodulation: Delay time from input to output	T_{pd}	Modulating signal 2Khz square wave 10mVpp	40	100	µs
Recovery time of reception after antenna modulation	T_{rec}	Note 1	400	500	µs

Note 1: RF period is time of one period transmitted on ANT outputs (at 125 kHz 8µs). T_{rec} after antenna modulation receiver chain is ready to demodulate. The condition is of course that the amplitude on antenna has already reached its steady state by that time (this depends on Q of antenna). See also Application Notes.

Block diagram



Pin Description

SO16 package

Pin	Name	Description	Type
1	VSS	Negative power supply (substrate)	GND
2	RDY/CLK	Ready flag and clock output, driver for AM modulation	O
3	ANT1	Antenna driver	O
4	DVDD	Positive power supply for antenna drivers	PWR
5	DVSS	Negative power supply for antenna drivers	GND
6	ANT2	Antenna driver	O
7	VDD	Positive power supply	PWR
8	DEMOD_IN	Antenna sensing voltage	ANA
9	CDEC_OUT	DC blocking capacitor connection « out »	ANA
10	CDEC_IN	DC blocking capacitor connection « in »	ANA
11	AGND	Analog ground	ANA
12	MOD	A High level voltage modulates the antenna	IPD
13	DEMOD_OUT	Digital signal representing the AM seen on the antenna	O
14	SHD	A High level voltage forces the circuit into sleep mode	IPU
15	FCAP	PLL Loop filter capacitor	ANA
16	DC2	DC decoupling capacitor	ANA

GND: reference ground PWR: power supply ANA: analog signal
IPD: input with internal pull down IPU: input with internal pull up O: output

Functional Description

General

The P4095 is intended to be used with an attached antenna circuit and a microcontroller. Few external components are needed to achieve DC and RF filtering, current sensing and power supply decoupling.

A stabilised power supply has to be provided. Please refer to P4095 Application Notes for advice.

Device operation is controlled by logic inputs SHD and MOD. When SHD is high P4095 is in sleep mode, current consumption is minimised. At power up the input SHD has to be high to enable correct initialisation. When SHD is low the circuit is enabled to emit RF field, it starts to demodulate any amplitude modulation (AM) signal seen on the antenna. This digital signal coming from the AM demodulation block is provided through DEMOD_OUT pin to the microcontroller for decoding and processing.

High level on MOD pin forces in tri-state the main antenna drivers synchronously with the RF carrier. While MOD is high the VCO and AM demodulation chain are kept in state before the MOD went high. This ensures fast recovery after MOD is released. The switching ON of VCO and AM demodulation is delayed by 41 RF clocks after falling edge on MOD. In this way the VCO and AM demodulation operating points are not perturbed by start-up of antenna resonant circuit.

Analog Blocks

The circuit performs the two functions of an RFID basestation, namely: transmission and reception. Transmission involves antenna driving and AM modulation of the RF field. The antenna drivers deliver a current into the external antenna to generate the magnetic field.

Reception involves the AM demodulation of the antenna signal modulation induced by the transponder. This is achieved by sensing the absorption modulation applied by the tag (transponder).

Transmission

Referring to the block diagram, transmission is achieved by a Phase Locked Loop (PLL) and the antenna drivers.

Drivers

The antenna drivers supply the reader basestation antenna with the appropriate energy. They deliver current at the resonant frequency which is typically 125 kHz. Current delivered by drivers depends on Q of external resonant circuit.

It is strongly recommended that design of antenna circuit is done in a way that maximum peak current of 250 mA is never exceeded (see Typical Operating Configuration for antenna current calculation). Another limiting factor for antenna current is Thermal Convection of package. Maximum peak current should be designed in a way that internal junction temperature does not exceed maximum junction temperature at maximum application ambient temperature. 100% modulation (field stop) is done by switching OFF the drivers. The ANT drivers are protected against antenna DC short circuit to the power supplies. When a short circuit has been detected the RDY/CLK pin is pulled low while the main driver is forced in tri-state. The circuit can be restarted by activating the SHD pin.

Phase locked loop

The PLL is composed of the loop filter, the Voltage Controlled Oscillator (VCO), and the phase comparator blocks. By using an external capacitive divider, pin DEMOD_IN gets information about the actual high voltage signal on antenna.
Phase of this signal is compared with the signal driving antenna drivers. Therefore the PLL is able to lock the carrier frequency to the resonant frequency of the antenna. Depending on the antenna type the resonant frequency of the system can be anywhere in the range from 100 kHz to 150 kHz. Wherever the resonant frequency is in this range it will be maintained by the Phase Lock Loop.

Reception

The demodulation input signal for the reception block is the voltage sensed on the antenna. DEMOD_IN pin is also used as input to Reception chain. The signal level on the DEMOD_IN input must be lower than VDD-0.5V and higher than VSS+0.5V. The input level is adjusted by the use of an external capacitive divider. Additional capacitance of divider must be compensated by accordingly smaller resonant capacitor. The AM demodulation scheme is based on the "AM Synchronous Demodulation" technique.

The reception chain is composed of sample and hold, DC offset cancellation, bandpass filter and comparator. DC voltage of signal on DEMOD_IN is set to AGND by internal resistor. The AM signal is sampled, the sampling is synchronised by a clock from VCO. Any DC component is removed from this signal by the C_{DEC} capacitor. Further filtering to remove the remaining carrier signal, high and low frequency noise is made by second order highpass filter and C_{DC2}. The amplified and filtered receive signal is fed to asynchronous comparator. Comparator output is buffered on output pin DEMOD_OUT.

Signal RDY/CLK

This signal provides the external microprocessor with clock signal which is synchronous with the signal on ANT1 and with information about P4095 internal

state. Clock signal synchronous with ANT1 indicates that PLL is in lock and that Reception chain operation point is set. When SHD is high RDY/CLK pin is forced low. After high to low transition on SHD the PLL starts-up, and the reception chain is switched on. After time T_{SET} the PLL is locked and reception chain operation point has been established. At this moment the same signal which is being transmitted to ANT1 is also put to RDY/CLK pin indicating to microprocessor that it can start observing signal on DEMOD_OUT and giving at the same time reference clock signal. Clock on RDY/CLK pin is continuous, it is also present during time the ANT drivers are OFF due to high level on MOD pin. During the time T_{SET} from high to low transition on SHD pin RDY/CLK pin is pulled down by 100 kΩ pull down resistor. The reason for this is in additional functionality of RDY/CLK pin in case of AM modulation with index which is lower then 100%. In that case it is used as auxiliary driver which maintains lower amplitude on coil during modulation. (see also Typical Operating Configuration)

Remark: Please refer to AN4095 for external components calculation and limits.

Typical Operating Configuration

Read Only Mode

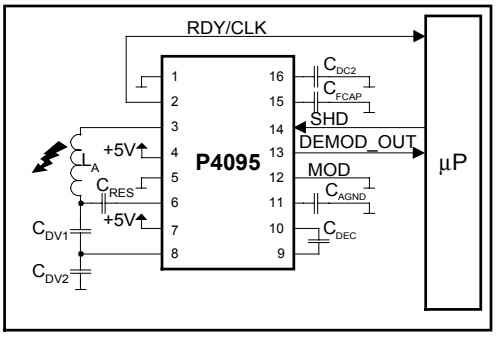


Figure 1

Read/Write mode (Low Q factor antenna)

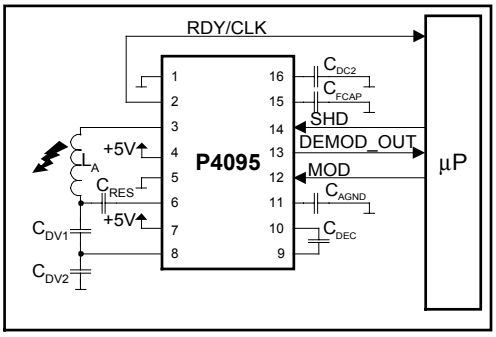


Figure 2

Read/Write mode (High Q factor antenna)

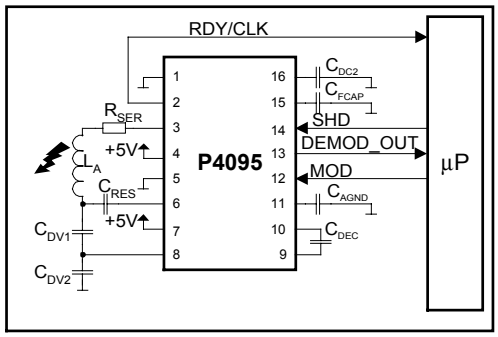


Figure 3

Read/Write mode (AM modulation)

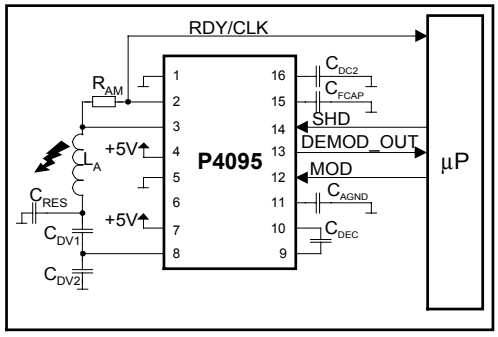


Figure 4

Figure 1 presents P4095 used in Read Only mode. Pin MOD is not used. It is recommended to connect it to VSS.

Figure 2 presents typical R/W configuration for OOK communication protocol reader to transponder (eg. P4150). It is recommended to be used with low Q factor antennas (up to 15).

When the antenna quality is high using configuration of figure 1 or 2 the voltage on antenna can arrive in the range of few hundred volts and antenna peak current may exceed its maximum value. In such a case the capacitive divider ratio has to be high thus limiting the sensitivity. For such case it is better to reduce antenna circuit quality by adding serial resistor. In this way the antenna current is lower and thus power dissipation of IC is reduced with practically the same performance (Figure 3).

In the case AM modulation communication protocol reader to transponder (eg. P4069) is needed a single ended configuration has to be used (figure 4). When pin MOD is pulled high driver on ANT1 is put in three state, driver RDY/CLK continues driving thus maintaining lower antenna current. Modulation index is adjusted by resitor R_{AM}. As mentioned above RDY/CLK signal becomes active only after the demodulation chain operating point is set.
Before it is pulled down by high impedance pull down resistor (100 kΩ) in order not to load ANT1 output. In the case of AM modulation configuration the total antenna current change at the moment RDY/CLK pin becomes active, so external microprocessor has to wait another T_{SET} before it can start observing DEMOD_OUT.

Read Only mode with external peak detector

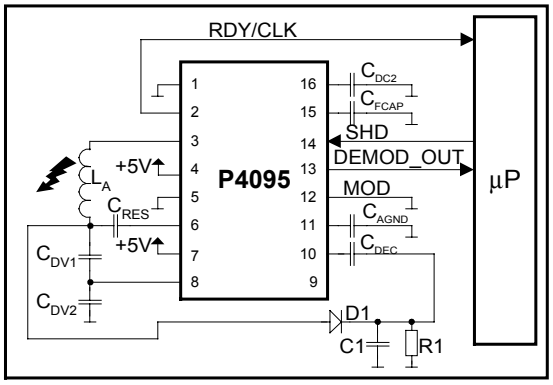


Figure 5

Read/Write mode with external peak detector

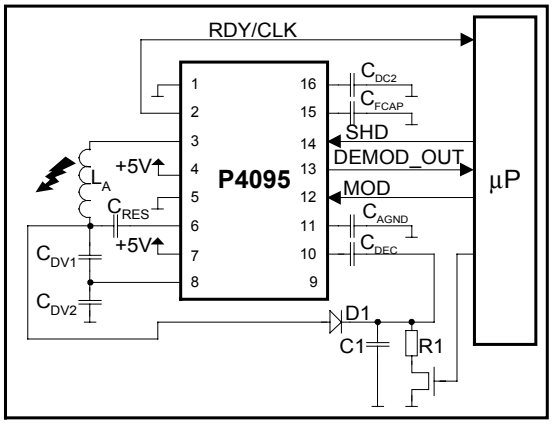


Figure 6

As mentioned above for high Q antennas the voltage on antenna is high and read sensitivity is limited by demodulator sensitivity due to capacitive divider. Read sensitivity (and thus reading range) can be increased by using external envelope detector circuit. Input is taken on antenna high voltage side output is directly fed to CDEC_IN pin. However, the capacitor divider is still needed for PLL locking. Such configuration is shown in figure 5, the envelope detector is formed by three components: D1, R1 and C1.

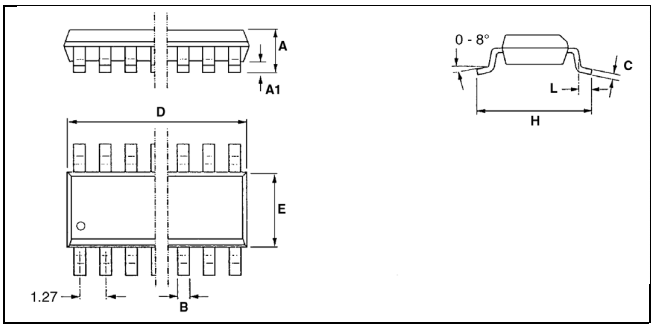
The configuration presented in figure 5 may also be used for read write applications but it has a drawback in the case fast recovery of reading is needed after communication reader to transponder is finished. The reason is in fact that DC voltage after diode D1 is lost during modulation and it takes very long time before it is established again.

Figure 6 presents a solution to that problem. A high voltage NMOS transistor blocks the discharge path during modulation, so operating point is preserved. The signal controlling NMOS gate has to be put low synchronously with signal MOD, but it can be put high only after the amplitude on antenna has recovered after modulation.

PCB Layout
Refer to "P4095 Application Note".

Package and Ordering Information

Dimensions of SOIC 16 Package (table in millimeters)



	Common Dimensions		
Symbol	**Min**	**Nom**	**Max**
A	1.55	1.63	1.73
A1	0.127	0.15	0.25
B	0.35	0.41	0.49
C	0.19	0.20	0.25
D	9.80	9.93	9.98
E	3.81	3.94	3.99
H	5.84	5.99	6.20
L	0.41	0.64	0.89

Figure 7

Ordering Information

The P4095 is available in the following package:

Type	**Package**
P4095-16S	SOIC 16-150

When ordering, please specify complete part number.

Appendix

Equations

Antenna resonant frequency f_0:

$$f_0 = \frac{1}{2\pi\sqrt{L_A C_0}} \qquad (1)$$

Where C_0 is resonant capacitor composed of C_{RES}, C_{DV1} and C_{DV2}:

$$C_0 = C_{RES} + \frac{C_{DV1} * C_{DV2}}{C_{DV1} + C_{DV2}} \qquad (2)$$

Usually antenna coil is specified by its inductance (L_A) and Q factor (Q_A). Serial resistance of antenna is defined by following equation:

$$R_{ANT} = \frac{2\pi f_0 L_A}{Q_A} \qquad (3)$$

The equations which follow are valid for bridge configuration as defined on Figures 1, 2 and 3. For figures 1 and 2 R_{SER} has to be considered 0.

The AC current amplitude at resonant frequency is defined as follows:

$$I_{ANT} = \frac{4}{\pi} \frac{V_{dd} - V_{ss}}{R_{ANT} + R_{SER} + 2R_{AD}} \qquad (4)$$

RMS antenna current (important for power dissipation calculation):

$$I_{RMS} = \frac{I_{ANT}}{\sqrt{2}} \qquad (5)$$

Peak to peak voltage on antenna is defined by following equation:

$$V_{ANTpp} = \frac{I_{ANT}}{\pi f_0 C_0} \qquad (6)$$

To ensure correct operation of the AM demodulation chain, the AC peak to peak voltage on DEMOD_IN pin (V_{DMOD_INpp}) has to be inside common mode range. Once peak to peak voltage on antenna is known the capacitor divider division factor can be calculated:

$$V_{DMOD\_INpp} = V_{ANTpp} \frac{C_{DV1}}{C_{DV1} + C_{DV2}} \qquad (7)$$

Power dissipation is composed of power dissipated on ANT drivers and internal power consumption:

$$P = 2 \cdot I_{RMS}{}^2 \cdot R_{AD} + I_{DDon}\left(V_{DD} - V_{SS}\right) \qquad (7)$$

Temperature increase of die due to power dissipation is:

$$\Delta T = P \cdot R_{Th} \qquad (8)$$

Where R_{Th} is Package thermal resistor.

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