Multi Frequency Contactless Identification Device

Anti-Collision compatible with BTG's Supertag Category Protocols

Features

- Implements all BTG anti-collision protocols: Fast SWITCH-OFF and SLOW-DOWN, and FREE-RUNNING
- Can be used to implement low frequency inductive coupled transponders, high frequency RF coupled transponders or bi-frequency transponders
- Factory programmed 64 bit ID number
- Eight data rate options: 0.5 kbit/s to 64 kbit/s
- Eight maximum random delay options
- Two data encoding options
- Any field frequency: Typically 100 kHz, 13.5 MHz inductive and 100 MHz to 2.54 GHz RF
- Data transmission done by amplitude modulation
- 110 pF on-chip resonant capacitor
- On-chip rectifier and voltage limiter
- On-chip oscillator
- Low voltage operation - down to 1 V
- Low power consumption
- -40 to +85 ^{O}C temperature range

Description

The P4022 chip implements patented anti-collision protocols for both *high* frequency and *low* frequency applications. It is even possible to identify transponders with identical codes, thereby making it possible to count identical items. The chip is typically used in “passive” transponder applications, i.e. it does not require a battery power source. Instead, it is powered up by an electromagnetic energy field or beam transmitted by the reader, which is received and rectified to generate a supply voltage for the chip. A pre-programmed code is transmitted to the reader by varying the amount of energy that is reflected back to the reader. This is done by modulating an antenna or coil, thereby effectively varying the load seen by the reader.

Low frequency applications are those applications that can make use of the on-chip full wave rectifier bridge to rectify the incident energy. These are typically applications that use inductive coupling to transmit energy to the chip. The carrier frequency is typically less than 500 kHz. The design of the on-chip rectifier and resonance capacitor is optimized for frequencies in the order of 125 kHz. Low frequency transponders can be implemented using just a P4022 chip and an external coil that resonates with the on-chip tuning capacitor at the required carrier frequency. An external power storage capacitor can be added to improve reading range. Low frequency inductive coupled applications typically have lower reading distances and lower data rates (4 kbit/s or 8 kbit/s @ 125 kHz). Reading rates of 30 transponders per second at 4 kbit/s can be attained.

High frequency applications are those applications that cannot make use of the on-chip rectifier to rectify the incident energy. Instead, external microwave Schottky diodes are required to rectify the carrier wave. These are typically applications that use electromagnetic RF coupling to transmit energy to the chip using carrier frequencies greater than 100 MHz. High frequency transponders can be implemented using a P4022 chip, one to three microwave diodes and a printed antenna. An external power storage capacitor can be added to improve reading range. High frequency RF coupled applications typically have higher reading distances (> 4 m) and higher data rates (64 kbit/s). Reading rates of 480 transponders per second at 64 kbit/s can be attained.

It is also possible to implement transponders that work in both high and low frequency applications (bi-frequency transponders).

Applications

- Access control
- Asset control
- Licensing
- Auto-tolling
- Animal tagging
- Sports event timing
- Electronic keys

Typical Operating Configurations

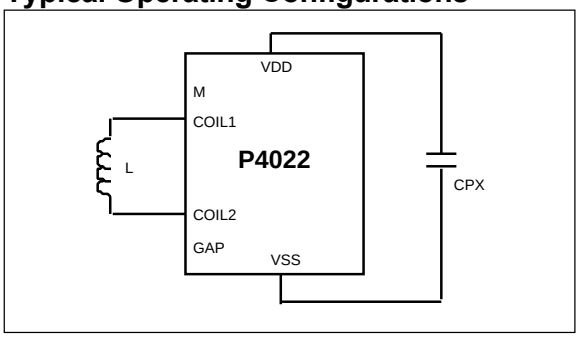

Figure 1: Low frequency inductive transponder implementation.

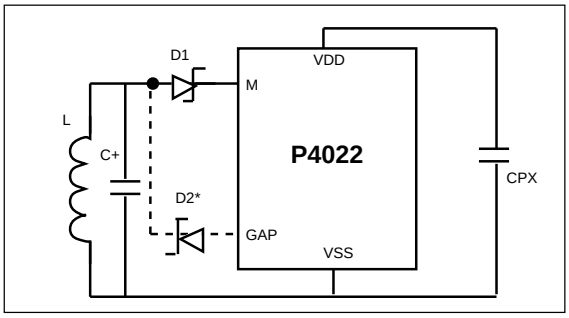

Figure 2: Medium frequency (13.56 MHz) inductive transponder implementation. D2 is optional.
L: coil antenna (typical value 1.2 µH).
C+: tuning capacitor (typical value 110 pF)

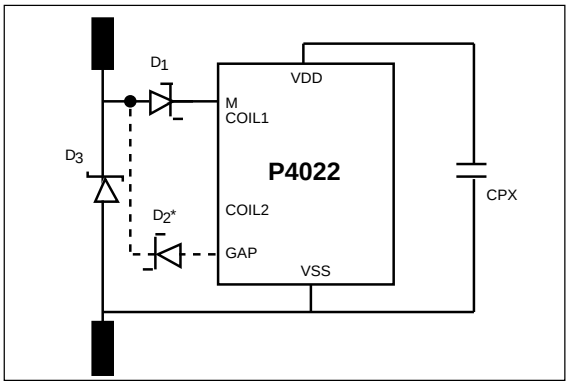

Figure 3: High frequency RF transponder implementation. D2 is optional.

Pin Assignment

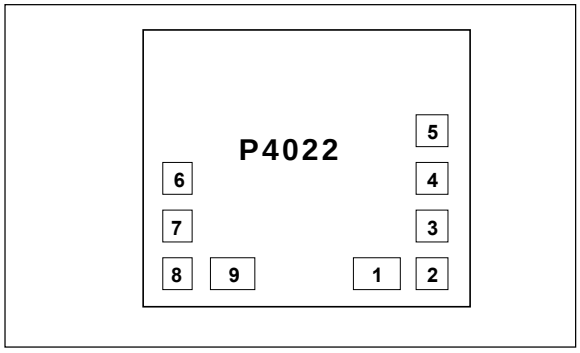

Figure 4: Pin Assignment

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak current induced on COIL1 and COIL2	I_{COIL}	± 50 mA
Maximum DC voltage induced between M and V_{SS} 1)	V_M	4.5 V
Maximum DC current supplied into M 1)	I_M	50 mA
Power supply	$V_{DD} - V_{SS}$	-0.3 to 3.5 V
Max. voltage other pads	V_{max}	V_{DD} + 0.3 V
Min. voltage other pads	V_{max}	V_{SS} - 0.3 V
Storage temperature	T_{STORE}	-55 to +125 °C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	1000 V

1) whatever is reached first

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all the terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature	T_A	-40		+85	^{O}C
Maximum coil current	I_{COIL}			50	mA
AC voltage on coil*	V_{COIL}			8	V_{pp}
DC voltage on M*	V_M			3.5	V

Table 2

* The AC voltage on the coil and the DC voltage at pad M are limited by the on-chip shunt regulator.

Electrical Characteristics

V_{SUPPLY} between 1.2 and 3.0 V, T_A = 25 ^{O}C, unless otherwise specified.

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
Supply voltage (VDD – VSS)	V_{SUPPLY}		1.2		3.5	V
Oscillator frequency	F_{OSC}	V_{SUPPLY} between 1.2 and 3.0 V	110	128	140	kHz
Power-on reset threshold	V_{PONR}	V_{SUPPLY} rising	0.7	1.2	1.6	V
Power-on reset threshold	V_{PONF}	V_{SUPPLY} falling	0.5	1.0	1.4	V
Power-on reset hysteresis			130	200	270	mV
GAP input time constant	T_{GAP}			0.2		µs
Modulation transistor ON resistance	R_{ON}				40	Ω
Resonance capacitor	CR		106.7	110	113.3	pF
Total current consumption from CP	I_{TFREE}	FREE-RUNNING mode, V_{SUPPLY} = 1.2 V		2.6		µA
Total current consumption from CP	I_{TFREE}	FREE-RUNNING mode, V_{SUPPLY} = 3 V		10		µA
Total current consumption from CP	I_{TGAP}	GAP enabled, V_{SUPPLY} = 1.2 V		14		µA
Total current consumption from CP	I_{TGAP}	GAP enabled, V_{SUPPLY} = 3 V		40		µA
Total current consumption from CP	I_{TDEAD}	SWITCHED-OFF state, V_{SUPPLY} = 1.2 V		15		µA
Total current consumption from CP	I_{TDEAD}	SWITCHED-OFF state, V_{SUPPLY} = 3 V		60		µA

Table 3

Current Consumption

The total typical current consumption from the storage capacitor CP in various modes is shown in Table 4 below.

The total current consumption in conjunction with the size of the power storage capacitance determines the maximum time that transistor Q2 can be turned on and Q1 turned off, before the supply voltage drops below 1 V, thereby resulting in the power-on reset block resetting the chip. This in turn determines the minimum data bit rate and maximum range. Similarly the total storage capacitance and total current determine the maximum unpowered SWITCHED-OFF state time.

The second column shows the current drawn in FREE-RUNNING mode. The third column shows the current drawn for the bi-directional protocols, which includes the current drawn by the GAP input pull-up. The fourth column shows the total current drawn in SWITCHED-OFF state. In this mode both the GAP input and the shunt regulator draws current from the storage capacitor.

Supply (V)	Current (Free) (µA)	Current (Bi-directional) (µA)	Current (SWTICHED-OFF state) (µA)
1.0	1.8	2.2	2.8
1.2	2.6	3.6	4.6
1.5	3.8	6.3	8.3
2.0	6	13	16
3.0	11	31	51

Table 4

Table 5 below shows the theoretical storage capacitance required for various applications. For free-running applications, the capacitance required is determined by the data bit rate and encoding method. Only the Logic, PON and oscillator draw current in Free-running applications. For the bi-directional protocols, the GAP input pull-up also draws current during modulation.

Data bit rate (kbit/s)	En-coding	Free-running (pF)	Bi-direc-tional (pF)	Counting (µF)
4	Man	2700	3600	20
4	Glitch	670	900	20
64	Man	170	240	20
64	Glitch	40	80	20

Table 5

For counting applications (SWITCH-OFF BTG-Supertag) the required unpowered time in the SWITCHED-OFF state determines the size of the capacitor. *In applications where the chip can be guaranteed to stay powered, the capacitor size is determined by the data bit rate*.

It should be noted that the on-chip capacitance is sufficient for free-running applications at 64 kbit/s, while inductive applications at 4 kbit/s require a few nanofarad externally. Unpowered counting applications will require more than 20 µF to achieve 1 second unpowered time in the SWITCHED-OFF state.

Timing Characteristics

1) All timings are derived from the on-chip oscillator, which can vary by 30%.

2) The minimum *low frequency* GAP width for a single chip is 1 bit at its own clock frequency. The reader must however allow for the 30% spread in clock frequencies possible in a group of tags. Therefore the minimum width of the GAP in MUTE and WAKE-UP signals must be 1.5 bits. High frequency GAPs can be arbitrarily narrow (specified as minimum 50 ns).

3) The maximum GAP width for a single chip is 6 bits at its own clock frequency. The reader must however allow for the 30% spread in clock frequencies possible in a group of tags. Therefore the maximum width of the GAP in MUTE and WAKE-UP signals must be 5 bits.

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
High frequency GAP width	T_{HFGAP}		50			ns
High frequency ACK GAP width	T_{HFGAP}				6	bit
High frequency MUTE and WAKE-UP GAP width	T_{HFGAP}				5	bit
Low frequency ACK GAP width	T_{LFGAP}		1.0		6	Bit
Low frequency MUTE and WAKE-UP GAP width	T_{LFGAP}		1.5		5	Bit
GAP separation in WAKE-UP signal			1.5		5	Bit

Table 6

Anti-collision Protocol Overview

The protocols are a collection of simple but fast and reliable anti-collision protocols. They allow fast reading of large numbers of transponders simultaneously using a single reader. It is even possible to identify transponders with identical codes, thereby making it possible to count identical items.

Free-running protocol

The basis of the BTG-Supertag series of protocols is that transponders transmit their own codes at random times to a reader. By just listening and recording unique codes when they are received, the reader can eventually detect every tag. The reader detects collisions by typically checking a CRC. This basic protocol is known as the "Free-running" protocol. It requires uniquely coded tags. Its main advantage is that the reader design is simple, and the spectrum requirement is much less – a very narrow band is required.

Bi-directional protocols

Allowing bi-directional communication between reader and transponders can speed up the basic free-running protocol. Communication from the reader to transponders is achieved by turning the illuminating energy field off for short periods. The transponders detect these *gaps* in the energy transmission and interpret them as required.

Switch-off and Slow-down Modes

Reducing the effective population of transmitting transponders in the reader field can speed up the free-running protocol. One method to achieve this is by either switching transponders off or slowing them down once they have been detected. To achieve this, the reader sends an ACK signal to a transponder after its code has been successfully received. The transponder then either switches off completely or reduces its repeat rate until it is powered down. This reduces the number of collisions between transponder transmissions, thereby reducing the time required to read a group of tags. The Switch-off protocol's main advantage is that identical transponders can be counted.

In the P4022 the ACK signal is implemented as two consecutive *gaps* with the appropriate timing and received at a specific time after a code has been transmitted.

Fast Mode

A second method of speeding up the reading of tags, is to inhibit other transponders from transmitting while one transponder is transmitting. This is done by sending a MUTE signal to all the transponders when the start of a transmission is detected. The transponders stay muted long enough to allow the transmission of one code. This allows the transponder that has started transmitting to complete its transmission without any collisions. The other transponders continue

with their own protocols automatically after a time out, or continue immediately upon detection of an ACK signal indicating that the transmission which caused the MUTE has been completed.

In the P4022 the MUTE signal is implemented as a single *gap* received while the transponder is not transmitting.

Protocol combinations

The FREE-RUNNING and the two basic bi-directional protocols, SWITCH-OFF and SLOW-DOWN, can all be combined with the Fast protocol to give six different protocols, i.e. Normal FREE-RUNNING, Normal SLOW-DOWN, Normal SWITCH-OFF, Fast FREE-RUNNING, SLOW-DOWN, and Fast SWITCH-OFF.

The following should be noted about the different protocols:

1) The SWITCH-OFF protocols must be used for counting applications.
2) All the protocols except the SWITCH-OFF protocols have built in redundancy because of the fact that they can transmit a code more than once.
3) Normal FREE-RUNNING is the only uni-directional protocol. It has the lowest power spectrum requirement because the reader transmits a CW wave.
4) Fast SWITCH-OFF and Fast SLOW-DOWN are the fastest protocols, and should be used where speed is important, or where the data rate limits the reading rate. Fast SLOW-DOWN is slightly slower, but theoretically has a lower error rate.
5) For 125 kHz inductive applications using a 4 kbit/s data rate, Fast SLOW-DOWN is probably the best overall protocol.
6) For RF applications using a 64 kbit/s data rate, normal FREE-RUNNING protocol is probably the best protocol.

Reader determined protocols

If the reader does not send MUTE signals to transponders that were programmed for one of the FAST protocols, the protocol merely reverts to the equivalent normal protocol. Similarly, if the reader does not send ACK signals to transponders that were programmed for SLOW-DOWN or SWITCH-OFF, the protocol reverts to a FREE-RUNNING protocol. In this manner, the reader can determine the protocol that is used.

Note, however, that unless a transponder was specifically programmed for the FREE-RUNNING protocol, its GAP input must be pulled down. This happens automatically in low frequency inductive applications, where the GAP input is pulled down by the internal GAP detector diode. In RF applications, however, the GAP input will have to be pulled down explicitly. This will consume extra current.

Protocol saturation

As the number of transponders in a reader beam is increased, the number of collisions increase, and it takes longer to read all the tags. This process is not linear. To read twice as many transponders could take more than twice as long. This effect is called protocol *saturation*.

The normal FREE-RUNNING protocol saturates the easiest of all the protocols, because it does not have any means of reducing the transmitting population. The Fast protocols, on the other hand, are virtually immune against saturation, as they prevent collisions by muting all transponders except the transmitting one.

One way of delaying the onset of saturation, is to reduce the initial repeat rate (not data rate) at which transponders transmit their codes. This is done by increasing the maximum random delay between transmissions. Seven different settings are available from 16 bits to 64 kbits. A higher setting means it will take longer to read a small number of tags, but it will take a larger number of transponders to saturate the communication channel.

Table 7 below compares reading times at 4 kbit/s vs. the number of transponders in a group. In each case the repeat delay was optimised for a group of 30 transponders.

	Time (s)				
No of transponders	**3**	**10**	**30**	**100**	**300**
Free-running	3.1	5.8	10.8	49.3	-
Slow-down	0.86	1.8	5.8	89	-
Switch-off	0.79	1.5	3.4	34	-
Fast Free-running	0.30	0.78	2.9	21	690
Fast Slow-down	0.27	0.55	1.4	6.2	33
Fast Switch-off	0.26	0.49	1.0	3.3	13

Table 7

Reading rates

Table 8 below compares reading times at 4 kbit/s for the six protocols. The optimum repeat delay setting was chosen in each case. Reading rate is linear with data bit rate. At a bit rate of 64 kbit/s, the reading rates are 16 times faster than at 4 kbit/s.

	Time (s)			
Data rate (kbit/s)	**4**		**64**	
No of tags	**5**	**30**	**5**	**30**
Free-running	0.39	10.8	0.022	0.58
Slow-down	0.35	5.8	0.019	0.32
Switch-off	0.29	3.4	0.017	0.19
Fast Free-running	0.18	2.9	0.010	0.15
Fast Slow-down	0.11	1.4	0.007	0.084
Fast Switch-off	0.085	1.0	0.007	0.060

Table 8

Optimum repeat delay settings

Table 9 lists the optimum repeat delay settings for each of the protocols vs. number of transponders in a group.

Protocol	**Number of tags**			
	3	**10**	**30**	**100**
Free-running	1k	4k	16k	64k
Slow-down	1k	1k	4k	16k
Switch-off	1k	1k	4k	16k
Fast Free-running	256	1k	1k	4k
Fast Slow-down	256	256	1k	1k
Fast Switch-off	256	256	1k	1k

Table 9

Functional description

Block diagram

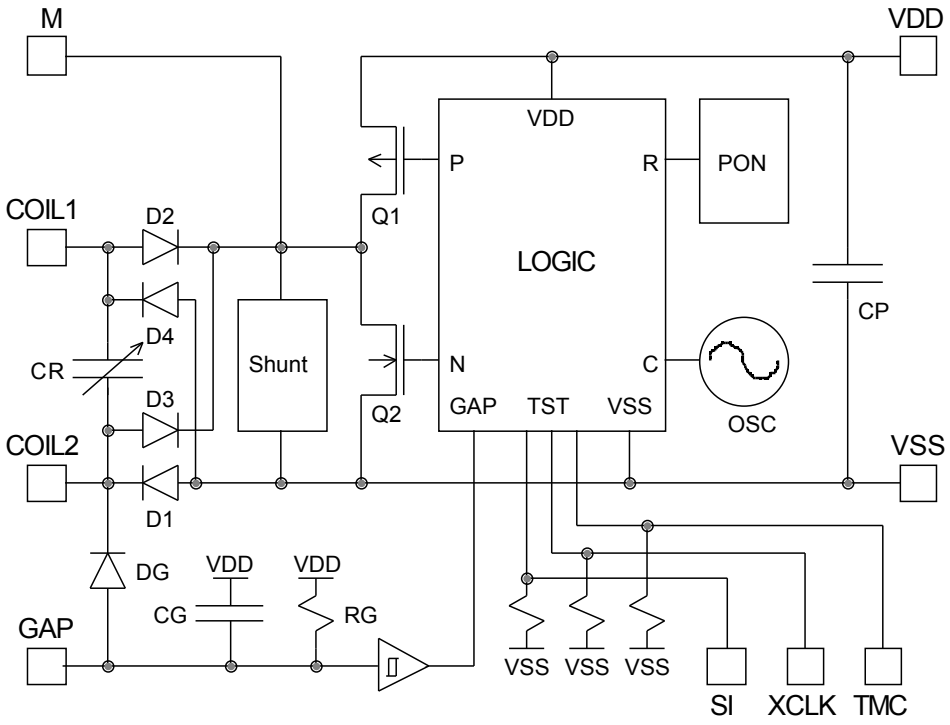

Figure 4: P4022 Block diagram

Resonance capacitor

The resonance capacitor CR has a nominal value of 110 pF and is trimmed to ± 3%. For resonance at 125 kHz an external 14.7 mH coil is required. At 13.65 MHz the required coil inductance drops to 1.2 µH.

Rectifier bridge

Diodes D1-D4 form a full wave rectifier bridge. They have relatively large forward resistances (100 -200 Ω). This is quite sufficient at 128 kHz, where the output impedance of the tuned circuit is high, but at 13.5 MHz the diode resistance becomes significant and external diodes have to be used to bypass the internal ones. The diode resistance affects the rate at which the power capacitor CP can be charged. It also affects the modulation depth that can be achieved.

Shunt regulator

The shunt regulator has two functions. It limits the voltage across the logic and in high frequency applications it limits the voltage across the external microwave Schottky diodes, which typically have reverse breakdown voltages less than 5 V.

The shunt regulator draws less than 500 nA at 1 V. Its maximum current shunt capability is 50 mA at 3.5 V.

Oscillator

The on-chip RC oscillator has a centre frequency of 128 kHz and a spread of 30% over the full temperature and supply range.

Power-on reset (PON)

The reset signal keeps the logic in reset when the supply voltage is lower than the threshold voltage. This prevents incorrect operation and spurious transmissions when the supply voltage is too low for the oscillator and logic to work properly. It also ensures that transistor Q2 is off and transistor Q1 is on during power-up to ensure that the chip starts up.

Modulation transistor

The N channel transistor Q2 is used to modulate the transponder coil or antenna. When it is turned on it loads the antenna or coil, thereby changing the load seen by the reader antenna or coil, and effectively changing the amount of energy that is reflected to the reader. It has an on resistance of typically less than 40 Ω. The on resistance affects the depth of modulation, especially at higher carrier frequencies (> 10 MHz), where the coil or antenna impedance can be lower than 200 Ω.

Charge preservation transistor

The P channel transistor Q1 is turned off whenever the modulation transistor Q2 is turned on to prevent Q2 from discharging the power storage capacitor. This is done in a non-overlapping manner, i.e. Q1 is first turned off before Q2 is turned on, and Q2 is turned off before Q1 is turned on.

Gap detection

Poly-silicon diode DG is used to detect a gap in the illuminating field. It is a minimum sized diode with forward resistance in the order of 2 kΩ. The low pass filter shown diagrammatically as CG and RG actually consists of a pull-up transistor (approximately 100 kΩ) in conjunction with the parasitic capacitance of the GAP input pad (approximately 2 pF). The effective time constant is in the order of 0.2 µs.

Through the diode the GAP input will be pulled low during each negative going cycle of the carrier. When the carrier is switched off, the GAP input will be pulled high by the pull-up transistor.

At very high carrier frequencies (> 100 MHz) the carrier will be filtered out, so that the GAP input will be low continuously when the carrier is present. When the carrier disappears, the GAP input will go high with the time constant of the low pass filter. At very low frequencies the GAP input will go high and low at each cycle of the carrier, and will stay high when the carrier disappears. To detect the gap, the logic must check for a high period longer than the maximum high period of the carrier.

As the rise and fall times of the GAP can be slow, a Schmitt trigger is used to buffer the GAP input.

Power storage capacitor

A 94 pF power supply capacitor is included in the layout of the P4022. This is sufficient for 64 kbit/s applications, but 4 kbit/s applications will required an additional external storage capacitor.

LOGIC block

Depending on the state of the SI input at power-up, the P4022 either enters a test mode (SI = 1) or its normal operating mode (SI = 0). The SI pin is internally pulled down, so that it can be left open for normal operation.

After the power-on reset has disappeared, the chip boots by reading the SEED and CTL ROMs.

The chip then enters its normal operating mode, which basically consists of clocking a 16 bit timer counter with the bit rate clock until it compares with the number in the random number generator. At this point a code is transmitted with the correct preamble at the correct data rate and encoded correctly. The random number generator is clocked to generate a new pseudo random number, and the 16 bit counter is reset to start a new delay.

The width of the comparison between the 16 bit random number and the 16 bit delay count determines the maximum possible delay between transmissions (reading rate). Any one of eight maximum delay settings can be pre-programmed.

The basic free-running mode as described above can be modified by the reception of GAP (MUTE and ACK) signals, if these are enabled by the CTL bits.

If an ACK signal is received after transmission of a code, the chip either turns itself off completely or reduces the rate at which the delay counter is clocked, thereby slowing down the rate at which codes are transmitted.

If a MUTE signal is received while the chip is not transmitting, the current operation of the chip is interrupted for 128 clock periods, after which it continues normally. Reception of more MUTEs during the sleep state restarts the sleep state. The sleep state is also terminated by the reception of a WAKE-UP signal (an ACK signal to a chip which has just completed transmitting).

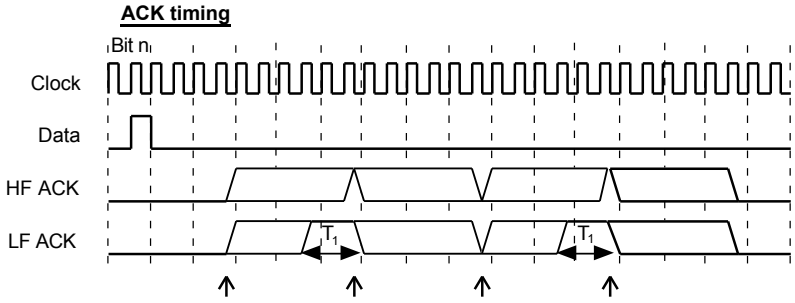

Figure 5: **ACK timing diagram**

GAP Detection Algorithm

The GAP detection logic contains two main controllers, one for detecting the ACK signal, and one for detecting the MUTE and WAKE-UP signals. The WAKE-UP signal is also called an asynchronous ACK, as it is really an ACK meant for another chip. It also contains a pre-processor for low frequency GAP signals.

Refer to the timing diagrams in Figure 5 and 6 for the following detailed description of the GAP detection algorithms.

ACK

The controller checks for a LOW 1.75 bit periods after the last bit of code has been transmitted. It then checks for a HIGH 3 bits later, a LOW 3 bits later and finally a HIGH a further 3 bits later.

The reader should synchronise itself to the frequency of the received code, check the CRC and then send two GAPs so that the above pattern is matched. Ideally to achieve the lowest error rate, the GAPS should be as narrow as possible and situated 4.75 and 7.75 bits after the last bit of code. In practice allowance must be made for the fact that the on-chip oscillator can drift in the

time between when the last code bit is transmitted and when the GAPs are expected. One reason for the drift is that the oscillator is supply voltage dependent, and the supply voltage will typically be rising during this time, since the transponder will not be modulating its coil or antenna.

The slope of the rising and falling edges of the GAPs can also be adjusted to reduce reader power bandwidth. In the case of high frequency GAPs the envelope is used directly. Low frequency GAPs have to be pre-processed. They are detected by checking for high periods lasting longer than one bit period. For this reason there is a set-up time of 1 bit. The minimum GAP width is therefore 1 bit period (T_1 in the timing diagram).

MUTE

The MUTE signal is received asynchronously by the transponder. The controller checks for a HIGH less than 7 bits wide after pre-processing (T_2 in the timing diagram). As in the case of the ACK, low frequency MUTE GAPs must be at least one bit wide, but high frequency GAPs can be arbitrarily narrow.

When transmitting a MUTE, the reader must take into account that there could be a spread of 30% in the clock frequencies of all the receiving transponders. The reader should therefor limit the width of a MUTE to be less than 5 bits of the nominal bit rate (T_4 in the timing diagram). A low frequency MUTE should also be wider than 1.5 bits of the nominal bit rate (T_3 in the timing diagram).

The MUTE should be sent as early as possible after a code transmission has been detected, while still making sure that it is a code transmission and not just noise. The earlier the MUTE is sent, the more time the reader has to recover before the SYNCH and code bits arrive, and the smaller the probability that another transponder has started a colliding transmission.

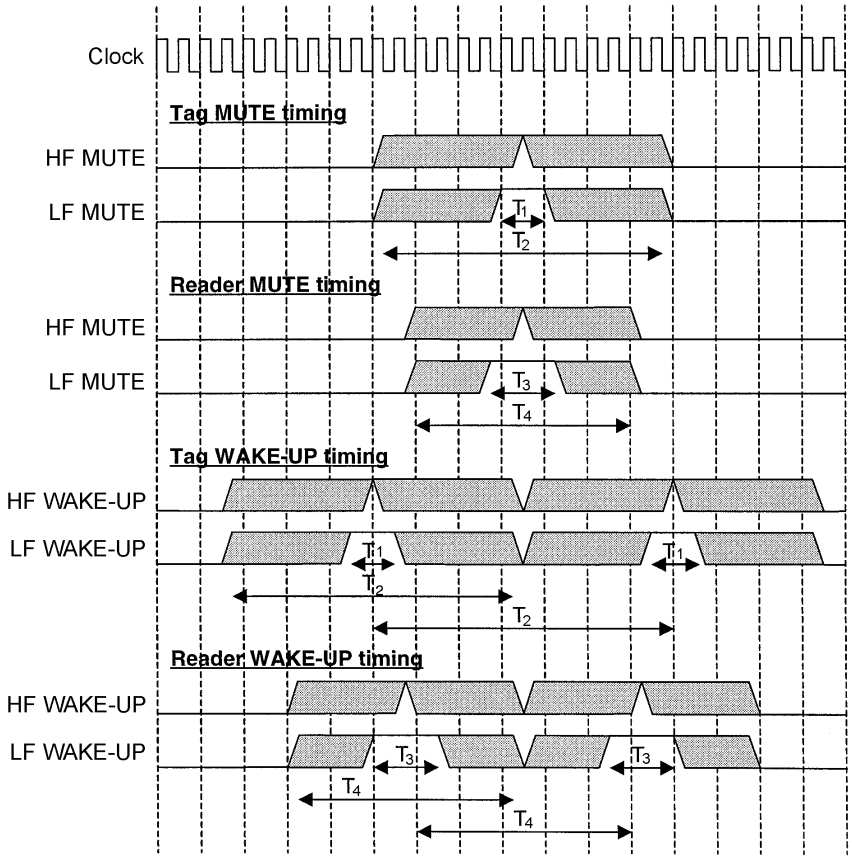

Figure 6: **MUTE and WAKE-UP timing diagrams**

WAKE-UP

An ACK sent after correct receipt of a code is interpreted by the other transponders in the field as a WAKE-UP. The ACK arrives synchronously at the transponder that has just transmitted, but asynchronously at all the other transponders. If necessary, a WAKE-UP can also be sent if the code is not received correctly, making sure that it will not be interpreted as an ACK by the transmitting transponder. This could speed up the protocol, but runs the risk of turning transponders off by accident.

To detect a WAKE-UP, the chip checks for two GAPs, less than 7 bits apart and each less than seven bits wide. As with the MUTE allowance must made for the 30% spread in clock frequencies. To be safely interpreted as a WAKE-UP, the GAPs should be sent less than 5 bits apart, and each should be less than 5 bits wide. This has an implication in the case of the high frequency ACK, which could theoretically consist of two very narrow GAPs 6 bits apart. In practice though, the GAPs will be typically at least one bit wide, making the separation five bits.

Like the MUTE, the low frequency ACK GAPs should be at least 1.5 bits wide to serve as a reliable WAKE-UP.

It should be noted that failure to reliably recognise WAKE-UPs is not critical. The protocol might be slowed down marginally, but will still work, as the chips time-out of the sleep mode automatically after 128 bits.

Data Encoder

The transmitted code always consists of an 11 bit preamble followed by the 64 code bits. The preamble consists of 8 start bits (ZEROES), followed by a SYNCH. The SYNCH consists of a LOW for two bit periods followed by a ONE.

The P4022 can be programmed for one of two data encoding methods. The first method is a variation on Manchester II, i.e. a ONE is represented by a HIGH in the first half of a bit period, and a ZERO is represented by a LOW in the first half of a bit period.

The second encoding method is called GLITCH encoding. A ONE is represented by a HIGH in the first quarter of the bit period, while a ZERO is represented by a HIGH in the third quarter of the bit period.

In GLITCH encoding the longest modulation period is one quarter of a bit period, compared to the Manchester encoding, where the longest modulation period is one full bit period. GLITCH encoding therefore requires a much smaller power storage capacitor.

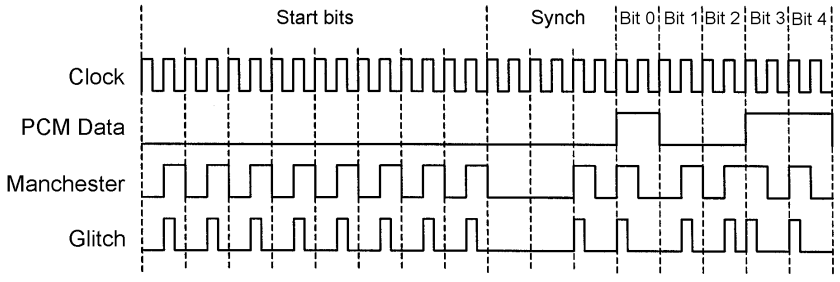

Figure 7: Data encoding methods

ROM programming

The P4022 contains three laser fuse ROM blocks that are pre-programmed by the foundry. Blowing a laser fuse writes a ZERO into the ROM bit.

CODE ID ROM

This ROM contains the 64 bit ID code. Unless otherwise specified, the foundry will automatically program a unique 48 bit ID and 16 bit CRC. In this case the most significant bit of the ID is programmed into bit 0 of the ROM, which will be transmitted first.

SEED ROM

The SEED ROM block contains the 16 bit control ROM. The 16 bit seed for the on-chip pseudo-random number generator is pre-programmed by the foundry into this ROM. This data is used internally and not transmitted.

CONTROL ROM

The operational modes of the P4022 are pre-programmed into the CONTROL ROM. It must be specified by the client as a 16 bit unsigned integer or two unsigned chars (bytes), as shown in Table 11. The programmable options are listed in Table 10. This data is used internally and not transmitted.

Control ROM Bit definition

Parameter	Value	Mode
Fast / Normal Mode	0	Normal
	1	Fast
Free-running	0	GAP detection enabled
	1	GAP disabled (Free-running)
ACK mode	0	Slow-down
	1	Switch-off
Maximum initial random delay	0	0 (Continuous)
	1	16 bits
	2	64 bits
	3	256 bits
	4	1 kbits
	5	4 kbits
	6	16 kbits
	7	64 kbits
Data rate	0	64 kbit/s
	1	32 kbit/s
	2	16 kbit/s
	3	8 kbit/s
	4	4 kbit/s
	5	2 kbit/s
	6	1 kbit/s
	7	0.5 kbit/s
Encoding method	0	Glitch encoding
	1	Manchester encoding
GAP type	0	Low frequency GAP detection
	1	High frequency GAP detection

Table 10

Control ROM Map

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte[1]								Byte[0]							
					HF GAP	Man-chester		Data rate		Random delay			Switch-off	Free-running	Fast

Table 11

Package and Ordering Information

Pad Description

Pad	Name	Function
1	COIL2	Coil terminal 2
2	V_{SS}	Negative internal supply voltage
3	GAP	GAP input
4	SI	Serial test data input (pull down)
5	TMC	Test mode control (pull down)
6	XCLK	External test clock (pull down)
7	V_{DD}	Positive internal supply voltage
8	M	Connection to external antenna
9	COIL1	Coil terminal 1

Table 12

Chip Size

57 x 69 mil

Configuration Examples

Application Parameters	Typical Practical Parameters	Configuration	CONTROL ROM Bits	External Capacitor
Inductive coupling, 125 kHz carrier, batches < 50 tags, 1 second per batch	Warehousing, asset control, sports event timing, mining, personnel tracking	Fast Slow-down, 8 kbits/s, Glitch encoding, 4 kbit delay	0x00E9	600 pF
Inductive coupling, 125 kHz carrier, batches < 5 tags 0.1 second per batch	Sports event timing, Conveyer belt, personnel tracking, auto-tolling	Fast Slow-dow, 8 kbit/s, Glitch encoding, 256 bit delay	0x00D9	600 pF
Inductive coupling, 125 kHz carrier, batches < 50 identical tags (counting), 1 second per batch guaranteed power	Warehousing	Fast Switch-off, 8 kbit/s Glitch encoding, 4 kbit delay	0x00ED	600 pF
Inductive coupling, 125 kHz carrier, batches < 50 identical tags (counting), 1 second per batch, 1 second unpowered	Warehousing	Fast Switch-off, 8 kbits/s, Glitch encoding, 4 kbit delay	0x00ED	20 µF
Inductive coupling, 125 kHz carrier, 1 tag at a time, 0.012 seconds per tag	Access control, conveyer belt	Free-running, 8 kbit/s, Glitch encoding, 16 bit delay	0x00CA	500 pF
RF coupling, 400-2540 MHz carrier, batch < 3 tags, 0.02 seconds per batch	Auto-tolling, sports event timing	Free-running, 64 kbit/s, Glitch encoding, 1 kbit delay	0x0022	none
RF coupling, 400-2540 MHz carrier, batch < 30 tags, 1 batch per second	Sports event timing, personnel tracking	Free-running, 64 kbit/s Glitch encoding, 16 kbit delay	0x0032	none
RF coupling, 400-2540 MHz carrier, batch < 200 tags 1 batch per second	Warehousing	Fast, Slow-down, 64 kbit/s, Glitch encoding, 4 kbit delay	0x0029	none