Spread-Compatible Low Skew Zero Delay Buffer

FEATURES

- Frequency Range 10MHz to 134 MHz
- Output Options:
  - 5 outputs PL123S-05
  - 9 outputs PL123S-09
- Zero input - output delay
- Optional Drive Strength:
  - Standard (8mA) PL123S-05/-09
  - High (12mA) PL123S-05H/-09H
- 3.3V, ±10% operation
- Available in Commercial and Industrial temperature ranges
- Available in 16-Pin SOP, SSOP or TSSOP (PL123S-09), and 8-Pin SOP (PL123S-05) packages
- Spread-compatible with spread-spectrum modulation clock inputs

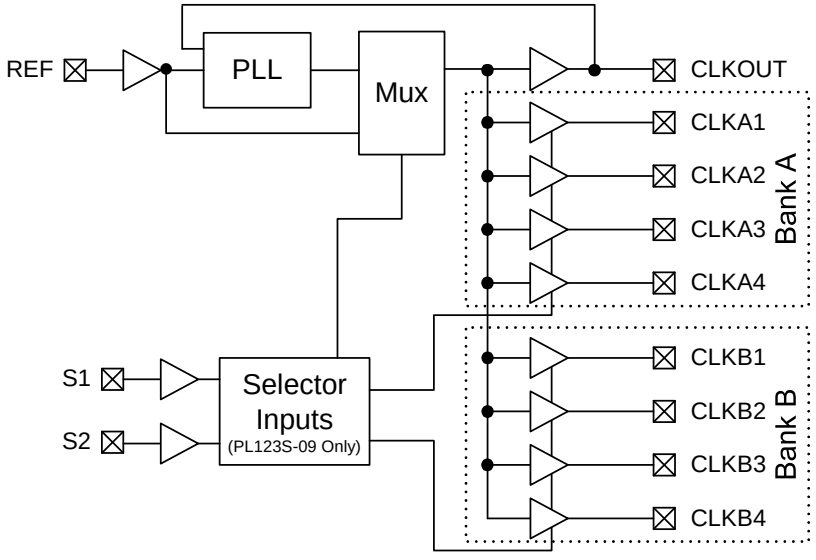
DESCRIPTION

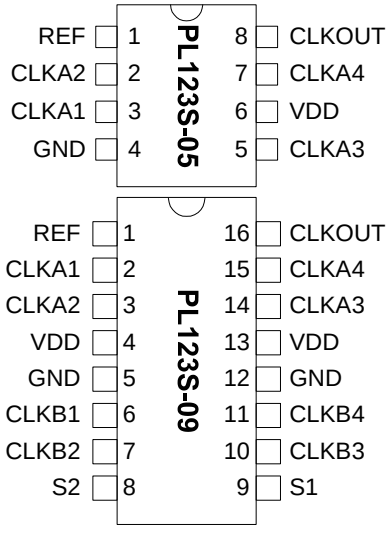
The PL123S-05/-09 (-05H/-09H for High Drive) are high performance, low skew, low jitter zero delay buffers designed to distribute high speed clocks. They have one (PL123S-05) or two (PL123S-09) low-skew output banks, of 4 outputs each, that are synchronized with the input. The PL123S-09 allows control of the banks of outputs by using the S1 and S2 inputs as shown in the Selector Definition table on page 2.

The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than ±100ps, the device acts as a zero delay buffer. The input output propagation delay can be advanced or delayed by adjusting the load on the CLKOUT pin.

These parts are not intended for 5V input-tolerant applications.

BLOCK DIAGRAM





PIN DESCRIPTIONS

Name	PL123S-09 TSSOP-16L, SOP-16L, SSOP-16L	PL123S-05 SOP-8L	Type	Description
REF[1]	1	1	I	Input reference frequency.
CLKA1[2]	2	3	O	Buffered clock output, Bank A
CLKA2[2]	3	2	O	Buffered clock output, Bank A
VDD	4,13	6	P	VDD connection
GND	5,12	4	P	GND connection
CLKB1[2]	6	-	O	Buffered clock output, Bank B
CLKB2[2]	7	-	O	Buffered clock output, Bank B
S2[3]	8	-	I	Selector input
S1[3]	9	-	I	Selector input
CLKB3[2]	10	-	O	Buffered clock output, Bank B
CLKB4[2]	11	-	O	Buffered clock output, Bank B
CLKA3[2]	14	5	O	Buffered clock output, Bank A
CLKA4[2]	15	7	O	Buffered clock output, Bank A
CLKOUT[2]	16	8	O	Buffered clock output. Internal feedback on this pin.

Notes: 1: Weak pull-down. 2: Weak pull-down on all outputs. 3: Weak Pull-Up on S1 and S2

SELECTOR DEFINITION FOR PL123S-09

S2	S1	CLOCK A1–A4 (Bank A)	CLOCK B1–B4 (Bank B)	CLKOUT	Output Source	PLL Shutdown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

INPUT / OUTPUT SKEW CONTROL

The PL123S-05/-09 will achieve Zero Delay from input to output when all the outputs are loaded equally. Adjustments to the input/output delay can be made by adding additional loading to the CLKOUT pin.
Please contact PhaseLink for more information.

SPREAD COMPATIBLE

Many products today utilize spread-spectrum modulation clocking to reduce electromagnetic interference (EMI) and pass FCC regulations. This product was designed to pass spread-spectrum input clock modulation frequencies to the output. When a buffer is not designed to pass spread spectrum, there will exist significant tracking jitter between input and output clocks, which may result in problems with system timing and synchronization.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

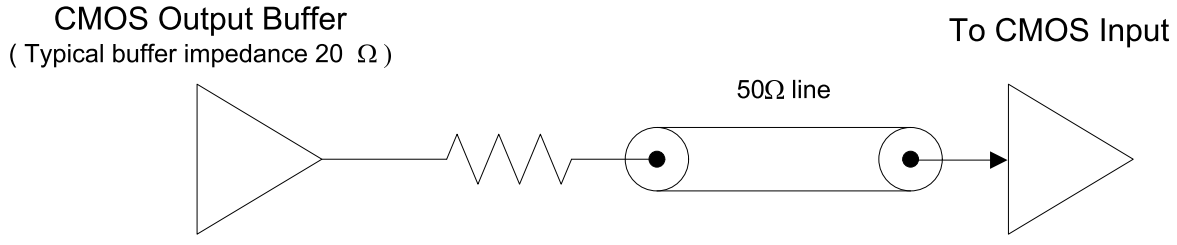
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Connect a 33 Ω series resistor at each of the output clocks to enhance the stability of the output signal

ABSOLUTE MAXIMUM CONDITIONS

Supply Voltage to Ground Potential ..... –0.5V to 4.6V
DC Input Voltage..... V_{SS} – 0.5V to 4.6V
Storage Temperature .....–65°C to 150°C
Junction Temperature…… 150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015)……> 2000V

OPERATING CONDITIONS

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Commercial Operating Temperature (ambient temperature)	0	70	°C
	Industrial Operating Temperature (ambient temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz	—	30	pF
	Load Capacitance, above 100 MHz	—	10	pF
C_{IN}	Input Capacitance	—	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	250	ms

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		–	0.8	V
V_{IH}	Input HIGH Voltage		2.5	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100	µA
V_{OL}	Output LOW Voltage[4]	I_{OL} = 8 mA I_{OL} = 12 mA	–	0.4	V
V_{OH}	Output HIGH Voltage[4]	I_{OH} = –8 mA I_{OL} = –12 mA	2.4	–	V
I_{DD}	Supply Current (Unloaded Outputs)	66.67MHz with unloaded outputs Commercial Temp.	–	32	mA
		66.67MHz with unloaded outputs Industrial Temp.	–	45	mA

Notes: 4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

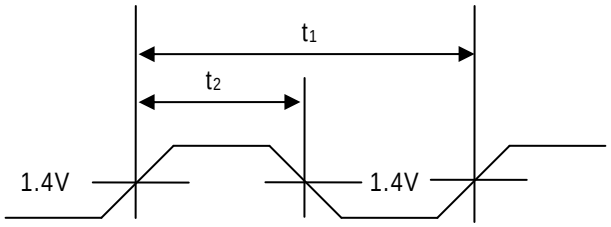
SWITCHING CHARACTERISTICS [5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load	10	–	100	MHz
		10-pF load	10	–	134	MHz
	Duty Cycle [4] = t2 ÷ t1	Measured at 1.4V, F_{OUT} = 66.67MHz	40	50	60	%
	Duty Cycle [4] = t2 ÷ t1	Measured at 1.4V, F_{OUT} <50MHz	45	50	55	%
t_3	Rise Time [4]	Measured between 0.8V and 2.0V	–	2.5	–	ns
	Rise Time [4] (High Drive)	Measured between 0.8V and 2.0V	–	1.5	–	ns
t_4	Fall Time [4]	Measured between 0.8V and 2.0V	–	2.5	–	ns
	Fall Time [4] (High Drive)	Measured between 0.8V and 2.0V	–	1.5	–	ns
t_5	Output to Output Skew	All outputs equally loaded	–	–	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge [4]	Measured at VDD/2	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge [4]	Measured at VDD/2. Measured in PLL bypass mode, PL123S-09 only.	1	5	8.5	ns
t_7	Device to Device Skew [4]	Measured at VDD/2 on the CLKOUT pin	–	0	700	ps
t_8	Output Slew Rate [4]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–	–	V/ns
t_J	Cycle to Cycle Jitter [4]	Measured at 66.67 MHz, loaded outputs	–	75	200	ps
t_{LOCK}	PLL Lock Time [4]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

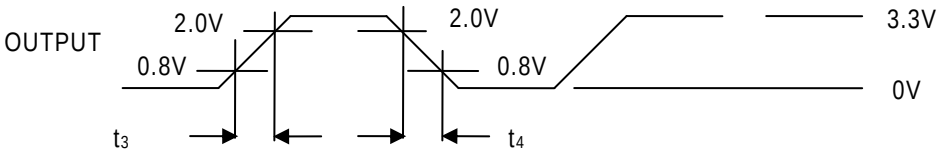
Notes:
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. All parameters are specified with loaded outputs.

SWITCHING WAVEFORMS

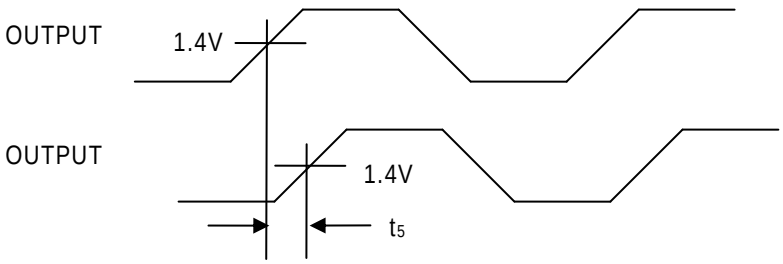
Duty Cycle Timing



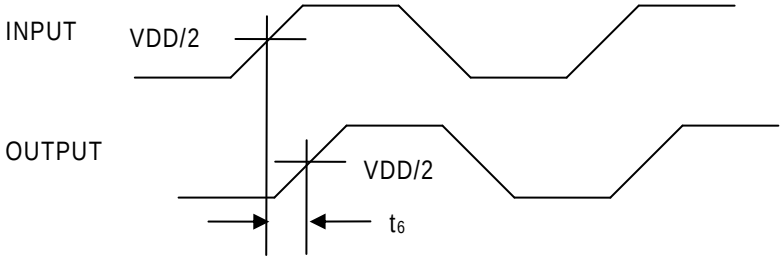
All Outputs Rise/Fall Time



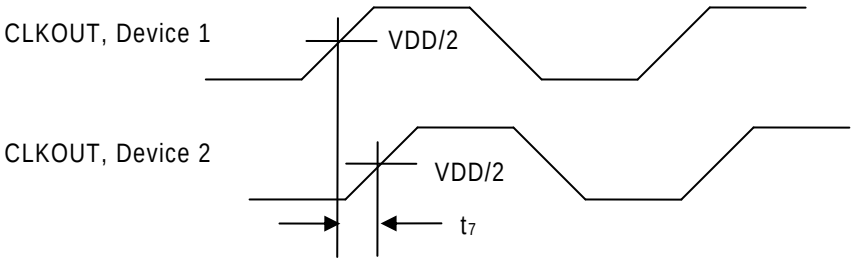
Output-Output Skew



Input-Output Propagation Delay

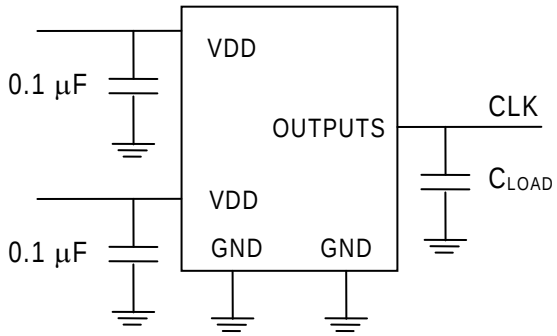


Device-Device Skew

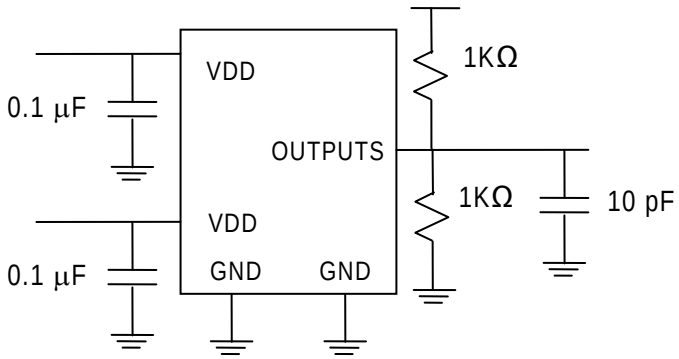


TEST CIRCUITS

Test Circuit #1



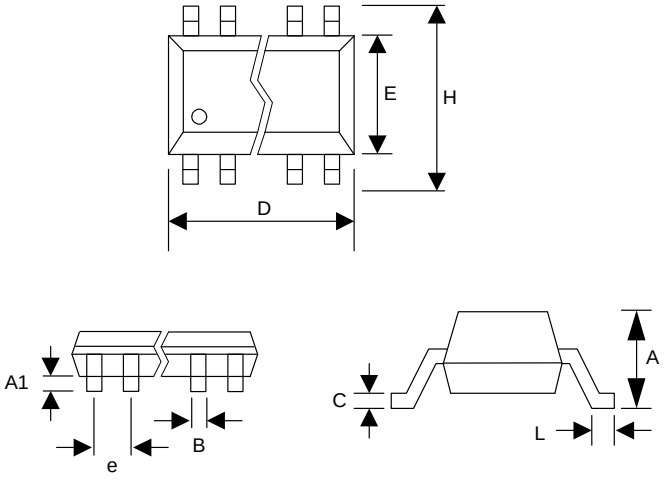
Test Circuit #2



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

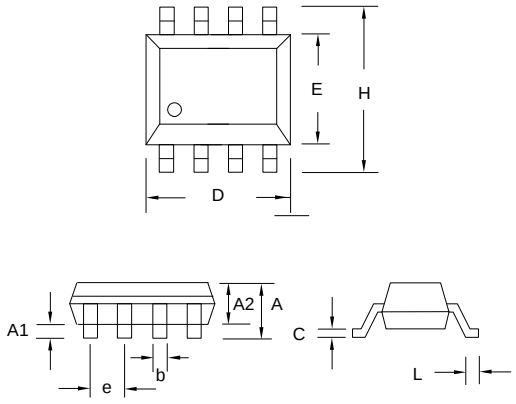
SOP-16L, SSOP-16L, TSSOP-16L (mm)

	SOP		SSOP		TSSOP	
Symbol	Min.	Max.	Min.	Max.	Min.	Max.
A	1.35	1.75	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15	0.05	0.15
B	0.33	0.51	0.2	0.3	0.19	0.30
C	0.19	0.25	0.18	0.25	0.09	0.20
D	9.80	10.00	4.8	5.0	4.90	5.10
E	3.80	4.00	3.8	3.98	4.30	4.50
H	5.80	6.20	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.40	1.27	0.45	0.75
e	1.27 BSC		0.635 BSC		0.65 BSC	



SOP 8L

Symbol	Dimension in mm	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	

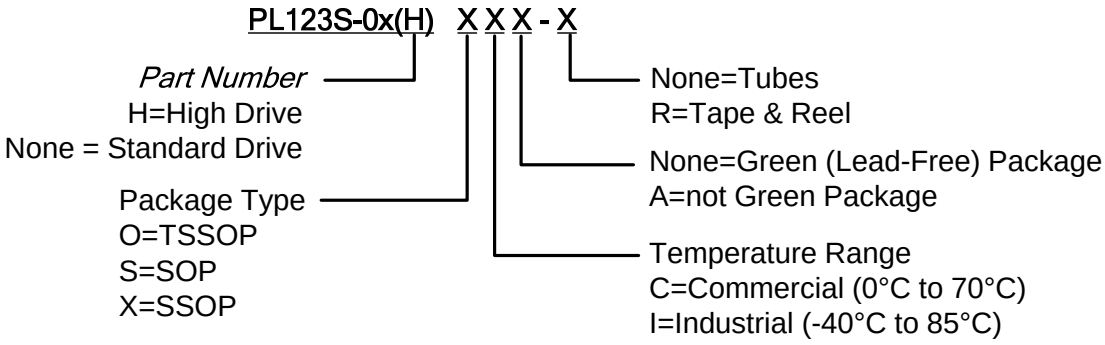


ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-05/-0990 Fax: (510) 492-05/-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
Green (Lead-Free) Package		
PL123S-05SC	P123S-05	8-Pin SOP Tube
PL123S-05SC-R	P123S-05	8-Pin SOP (Tape and Reel)
PL123S-05HSC	P123S-05H	8-Pin SOP Tube
PL123S-05HSC-R	P123S-05H	8-Pin SOP (Tape and Reel)
PL123S-09OC	P123S-09	16-Pin TSSOP Tube
PL123S-09OC-R	P123S-09	16-Pin TSSOP (Tape and Reel)
PL123S-09HOC	P123S-09H	16-Pin TSSOP Tube
PL123S-09HOC-R	P123S-09H	16-Pin TSSOP (Tape and Reel)
PL123S-09SC	P123S-09	16-Pin SOP Tube
PL123S-09SC-R	P123S-09	16-Pin SOP (Tape and Reel)
PL123S-09HSC	P123S-09H	16-Pin SOP Tube
PL123S-09HSC-R	P123S-09H	16-Pin SOP (Tape and Reel)
PL123S-09XC	P123S-09	16-Pin SSOP Tube
PL123S-09XC-R	P123S-09	16-Pin SSOP (Tape and Reel)
PL123S-09HXC	P123S-09H	16-Pin SSOP Tube
PL123S-09HXC-R	P123S-09H	16-Pin SSOP (Tape and Reel)

(continued)

PART NUMBER

Part/Order Number	Marking	Package Option
Not Green Package		
PL123S-05SCA	P123S-05	8-Pin SOP Tube
PL123S-05SCA-R	P123S-05	8-Pin SOP (Tape and Reel)
PL123S-05HSCA	P123S-05H	8-Pin SOP Tube
PL123S-05HSCA-R	P123S-05H	8-Pin SOP (Tape and Reel)
PL123S-09OCA	P123S-09	16-Pin TSSOP Tube
PL123S-09OCA-R	P123S-09	16-Pin TSSOP (Tape and Reel)
PL123S-09HOCA	P123S-09H	16-Pin TSSOP Tube
PL123S-09HOCA-R	P123S-09H	16-Pin TSSOP (Tape and Reel)
PL123S-09SCA	P123S-09	16-Pin SOP Tube
PL123S-09SCA-R	P123S-09	16-Pin SOP (Tape and Reel)
PL123S-09HSCA	P123S-09H	16-Pin SOP Tube
PL123S-09HSCA-R	P123S-09H	16-Pin SOP (Tape and Reel)
PL123S-09XCA	P123S-09	16-Pin SSOP Tube
PL123S-09XCA-R	P123S-09	16-Pin SSOP (Tape and Reel)
PL123S-09HXCA	P123S-09H	16-Pin SSOP Tube
PL123S-09HXCA-R	P123S-09H	16-Pin SSOP (Tape and Reel)

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf