FEATURES

- 1:9 output fanout buffer for DC to 134MHz
- Low power consumption for portable applications
- Low input-output delay
- Output-Output skew less than 250ps
- 2.5V to 3.3V, ±10% operation
- Operating temperature range from -40°C to 85°C
- Available in 16-Pin SOP GREEN/RoHS package

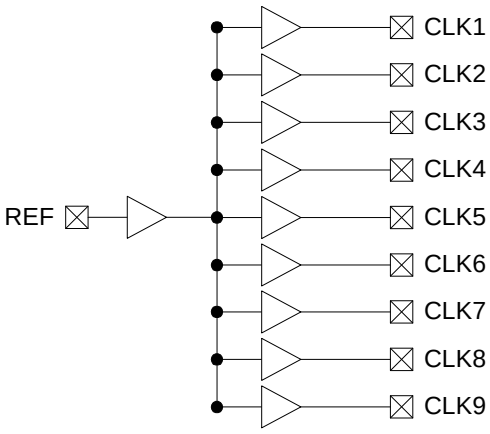
DESCRIPTION

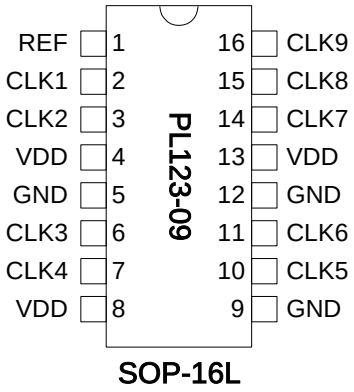
The PL123-09N is a low-cost fanout buffer for distributing high-speed clocks with low output to output skew. The PL123-09N accepts an input from DC to 134MHz and provides 9 outputs of the same frequency. A typical application for driving SDRAM in PC systems would use eight outputs to drive two DIMMs, or four SO-DIMMs, with the remaining output used for driving an external feedback to a PLL.

The PL123-09N is designed with three pairs of power/ground pins to minimize EMI and it consumes less than 32 mA at 66 MHz, ideal for low-power mobile applications. It is available in a compact 150-mil 16-pin SOP package.

These parts are not intended for 5V input-tolerant applications.

BLOCK DIAGRAM AND PACKAGE PINOUT





SOP-16L

PIN DESCRIPTIONS

Name	SOP-16L	Type	Description
REF	1	I	Input reference frequency.
CLK1	2	O	Buffered clock output
CLK2	3	O	Buffered clock output
VDD	4, 8, 13	P	VDD connection
GND	5, 9, 12	P	GND connection
CLK3	6	O	Buffered clock output
CLK4	7	O	Buffered clock output
CLK5	10	O	Buffered clock output
CLK6	11	O	Buffered clock output
CLK7	14	O	Buffered clock output
CLK8	15	O	Buffered clock output
CLK9	16	O	Buffered clock output

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces (> 1 inch) as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using frequencies < 50MHz and 0.01µF for designs using frequencies > 50MHz.

Typical CMOS termination

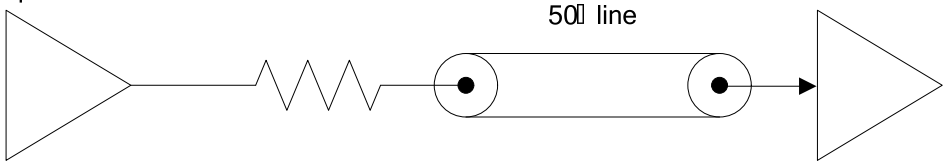
Place Series Resistor as close as possible to CMOS output

CMOS Output Buffer

(Typical buffer impedance 20 Ω)

To CMOS Input

50Ω line



Connect a 33 Ω series resistor at each of the output clocks to enhance the stability of the output signal

ABSOLUTE MAXIMUM CONDITIONS

Supply Voltage to Ground Potential ..... –0.5V to 4.6V
DC Input Voltage..... V_{SS} – 0.5V to 4.6V
Storage Temperature .....–65°C to 150°C

Junction Temperature..... 150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015).....> 2000V

OPERATING CONDITIONS

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	2.25	3.63	V
T_A	Commercial Operating Temperature (ambient temperature)	0	70	°C
	Industrial Operating Temperature (ambient temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz	—	30	pF
	Load Capacitance, above 100 MHz	—	10	pF
C_{IN}	Input Capacitance	—	7	pF
REF, CLK[1:9]	Operating Frequency, Input=Output	DC	134	MHz
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

ELECTRICAL CHARACTERISTICS (Commercial and Industrial Temperature Devices)

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage [1]		–	0.8	V
V_{IH}	Input HIGH Voltage [1]		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100	µA
V_{OL}	Output LOW Voltage [2]	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output HIGH Voltage [2]	I_{OH} = –8 mA	2.4	–	V
I_{DD}	Supply Current	66.67MHz with unloaded outputs	–	32	mA

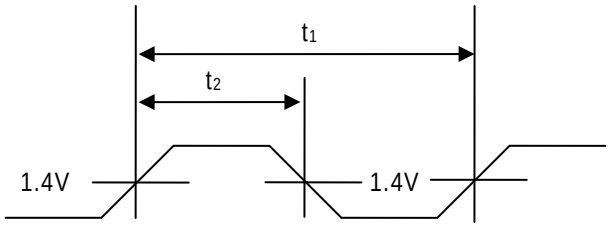
SWITCHING CHARACTERISTICS (Commercial and Industrial Temperature Devices) [3]

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
	Duty Cycle [2] = t2 ÷ t1	Measured at 1.4V	40	50	60	%
t_3	Rise Time [2]	Measured between 0.8V and 2.0V	–	–	1.5	ns
t_4	Fall Time [2]	Measured between 0.8V and 2.0V	–	–	1.5	ns
t_5	Output to Output Skew [2]	All outputs equally loaded	–	–	250	ps
t_6	Propagation Delay, REF Rising Edge to CLKX Rising Edge [2]	Measured at V_{DD}/2	1	5	9.2	ns

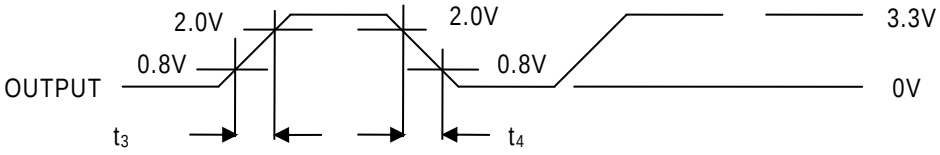
Notes:
1. REF input has a threshold voltage of V_{DD}/2
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.
3. All parameters are specified with loaded outputs.

SWITCHING WAVEFORMS

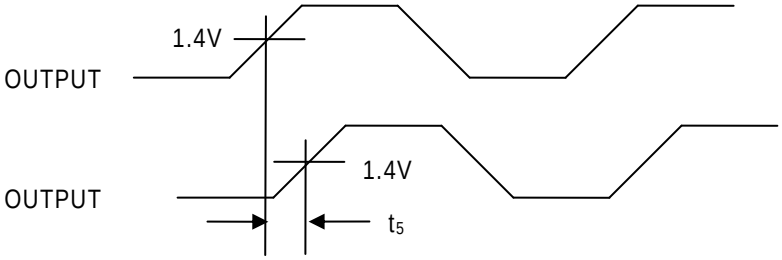
Duty Cycle Timing



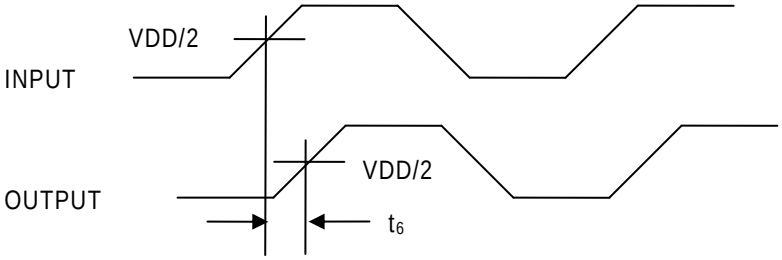
All Outputs Rise/Fall Time



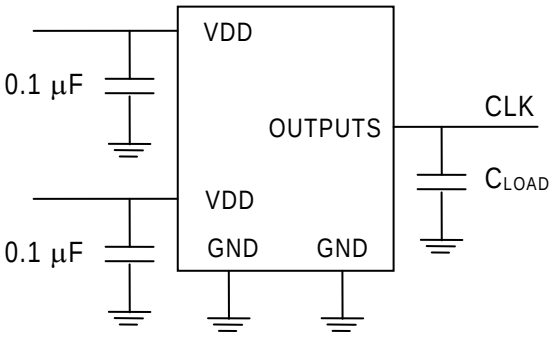
Output-Output Skew



Input-Output Propagation Delay



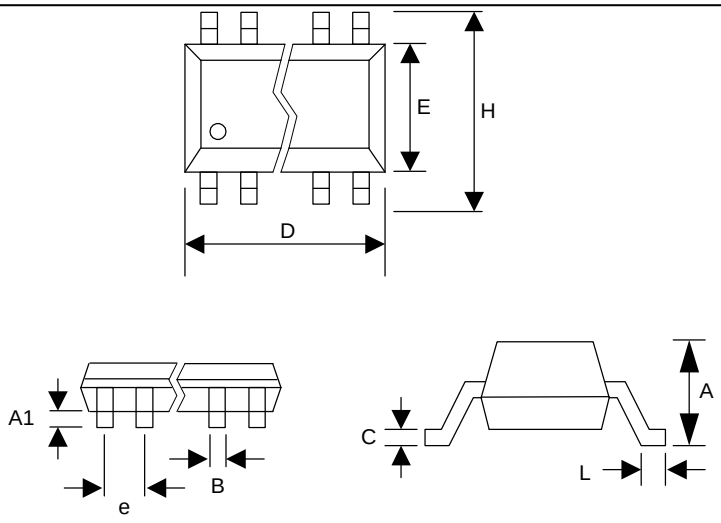
TEST CIRCUIT



PACKAGE DRAWING (GREEN PACKAGE COMPLIANT)

SOP-16L (mm)

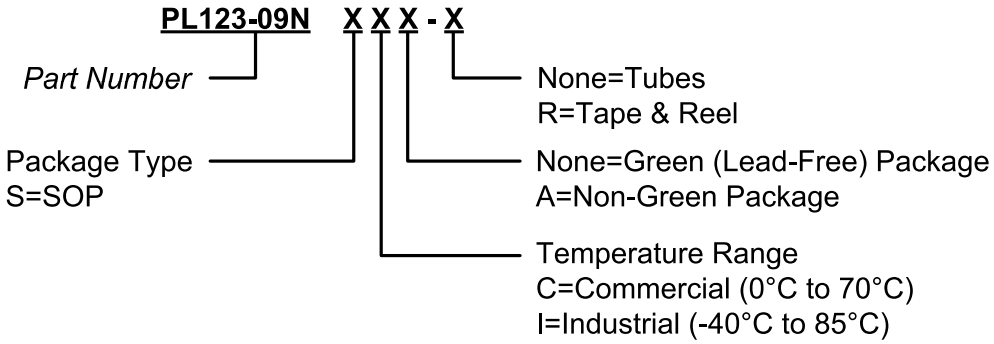
Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
H	5.80	6.20
L	0.40	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-05/-0990 Fax: (510) 492-05/-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
Green (Lead-Free) Package		
PL123-09NSC	P123-09N	16-Pin SOP Tube
PL123-09NSC-R	P123-09N	16-Pin SOP (Tape and Reel)
PL123-09NSI	P123-09N	16-Pin SOP Tube
PL123-09NSI-R	P123-09N	16-Pin SOP (Tape and Reel)
Non-Green Package		
PL123-09NSCA	P123-09N	16-Pin SOP Tube
PL123-09NSCA-R	P123-09N	16-Pin SOP (Tape and Reel)
PL123-09NSIA	P123-09N	16-Pin SOP Tube
PL123-09NSIA-R	P123-09N	16-Pin SOP (Tape and Reel)

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf