3.3V Zero Delay Buffer

FEATURES

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations, see “Available Configurations” table
- Multiple low-skew outputs
- Two banks of four outputs, three-stateable by two select inputs
- 10 MHz to 134 MHz operating range
- Low cycle-to-cycle jitter
- 16 pin SOP or TSSOP packages
- 3.3V operation
- Commercial and industrial temperature available

DESCRIPTION

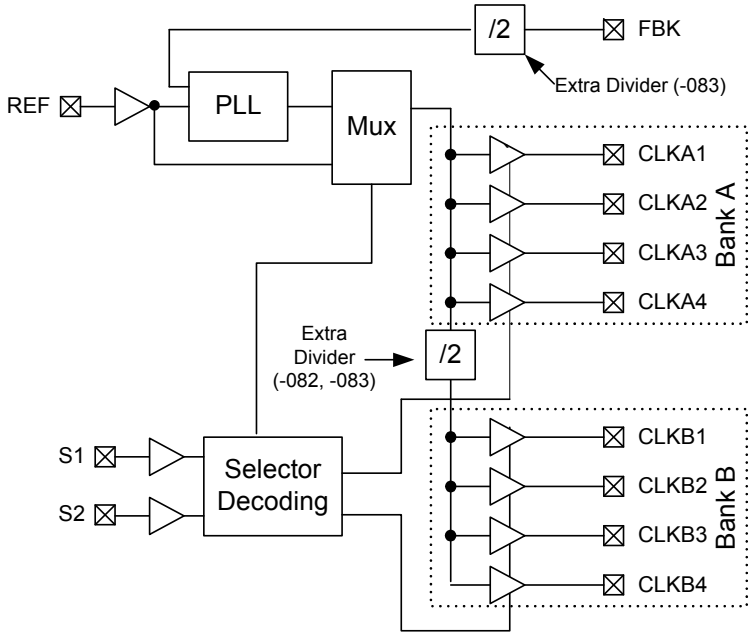
The PL123-08 is a PLL-based zero-delay buffer family, used to distribute up to eight outputs. Select inputs S2 and S1 control the state of the two output banks.

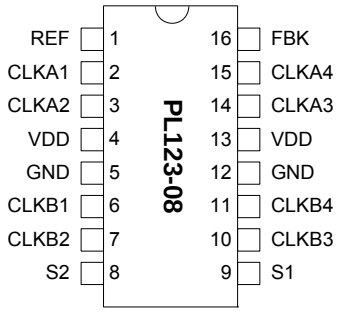
An external feedback pin enables removing delay from external components. It also provides adjustable input-to-output delay by varying its loading relative to the output pin loading.

Various options are available to multiply the input frequency by 0.5, 1, 2, or 4x (see the Available Configuration table for details). Standard (8 mA) and High (12 mA) drive strengths may also be ordered. In the special case when S2:S1 is 1:0, the PLL is bypassed and REF is output from DC to the maximum frequency, thus behaving like a (non-zero delay) fan-out buffer.

These parts are not intended for 5V input-tolerant applications.

BLOCK DIAGRAM





PIN DESCRIPTION

Pin	Name	Type	Description
1	REF[1]	I	Input reference frequency
2	CLKA1[2]	O	Clock output, Bank A
3	CLKA2[2]	O	Clock output, Bank A
4	VDD	P	3.3V supply
5	GND	P	Ground
6	CLKB1[2]	O	Clock output, Bank B
7	CLKB2[2]	O	Clock output, Bank B
8	S2[3]	I	Select input, bit 2
9	S1[3]	I	Select input, bit 1
10	CLKB3[2]	O	Clock output, Bank B
11	CLKB4[2]	O	Clock output, Bank B
12	GND	P	Ground
13	VDD	P	3.3V supply
14	CLKA3[2]	O	Clock output, Bank A
15	CLKA4[2]	O	Clock output, Bank A
16	FBK	I	PLL feedback input

SELECT INPUT DECODING

S2	S1	CLK A1–A4	CLK B1–B4	Output Source	PLL Shutdown
0	0	Three-State	Three-State	PLL	Y
0	1	Driven	Three-State	PLL	N
1	0	Driven[4]	Driven[4]	Reference	Y
1	1	Driven	Driven	PLL	N

AVAILABLE CONFIGURATIONS

Device	Feedback From	Bank A Frequency	Bank B Frequency
PL123-08	Bank A or Bank B	Reference	Reference
PL123-08H	Bank A or Bank B	Reference	Reference
PL123-082	Bank A	Reference	Reference / 2
PL123-082	Bank B	2 X Reference	Reference
PL123-083	Bank A	2 X Reference	Reference or Inverted Reference [5]
PL123-083	Bank B	4 X Reference	2 X Reference

Notes: 1: Weak pull-down. 2: Weak pull-down on all outputs. 3: Weak pull-up on these inputs.
4: Outputs inverted on PL123-082 and -083 in bypass mode (S2=1, S1=0).
5: Output is phase indeterminant (0° or 180° from input clock). If phase integrity is required, use PL123-082.

ZERO-DELAY AND SKEW CONTROL

The PLL's feedback path must be closed by connecting FBK to one of the available eight outputs. The output driving the FBK pin will drive an (internal) output pin load of 7pF plus any additional loading placed on this output pin.

For zero-delay applications, all outputs, including the FBK pin connected to an output pin, must be loaded equally. Varying the loading between the FBK pin and output pins can adjust the input-to-output delay.

MAXIMUM RATINGS

Supply Voltage to Ground Potential.....-0.5V to 4.6V

DC Input Voltage (Except REF).....-0.5V to VDD+0.5V

DC Input Voltage REF.....-0.5V to 4.6V

Storage Temperature.....-65 to 150 °C

Junction Temperature.....150 °C

Static Discharge Voltage (MIL-STD-883, Method 3015)..> 2KV

OPERATING CONDITIONS

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Commercial Operating Temperature (ambient temperature)	0	70	°C
	Industrial Operating Temperature (ambient temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz	–	30	pF
	Load Capacitance, above 100 MHz	–	15	pF
C_{IN}	Input Capacitance [6]	–	7	pF
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Notes: 6: Applies to both REF clock and FBK inputs.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

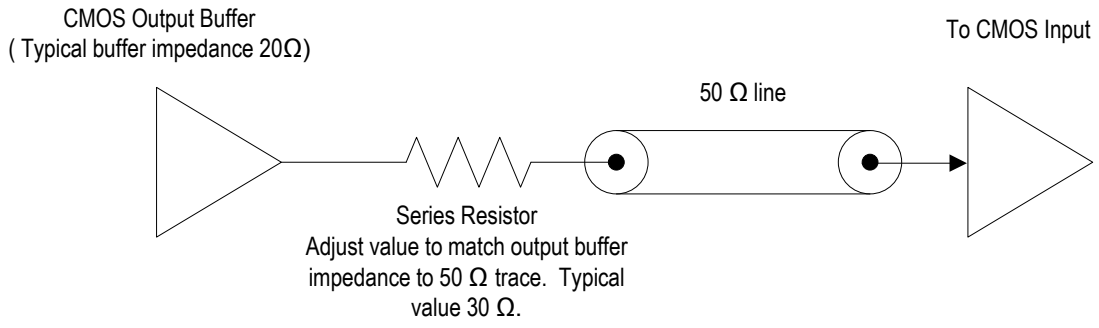
Signal Integrity and Termination Considerations

- Keep traces short
- Trace = Inductor. With a capacitive load, equals ringing
- Long trace = Transmission Line. Without proper termination this will cause reflections (causing ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Terminate traces with characteristic impedance of the trace to avoid reflections (see figure below).

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to bypass noise from the power supply
- Multiple VDD pins should be decoupled separately for best performance.
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs supporting frequencies below 50MHz (0.01μF for designs supporting frequencies above 50MHz).

Typical CMOS termination
Place Series Resistor as close as possible to CMOS output



ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min.	Max.	Unit
VIL	Input LOW Voltage		–	0.8	V
VIH	Input HIGH Voltage		2.0	–	V
IIL	Input LOW Current	VIN = 0V	–	50.0	µA
IIH	Input HIGH Current	VIN = VDD	–	100.0	µA
VOL	Output LOW Voltage[7]	IOL = 8 mA (-08, -082, -083) IOL = 12 mA (-08H)	–	0.4	V
VOH	Output HIGH Voltage[7]	IOH = –8 mA (-08, -082, -083) IOL = –12 mA (-08H)	2.4	–	V
IDD (PD mode)	Power Down Supply Current	REF = 0 MHz, Commercial Temp.		12.0	µA
		REF = 0 MHz, Industrial Temp.	–	25.0	µA
IDD	Supply Current (Unloaded Outputs)	100-MHz REF Select inputs at VDD or GND	–	45.0	mA
			–	70.0 (-08H)	mA
		66-MHz REF (-08, -082, -083), Commercial	–	32.0	mA
		33-MHz REF (-08, -082, -083), Commercial	–	18.0	mA
		66-MHz REF (-08, -082, -083), Industrial Temp.	–	35.0	mA
		33-MHz REF (-08, -082, -083), Industrial Temp.	–	20.0	mA

Notes: 7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

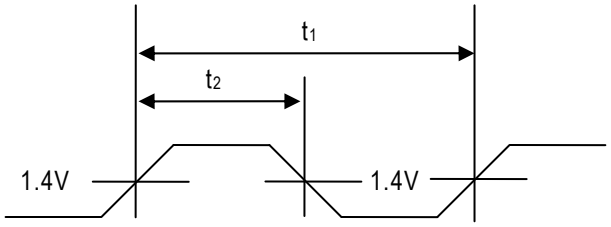
SWITCHING CHARACTERISTICS [8]

Parame-	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load, All devices	10	–	100	MHz
t_1	Output Frequency	20-pF load, –08H devices	10	–	134	MHz
t_1	Output Frequency	15-pF load, –08, –082, –083 devices	10	–	134	MHz
	Duty Cycle [7] = t2 ÷ t1	Measured at 1.4V, FOUT = 66.66 MHz 30-pF load	40	50	60	%
	Duty Cycle [7] = t2 ÷ t1	Measured at 1.4V, FOUT <50.0 MHz 15-pF load	45	50	55	%
t_3	Rise Time [7] (–08, –082, –083)	Measured between 0.8V and 2.0V, 30-pF load Commercial Temperature	–	–	2.20	ns
		Measured between 0.8V and 2.0V, 30-pF load Industrial Temperature	–	–	2.50	ns
		Measured between 0.8V and 2.0V, 15-pF load	–	–	1.50	ns
t_3	Rise Time [7] (–08H)	Measured between 0.8V and 2.0V, 30-pF load	–	–	1.50	ns
t_4	Fall Time [7] (–08,–082,–083)	Measured between 0.8V and 2.0V, 30-pF load Commercial Temperature	–	–	2.20	ns
		Measured between 0.8V and 2.0V, 30-pF load Industrial Temperature	–	–	2.50	ns
		Measured between 0.8V and 2.0V, 15-pF load	–	–	1.50	ns
t_4	Fall Time [7] (–08H)	Measured between 0.8V and 2.0V, 30-pF load	–	–	1.25	ns
t_5	Output to Output Skew on same Bank (–08,–082,–083)	All outputs equally loaded	–	–	200	ps
	Output to Output Skew (–08H)	All outputs equally loaded	–	–	200	ps
	Output Bank A to Output Bank B Skew (–08)	All outputs equally loaded	–	–	200	ps
	Output Bank A to Output Bank B Skew (–082, –083)	All outputs equally loaded	–	–	400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge [7]	Measured at VDD/2	–	0	±250	ps
t_7	Device to Device Skew [7]	Measured at VDD/2 on the FBK pins of devices	–	0	700	ps
t_8	Output Slew Rate [7]	Measured between 0.8V and 2.0V on –08H device using Test Circuit #2	1	–	–	V/ns
t_J	Cycle to Cycle Jitter [7] (–08, –08H)	Measured at 66.67 MHz, loaded outputs, 15-pF load	–	75	200	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load	–	–	200	ps
		Measured at 133.3 MHz, loaded outputs, 15-pF load	–	–	100	ps
t_J	Cycle to Cycle Jitter [7] (–082, –083)	Measured at 66.67 MHz, loaded outputs 30-pF load	–	–	400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load	–	–	400	Ps
t_{LOCK}	PLL Lock Time [7]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

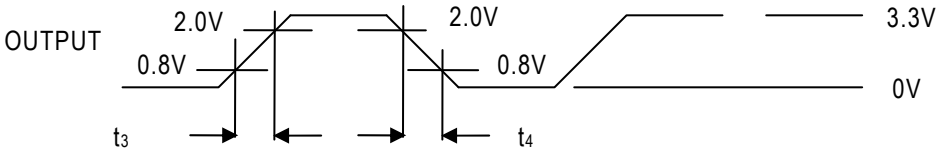
Notes: 8. All parameters are specified with loaded outputs.

SWITCHING WAVEFORMS

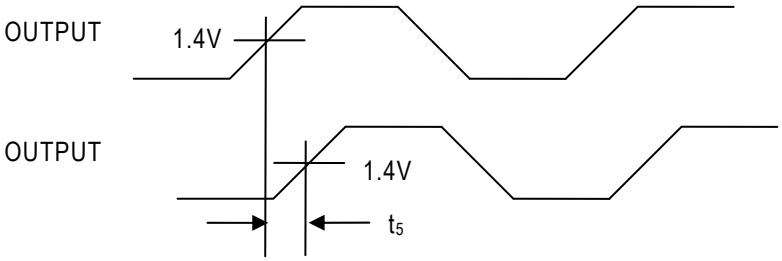
Duty Cycle Timing



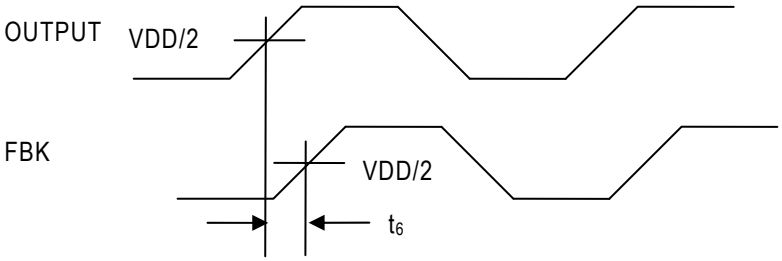
All Outputs Rise/Fall Time



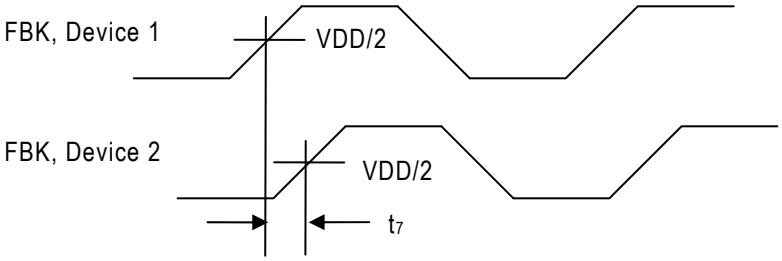
Output-Output Skew



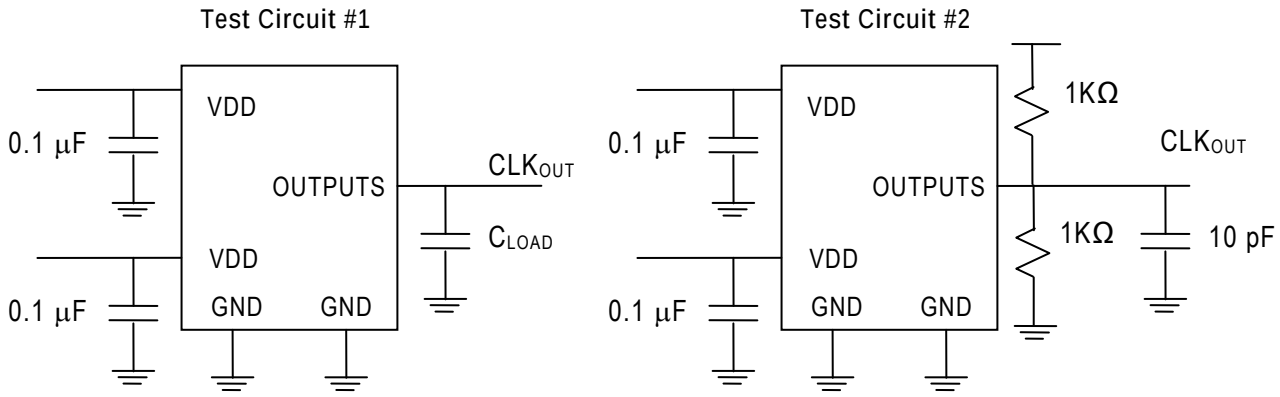
Input-Output Propagation Delay



Device-Device Skew



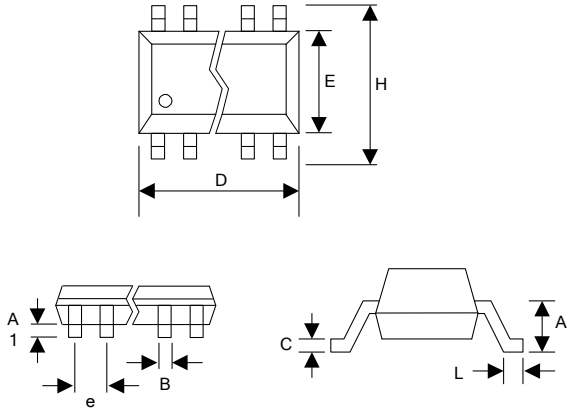
TEST CIRCUITS



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

16 PIN Narrow SOP, TSSOP (mm)

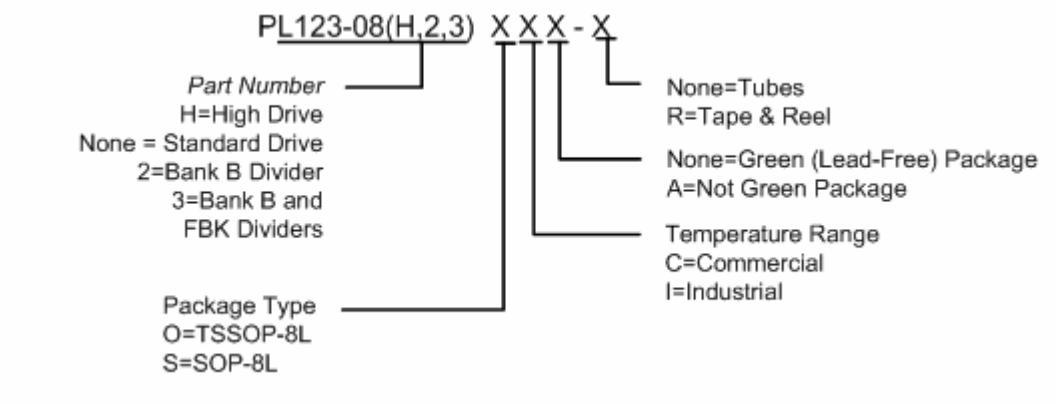
Symbol	SOIC Min.	SOIC Max	TSSOP Min.	TSSOP Max
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.00	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option	Operating Range
Green (Lead-Free) Package			
PL123-08HOC	P123-08H	16-Pin TSSOP Tube	Commercial
PL123-08HOC-R	P123-08H	16-Pin TSSOP (Tape and Reel)	Commercial
PL123-08SC	P123-08	16-Pin SOP Tube	Commercial
PL123-08SC-R	P123-08	16-Pin SOP (Tape and Reel)	Commercial
PL123-08HSC	P123-08H	16-Pin SOP Tube	Commercial
PL123-08HSC-R	P123-08H	16-Pin SOP (Tape and Reel)	Commercial
PL123-082SC	P123-082	16-Pin SOP Tube	Commercial
PL123-082SC-R	P123-082	16-Pin SOP (Tape and Reel)	Commercial
PL123-083SC	P123-083	16-Pin SOP Tube	Commercial
PL123-083SC-R	P123-083	16-Pin SOP (Tape and Reel)	Commercial
PL123-08HOI	P123-08H	16-Pin TSSOP Tube	Industrial
PL123-08HOI-R	P123-08H	16-Pin TSSOP (Tape and Reel)	Industrial
PL123-08SI	P123-08	16-Pin SOP Tube	Industrial
PL123-08SI-R	P123-08	16-Pin SOP (Tape and Reel)	Industrial
PL123-08HSI	P123-08H	16-Pin SOP Tube	Industrial
PL123-08HSI-R	P123-08H	16-Pin SOP (Tape and Reel)	Industrial
PL123-082SI	P123-082	16-Pin SOP Tube	Industrial
PL123-082SI-R	P123-082	16-Pin SOP (Tape and Reel)	Industrial
PL123-083SI	P123-083	16-Pin SOP Tube	Industrial
PL123-083SI-R	P123-083	16-Pin SOP (Tape and Reel)	Industrial

(continued)

PART NUMBER

Part/Order Number	Marking	Package Option	Operating Range
Not Green Package			
PL123-08HOCA	P123-08H	16-Pin TSSOP Tube	Commercial
PL123-08HOCA-R	P123-08H	16-Pin TSSOP (Tape and Reel)	Commercial
PL123-08SCA	P123-08	16-Pin SOP Tube	Commercial
PL123-08SCA-R	P123-08	16-Pin SOP (Tape and Reel)	Commercial
PL123-08HSCA	P123-08H	16-Pin SOP Tube	Commercial
PL123-08HSCA-R	P123-08H	16-Pin SOP (Tape and Reel)	Commercial
PL123-082SCA	P123-082	16-Pin SOP Tube	Commercial
PL123-082SCA-R	P123-082	16-Pin SOP (Tape and Reel)	Commercial
PL123-083SCA	P123-083	16-Pin SOP Tube	Commercial
PL123-083SCA-R	P123-083	16-Pin SOP (Tape and Reel)	Commercial
PL123-08HOIA	P123-08H	16-Pin TSSOP Tube	Industrial
PL123-08HOIA-R	P123-08H	16-Pin TSSOP (Tape and Reel)	Industrial
PL123-08SIA	P123-08	16-Pin SOP Tube	Industrial
PL123-08SIA-R	P123-08	16-Pin SOP (Tape and Reel)	Industrial
PL123-08HSIA	P123-08H	16-Pin SOP Tube	Industrial
PL123-08HSIA-R	P123-08H	16-Pin SOP (Tape and Reel)	Industrial
PL123-082SIA	P123-082	16-Pin SOP Tube	Industrial
PL123-082SIA-R	P123-082	16-Pin SOP (Tape and Reel)	Industrial
PL123-083SIA	P123-083	16-Pin SOP Tube	Industrial
PL123-083SIA-R	P123-083	16-Pin SOP (Tape and Reel)	Industrial

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf