3.3V Zero Delay Buffer

FEATURES

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations, see "Available Configurations" table
- Multiple low-skew outputs
- 10 MHz to 134 MHz operating range
- Low cycle-to-cycle jitter
- 8 pin SOP package
- 3.3V operation
- Commercial and industrial temperature available

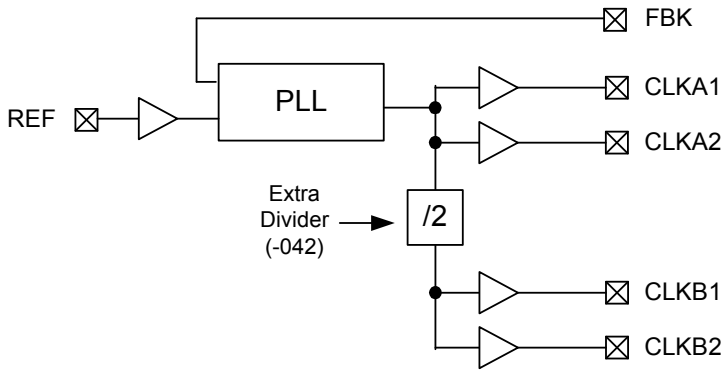
DESCRIPTION

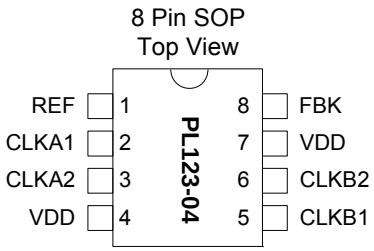
The PL123-04 is a PLL-based zero-delay buffer, used to distribute up to four outputs. An external feedback pin enables removing delay from external components. It also provides adjustable input-to-output delay by varying its loading relative to the output pin loading.

The PL123-042 option allows the user to obtain x1, x2, or x0.5 frequencies on the output bank. The exact multiplier depends on which output is connected to the FBK pin. Refer to the Available Configurations table below for more details.

These parts are not intended for 5V input-tolerant applications.

BLOCK DIAGRAM





AVAILABLE CONFIGURATIONS

Device	Feedback From	Bank A Frequency	Bank B Frequency
PL123-04	Bank A or Bank B	Reference	Reference
PL123-042	Bank A	Reference	Reference / 2
PL123-042	Bank B	2 x Reference	Reference

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PIN DESCRIPTION

Pin	Name	Type	Description
1	REF[1]	I	Input reference frequency
2	CLKA1[2]	O	Clock output, Bank A
3	CLKA2[2]	O	Clock output, Bank A
4	GND	P	Ground
5	CLKB1[2]	O	Clock output, Bank B
6	CLKB2[2]	O	Clock output, Bank B
7	VDD	P	3.3V Supply
8	FBK	I	PLL feedback input

Notes: 1: Weak pull-down.
2: Weak pull-down on all outputs.

The PLL's feedback path must be closed by connecting FBK to one of the available four outputs. The output driving the FBK pin will drive an (internal) pin load of 7pF plus any additional loading placed on this output pin.

For zero-delay applications, all outputs, including the FBK pin connected to an output pin, must be loaded equally. Varying the loading between the FBK pin and output pins can adjust the input-to-output delay.

MAXIMUM RATINGS

Supply Voltage to Ground Potential.....-0.5V to 4.6V

DC Input Voltage (Except REF).....-0.5V to VDD+0.5V

DC Input Voltage REF.....-0.5V to 4.6V

Storage Temperature.....-65 to 150 °C

Junction Temperature.....150 °C

Static Discharge Voltage (MIL-STD-883, Method 3015)..> 2KV

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LAYOUT RECOMMENDATIONS

The following guidelines assist in optimizing a PCB design:

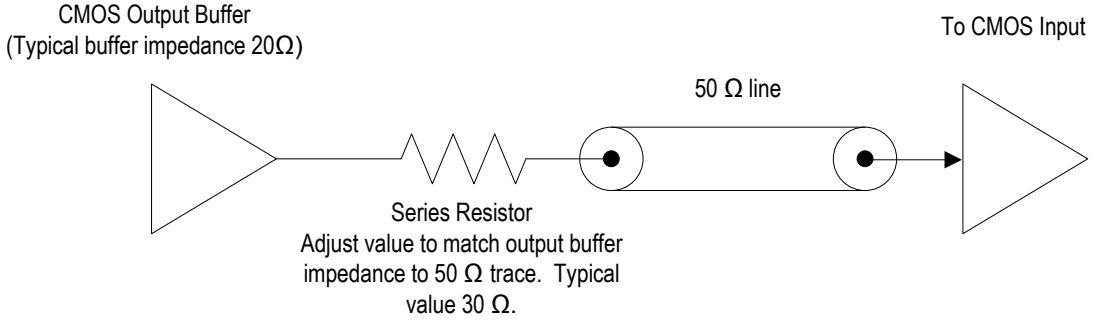
Signal Integrity and Termination Considerations

- Keep traces short
- Trace = Inductor. Adding a capacitive load may cause ringing.
- Long trace = Transmission Line. Without proper termination this will cause reflections (causing ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Terminate traces with characteristic impedance of the trace to avoid reflections (see figure below).

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to bypass noise from the power supply
- Multiple VDD pins should be decoupled separately for best performance.
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs supporting frequencies below 50MHz (0.01μF for designs supporting frequencies above 50MHz).

Typical CMOS termination
Place Series Resistor as close as possible to CMOS output



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OPERATING CONDITIONS

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Commercial Operating Temperature (ambient temperature)	0	70	°C
	Industrial Operating Temperature (ambient temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz	—	30	pF
	Load Capacitance, above 100 MHz	—	15	pF
C_{IN}	Input Capacitance [3]	—	7	pF
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Notes: 3: Applies to both REF clock and FBK inputs.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min.	Max.	Unit
VIL	Input LOW Voltage		–	0.8	V
VIH	Input HIGH Voltage		2.0	–	V
IIL	Input LOW Current	VIN = 0V	–	50.0	µA
IIH	Input HIGH Current	VIN = VDD	–	100.0	µA
VOL	Output LOW Voltage[4]	IOL = 8 mA	–	0.4	V
VOH	Output HIGH Voltage[4]	IOH = –8 mA	2.4	–	V
IDD (PD mode)	Power Down Supply Current	REF = 0 MHz, Commercial Temp.		12.0	µA
		REF = 0 MHz, Industrial Temp.	–	25.0	µA
IDD	Supply Current (Unloaded Outputs)	100-MHz REF Select inputs at VDD or GND	–	45.0	mA
		66-MHz REF, Commercial Temp.	–	32.0	mA
		33-MHz REF, Commercial Temp.	–	18.0	mA
		66-MHz REF, Industrial Temp.	–	35.0	mA
		33-MHz REF, Industrial Temp.	–	20.0	mA

Notes: 4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

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SWITCHING CHARACTERISTICS [5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load	10	–	100	MHz
t_1	Output Frequency	15-pF load	10	–	134	MHz
	Duty Cycle [4] = t2 ÷ t1	Measured at 1.4V, F_{OUT} = 66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle [4] = t2 ÷ t1	Measured at 1.4V, F_{OUT} <50.0 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Rise Time [4]	Measured between 0.8V and 2.0V, 30-pF load Commercial Temperature	–	–	2.20	ns
		Measured between 0.8V and 2.0V, 30-pF load Industrial Temperature	–	–	2.50	ns
		Measured between 0.8V and 2.0V, 15-pF load	–	–	1.50	ns
t_4	Fall Time [4]	Measured between 0.8V and 2.0V, 30-pF load Commercial Temperature	–	–	2.20	ns
		Measured between 0.8V and 2.0V, 30-pF load Industrial Temperature	–	–	2.50	ns
		Measured between 0.8V and 2.0V, 15-pF load	–	–	1.50	ns
t_5	Output to Output Skew on same Bank [4]	All outputs equally loaded	–	–	200	ps
	Output Bank A to Output Bank B Skew (–04)	All outputs equally loaded	–	–	200	ps
	Output Bank A to Output Bank B Skew (–042)	All outputs equally loaded	–	–	400	ps
t_6	Skew, REF Rising Edge to FBK Rising Edge [4]	Measured at VDD/2	–	0	±250	ps
t_7	Device to Device Skew [4]	Measured at VDD/2 on the FBK pins of devices	–	0	500	ps
t_J	Cycle to Cycle Jitter [4] (–04)	Measured at 66.67 MHz, loaded outputs, 15-pF load	–	90	175	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load	–	–	200	ps
		Measured at 133.3 MHz, loaded outputs, 15-pF load	–	–	100	ps
t_J	Cycle to Cycle Jitter [4] (–042)	Measured at 66.67 MHz, loaded outputs 30-pF load	–	–	400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load	–	–	375	ps
t_{LOCK}	PLL Lock Time [4]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

Notes: 5. All parameters are specified with loaded outputs.

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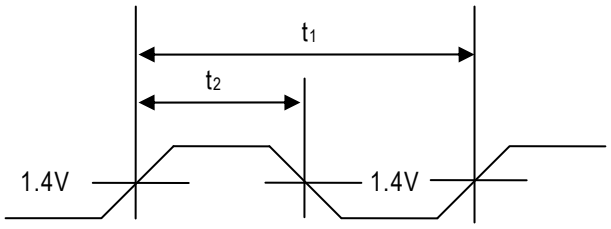
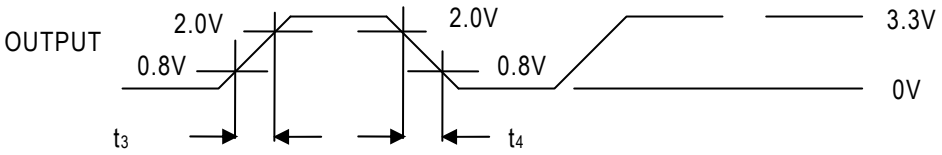
SWITCHING WAVEFORMS

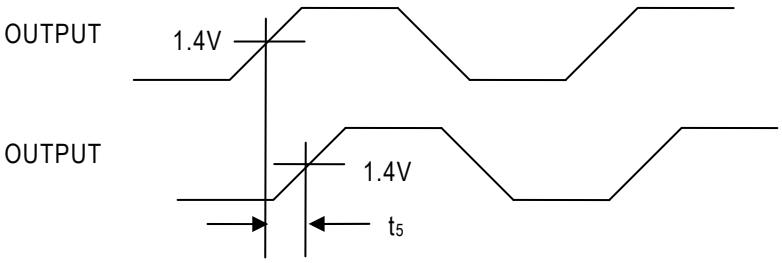
Duty Cycle Timing



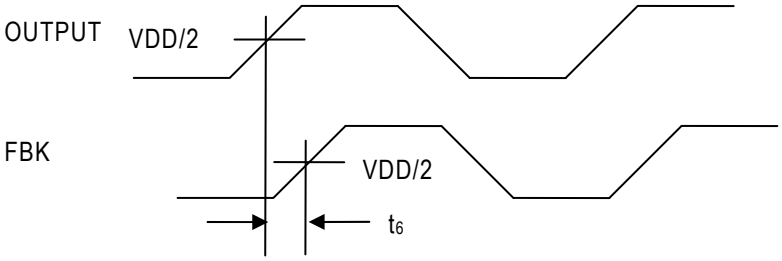
All Outputs Rise/Fall Time



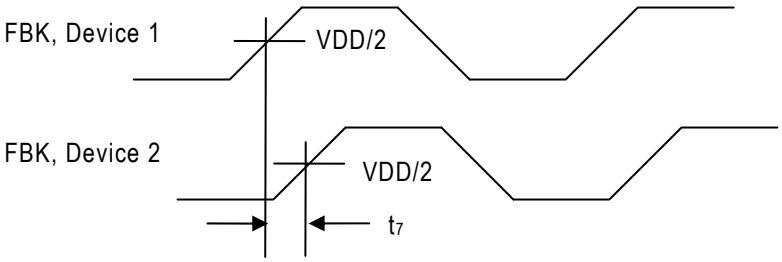
Output-Output Skew



Input-Output Propagation Delay



Device-Device Skew



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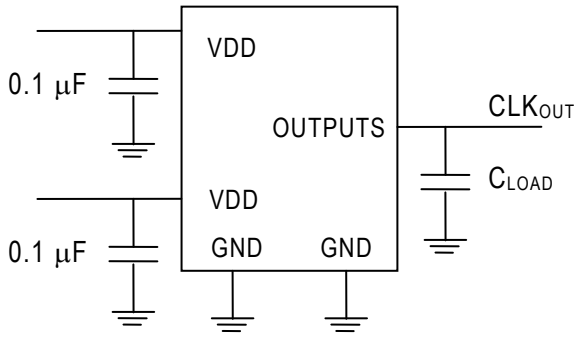
TEST CIRCUIT

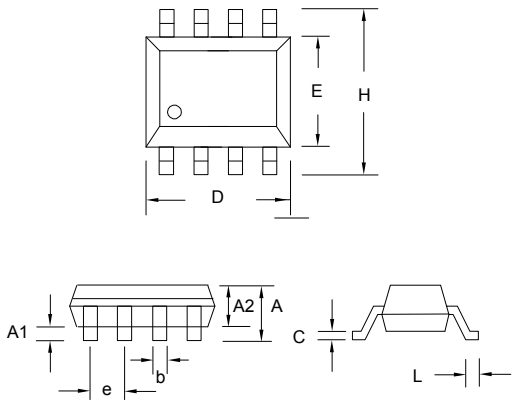
Test Circuit #1



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

8-Pin SOP

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



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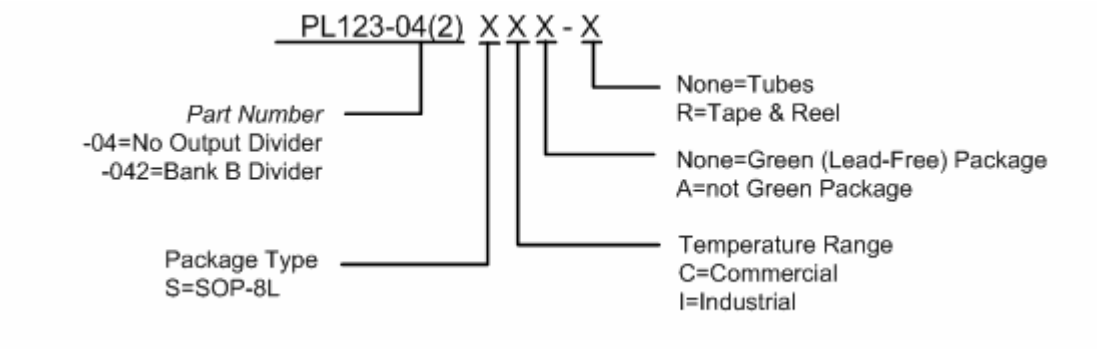
ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option	Range
Green (Lead-Free) Packages			
PL123-04SC	P123-04	8-Pin SOP Tube	Commercial
PL123-04SC-R	P123-04	8-Pin SOP (Tape and Reel)	Commercial
PL123-042SC	P123-042	8-Pin SOP Tube	Commercial
PL123-042SC-R	P123-042	8-Pin SOP (Tape and Reel)	Commercial
PL123-04SI	P123-04	8-Pin SOP Tube	Industrial
PL123-04SI-R	P123-04	8-Pin SOP (Tape and Reel)	Industrial
PL123-042SIC	P123-042	8-Pin SOP Tube	Industrial
PL123-042SIC-R	P123-042	8-Pin SOP (Tape and Reel)	Industrial
Not Green Packages			
PL123-04SCA	P123-04	8-Pin SOP Tube	Commercial
PL123-04SCA-R	P123-04	8-Pin SOP (Tape and Reel)	Commercial
PL123-042SCA	P123-042	8-Pin SOP Tube	Commercial
PL123-042SCA-R	P123-042	8-Pin SOP (Tape and Reel)	Commercial
PL123-04SIA	P123-04	8-Pin SOP Tube	Industrial
PL123-04SIA-R	P123-04	8-Pin SOP (Tape and Reel)	Industrial
PL123-042SICA	P123-042	8-Pin SOP Tube	Industrial
PL123-042SICA-R	P123-042	8-Pin SOP (Tape and Reel)	Industrial

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