TS128MEP6100

128MB 90PIN PC133 CL3 SDRAM
SO-DIMM With 16M X 16 3.3VOLT

Description

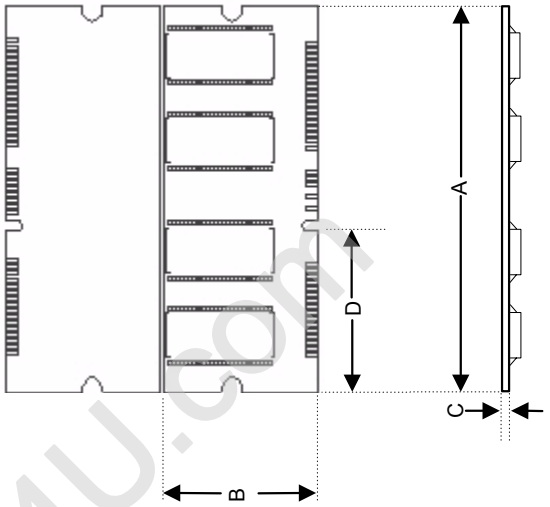
The TS128MEP6100 is a 32M bit x 32 Synchronous Dynamic RAM high-density memory modules. The TS128MEP6100 consists of 4 pieces of CMOS 16Mx16bits Synchronous DRAMs in TSOP-II 400mil packages on a 90-pin printed circuit board. The TS128MEP6100 is a one Line Memory Module and is intended for mounting into 90-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Performance Range: PC133.
- Burst Mode Operation.
- Auto and Self Refresh.
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Placement



PCB: 09-1730

Dimensions

Side	Millimeters	Inches
A	80.00 ± 0.200	3150 ± 0.008
B	32 ± 0.200	1.260± 0.008
C	1.00 ± 0.100	0.040 ± 0.004
D	33.70±0.100	1326.78±0.004

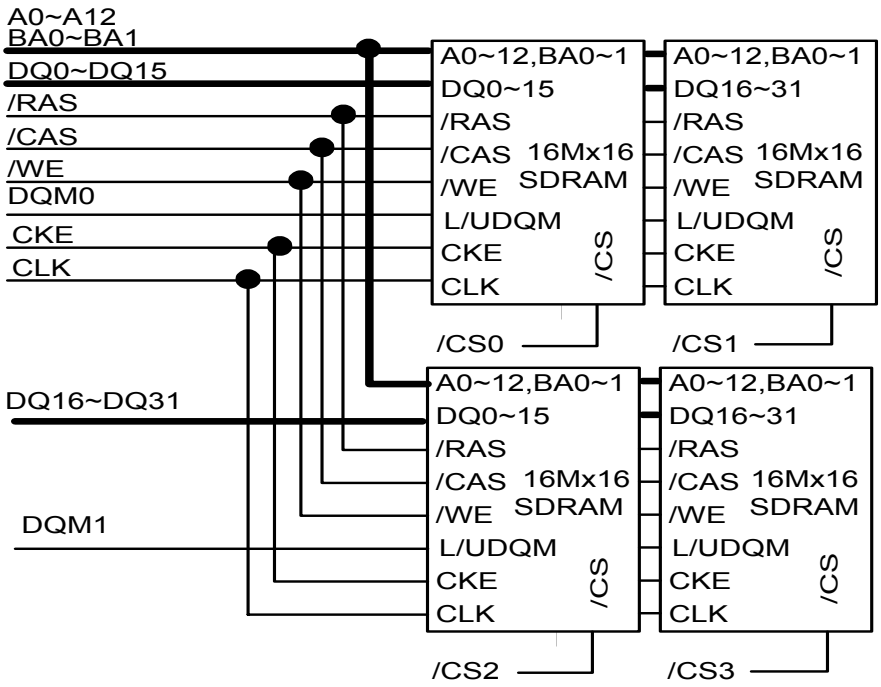
Pin Identification

Symbol	Function
A0~A12	Address inputs
BA0~BA1	Select Bank
DQ0~DQ31	Data inputs/outputs
CLK	Clock Input
CKE	Clock Enable Input
/CS0~/CS1	Chip Select Input
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
L/UDQM0~1	DQM
Vcc	Power Supply
Vss	Ground
NC	No Connection

Pinouts

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	49	NC	02	Vss	50	NC
03	SA1	51	NC	04	SCL	52	NC
05	SA0	53	NC	06	SDA	54	NC
07	Vss	55	A11	08	Vss	56	A12
09	Vcc	57	BA0	10	Vcc	58	BA1
11	DQ0	59	A9	12	DQ8	60	A10
13	DQ1	61	A7	14	DQ9	62	A8
15	DQ2	63	A5	16	DQ10	64	A6
17	DQ3	65	A3	18	DQ11	66	A4
19	DQ4	67	A1	20	DQ12	68	A2
21	DQ5	69	Vss	22	DQ13	70	A0
23	DQ6	71	Vcc	24	DQ14	72	Vcc
25	DQ7	73	DQ16	26	DQ15	74	DQ24
27	Vss	75	DQ17	28	Vss	76	DQ25
29	CLK0	77	DQ18	30	LDQM0	78	DQ26
31	Vss	79	DQ19	32	UDQM0	80	DQ27
33	NC	81	DQ20	34	/CS2	82	DQ28
35	/RAS	83	DQ21	36	/CS0	84	DQ29
37	NC	85	DQ22	38	/CAS	86	DQ30
39	CKE	87	DQ23	40	/CS3	88	DQ31
41	NC	89	Vss	42	/CS1	90	Vss
43	Vcc			44	/WE		
45	Vss			46	Vss		
47	UDQM1			48	LDQM1		

TS128MEP6100- Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 to +4.6	V
Voltage on V_{DD} supply to Vss	V_{DD}, V_{DDQ}	-1.0 to +4.6	V
Storage temperature	T_{STG}	-55 to +125	°C
Power dissipation	P_D	4	W
Mean time between failure	MTBF	50	Years

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	IOH=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	IOL=2mA
Input leakage current	I_{IL}	-10	-	10	uA	3
output leakage current	I_{oL}	-10	-	10	uA	-

Note: 1. V_{IH} (max) = 2.0V AC .The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (VDD = 3.3V ± .0.3V, TA = 0°C~70°C)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0~A_{11}, BA_0~ BA_1)	C_{IN1}	-	40	pF
Input capacitance (/RAS, /CAS, /WE)	C_{IN2}	-	40	pF
Input capacitance (CKE0)	C_{IN3}	-	40	pF
Input capacitance (CLK0)	C_{IN4}	-	14	pF
Input capacitance (/CS0~ /CS3)	C_{IN5}	-	10	pF
Input capacitance (DQM0~DQM1)	C_{IN6}	-	10	pF
Data input/output capacitance (DQ0~DQ31)	C_{OUT1}	-	14	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Value(Typ)	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA		400	mA	1
Precharge Standby Current in power-down mode	I_{CC2}**P**	CKE≤V_{IL}(max), t_{CC}=12ns		8	mA	
	I_{CC2}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞		8		
Precharge Standby Current in non power-down mode	I_{CC2}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=12ns Input signals are changed one time during 20ns		80	mA	
	I_{CC2}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		40		
Active Standby Current in power-down mode	I_{CC3}**P**	CKE≤V_{IL}(max), t_{CC}=12ns		20	mA	
	I_{CC3}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞		20		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=12ns Input signals are changed one time during 20ns		120	mA	
	I_{CC3}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		100		
Operating Current (Bust Mode)	I_{CC4}	I_{OL}= 0 mA Page Burst t_{CCD} = 2CLKs	3	560	mA	1
			2	-		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		800	mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		8	mA	

Note: 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 65°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V

AC Characteristics (TA = 0 to 65°C, VDD = 3.3V ± 0.3V, Vss= 0V)

Parameter	Symbol	Value	Unit	Note
System clock cycle time	T_{CK}	7.5	ns	1
CK high pulse width	t_{CKH}	2.5	ns	1
CK low pulse width	t_{CKL}(min)	2.5	ns	1
Access time from CK	T_{AC}	5.4	ns	1,2
Data-out hold time	T_{OH}	3.0	ns	1,2
CK to Data-out low impedance	t_{LZ}	0.0	ns	1,2
CK to Data-out high impedance	t_{HZ}	3.0	ns	1
Input setup time	T_{AS}, t_{CS}, t_{DS}, t_{CES}	1.5	ns	1
CKE setup time for power down exit	t_{CESP}	2.0	ns	1
Input hold time	T_{AH}, t_{CH}, t_{DH}, t_{CEH}	0.8	ns	1
Ref/Active to Ref/Active command period	t_{RC}	70.0	ns	1
Active to precharge command period	T_{RAS} (min)	45.0	ns	1
Active command to column command (same bank)	t_{RCD}	20.0	ns	1
Precharge to active command period	t_{RP}	20.0	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	15.0	ns	1
Active (a) to Active (b) command period	t_{RRD}	15.0	ns	1
Transition time (rise and fall)	t_T (min)	1.0	ns	
Refresh period	T_{REF} (max)	64.0	ms	

Note: 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.5V.

2. Access time is measured at 1.5V. Load condition is C_L = 50 pF

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	$BA_{0,1}$	A_{10}/AP	A_{11},A_{12} A_0~A_9	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X	X			
					L	V	V	V					
SDQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Note:
1. OP Code: Operand Code
   SA_0~SA_{11}, SBA_0~SBA_1: Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatically precharge without row precharge command is meant by “Auto”.
   Auto/self refresh can be issued only at both banks precharge state.
4. SBA_0~SBA_1: Bank select address.
   If both SBA_0 and SBA_1 are “Low” at read, write, row active and precharge, bank A is selected.
   If both SBA_0 is “Low” and SBA_1 is “High” at read, write, row active and precharge, bank B is selected.
   If both SBA_0 is “High” and SBA_1 is “Low” at read, write, row active and precharge, bank C is selected.
   If both SBA_0 and SBA_1 are “High” at read, write, row active and precharge, bank D is selected.
   If SA_{10}/AP is “High” at row precharge, SBA_0 and SBA_1 are ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command cannot be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. SDQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write SDQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read SDQM latency is 2)