7-BAND EVR FOR GRAPHIC EQUALIZER

■ GENERAL DESCRIPTION

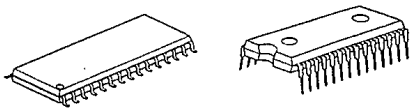
The NJU7305 is a electrical variable resistor(EVR) incorporated 7-band each for left and right channels, especially apply to stereo type graphic equalizer.

It consists of input controller, channel/band/level selector, 14 latches and resistor network blocks of 7 bands each for left and right channels.

The boost and cut value for each band of each channel can be set independently to each other by the channel/band/level selector controlled by external controller.

The maximum boost and cut range is ±12dB and the boost and cut value is adjusted by ±2dB step.

■ PACKAGE OUTLINE

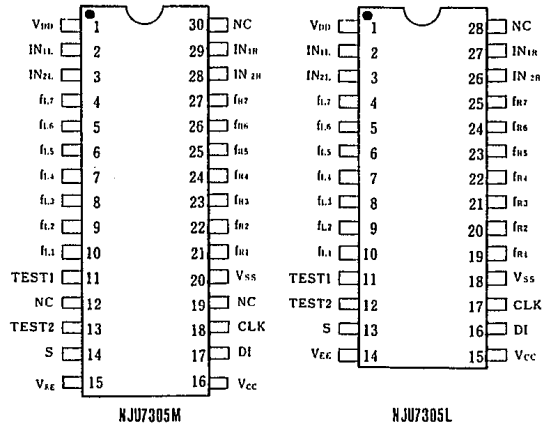


NJU7305M NJU7305L

■ FEATURES

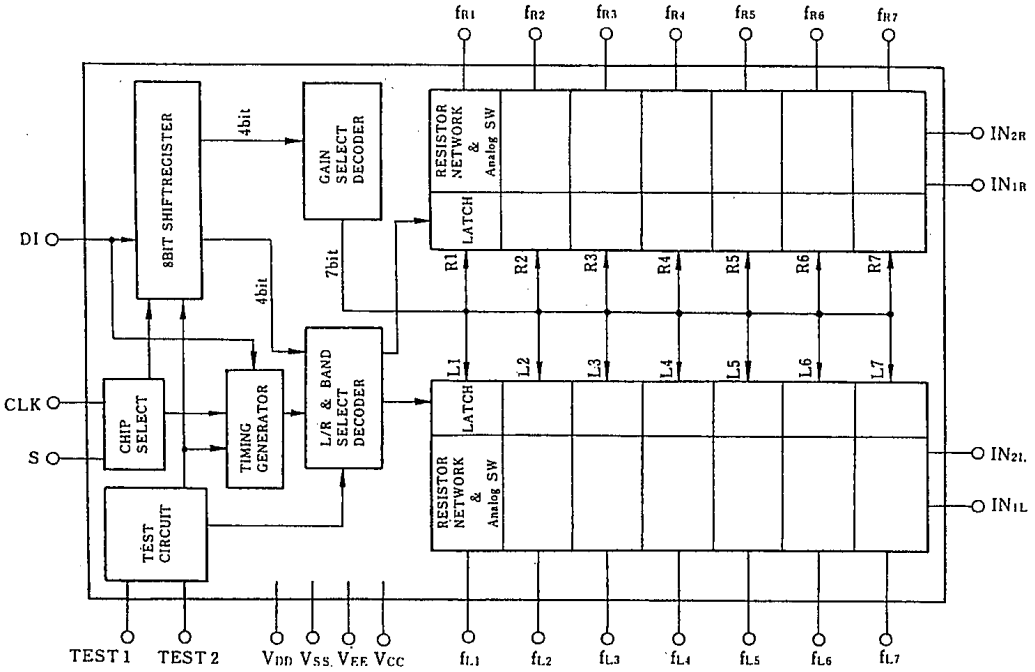
- 7 Bands Each for Left and Right Channels
- Stereo Application Graphic Equalizer
  Each Channel Independent Operation
- Maximum Boost and Cut --- ±12dB
- Boost and Cut Step --- ±2dB
- 8-bit Serial Data for the Equalizing
- Flat Level Setting Function
- Operating Voltage --- 7.5~15V
- Package Outline --- SDMP 30 / SDIP 28
- C-MOS Technology

■ PIN CONFIGURATION



NJU7305M NJU7305L

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No	Symbol	Function
1	V_{DD}	Power source for Audio signal +7.5V
18	V_{SS}	GND 0V
14	V_{EE}	Power source for Audio signal -7.5V
15	V_{CC}	Power source for Logic +5.0V
2, 27	I_{N1L}, I_{N1R}	Audio signal input terminal. Connect to Op-amp inverting input.
3, 26	I_{N2L}, I_{N2R}	Audio signal input terminal. Connect to Op-amp non-inverting input.
4 to 10	f_{L1} to f_{L7}	Band pass filter connecting terminal.
19 to 25	f_{R1} to f_{R7}	(14 terminals for left/right)
11 12	TEST1 TEST2	Maker Testing terminals. Normally (except testing) connects to the V_{DD} terminal
13	S	Chip-select input terminal.
16	DI	Serial data input terminal.
17	CLK	Clock signal input terminal.

■ FUNCTIONAL DESCRIPTION

(1) Data set and code format

The setting of each band is performed by two signals of data and clock as shown in Fig.1.

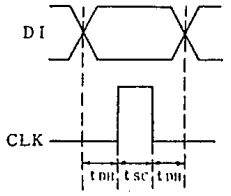
The 8 bits serial data including the information of channel selection (left/right), band selection and its gain are input from DI terminal.

The clock signal input from the CLK terminal shifts the serial data input form DI terminal into the shift register.

The 9th clock signal is used as latch pulse to latch all 8 bits of parallel data in the shift register.

All "1" of 8 bits code are special code to set 0dB for all bands at once. This function is useful for Power On initialization or flat level setting.

< Data and Shift Clock >



The shift clock should be risen after 1μs from the data changing.
t_{SC}=1μs(MIN)
t_{DH}=1μs(MIN)

< Time Chart >

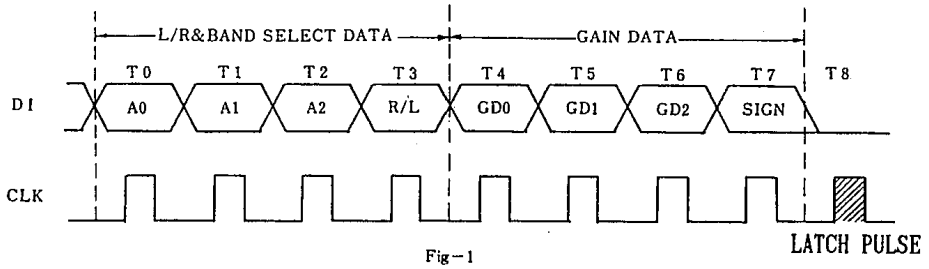


Fig-1

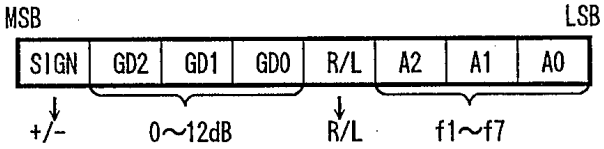
The 9th shift clock is used for the latch pulse. In this time the data must be "0" otherwise (the data is "1") the 9th clock shifts the data and the following clock signal latch the data when input data is "0".

If the error data is latched, the correct data must be set again from the top.

Note: The clock line should be shielded from the noise.

< Data Format >

The data is input by the LSB first format as shown bellow. And the gain data GD2 to GD0, left/right and band selection data are also shown in bellow.



GAIN DATA CODE

GAIN	SIGN	GD2	GD1	GD1
12	0	1	1	0
10	0	1	0	1
8	0	1	0	0
6	0	0	1	1
4	0	0	1	0
2	0	0	0	1
0dB	0	0	0	0
-2	1	0	0	1
-4	1	0	1	0
-6	1	0	1	1
-8	1	1	0	0
-10	1	1	0	1
-12	1	1	1	0

R/L & BAND SELECT DATA CODE

R/L	A2	A1	A0	BAND
0	0	0	0	f_{L7}
0	0	0	1	f_{L6}
0	0	1	0	f_{L5}
0	0	1	1	f_{L4}
0	1	0	0	f_{L3}
0	1	0	1	f_{L2}
0	1	1	0	f_{L1}
1	1	1	0	f_{R1}
1	1	0	1	f_{R2}
1	1	0	0	f_{R3}
1	0	1	1	f_{R4}
1	0	1	0	f_{R5}
1	0	0	1	f_{R6}
1	0	0	0	f_{R7}

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(2) Chip Select Function

S terminal is a chip select terminal. When the code "1" is input to the S terminal form CPU or other controller, the clock input is activated and the data will be written into the NJU7305(select status). When the code "0" is input to the S terminal, the clock input is not activated and the data will not be written into the NJU7305(unselect status).

S terminal	mode	f u n c t i o n
1	Select	The clock input is activated and the data is written into the NJU7305.
0	Unselect	The clock input is not activated and the data is written into the NJU7305.

(3) Power on initialization

The NJU7305 is not incorporated the power on initialization circuits, so that the internal circuits are not defined when the power is turned on. Therefore all "1" of 8 bits serial data with shift clock and latch pulse (9th clock) are required to set the flat state as explained before.

The internal circuits of NJU7305 are initialized by the above operation, then following input will be accepted.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}-V_{EE}	16	V
	V_{CC}	V_{SS}～V_{SS}+7(V_{DD}≧V_{CC})	
Input Voltage	V_{IN}	V_{SS}-0.3～V_{CC}+0.3 (DI,CLK,S)	V
		V_{EE}-0.3～V_{DD}+0.3(I_{N1L}～I_{N2L},I_{N1R}～I_{N2R})	
Power Dissipation	PD	200	mW
Operating Temperature	T_{opr}	-20 ～ +75	℃
Storage Temperature	T_{stg}	-40 ～ +125	℃

■ ELECTRICAL CHARACTERISTICS

(V_{SS}=0V,V_{DD}≧V_{CC}>V_{SS}≧V_{EE},Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}-V_{EE}	V_{EE}≧-7.5V	7.5	10	15	V
	V_{CC}		4.5	5.0	5.5	
Operating Current	I_{DD}	V_{DD}-V_{EE}=15V			1	mA
	I_{CC}	V_{CC}=5V			1	
Input Voltage	V_{IH}	CLK,DI,S	0.8V_{CC}		V_{CC}	V
	V_{IL}	Terminals	0		0.2V_{CC}	
Input Pulse Width	t_{PW}	CLK	1			μS
Setup Time	t_{SU}	DI	1			μS
Holding Time	t_{HLD}	DI	1			μS
Operating Frequency	f_{OPR}	CLK			330	kHz
Total Harmonics Distortion	THD1	Flat Status, f=20kHz		0.005	0.01	%
	THD2	Flat Status, f= 1kHz		0.0015	0.003	
	THD3	Boost Status, f=20kHz		0.04	0.10	
	THD4	Boost Status, f= 1kHz		0.015	0.03	
		(Circuit 1)				
Crosstalk	CT	(Circuit 2)		55		dB
Setting Error	ΔB	V_{DD}-V_{EE}=15V (Circuit 1)	-1		1	dB
Analog SW Off Leakage Current	I_{off}	f_{L1}～f_{L7} f_{R1}～f_{R7}			10	μA

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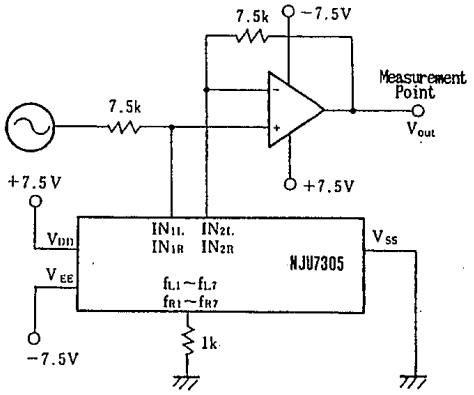
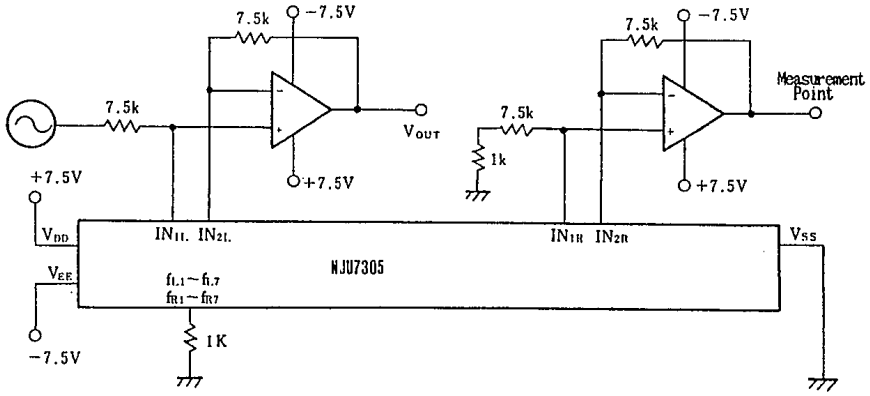
■ MEASUREMENT CIRCUITS

Circuit 1



Circuit 2



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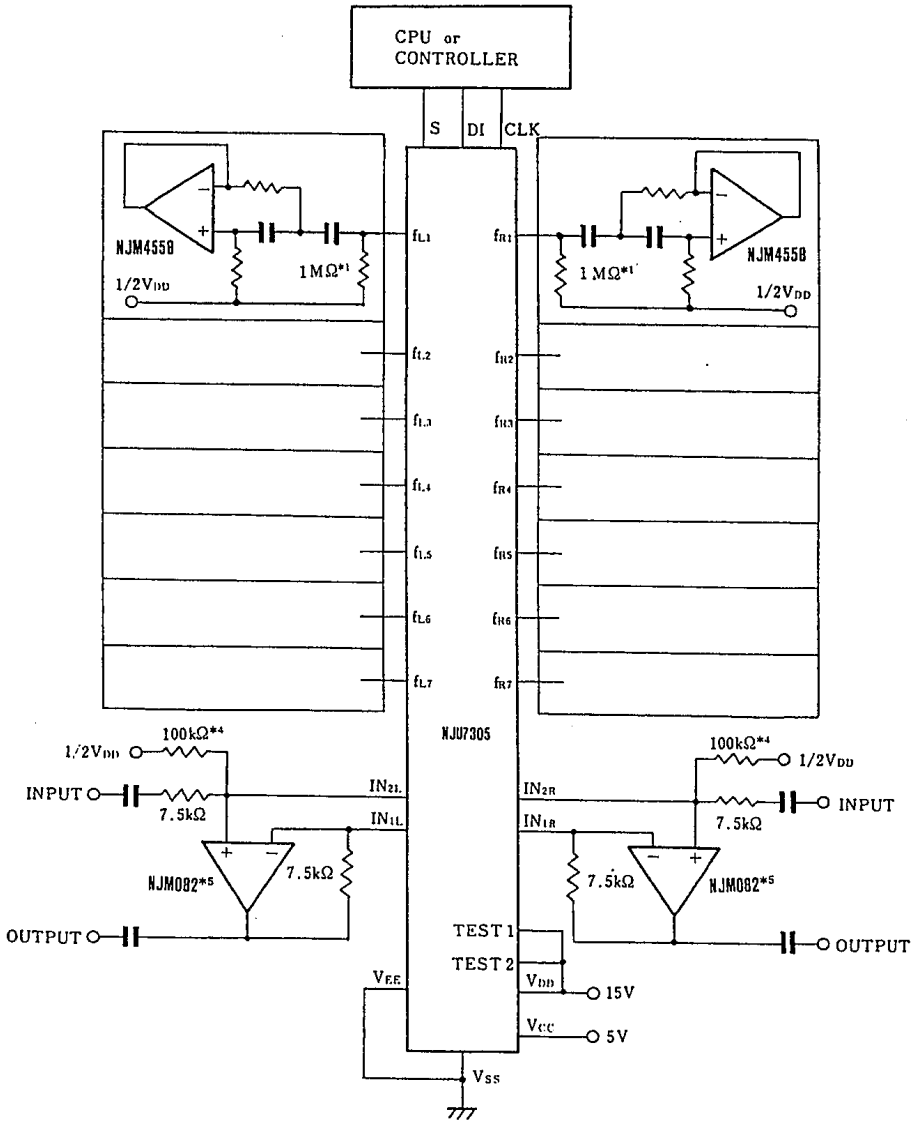
APPLICATION CIRCUIT 1

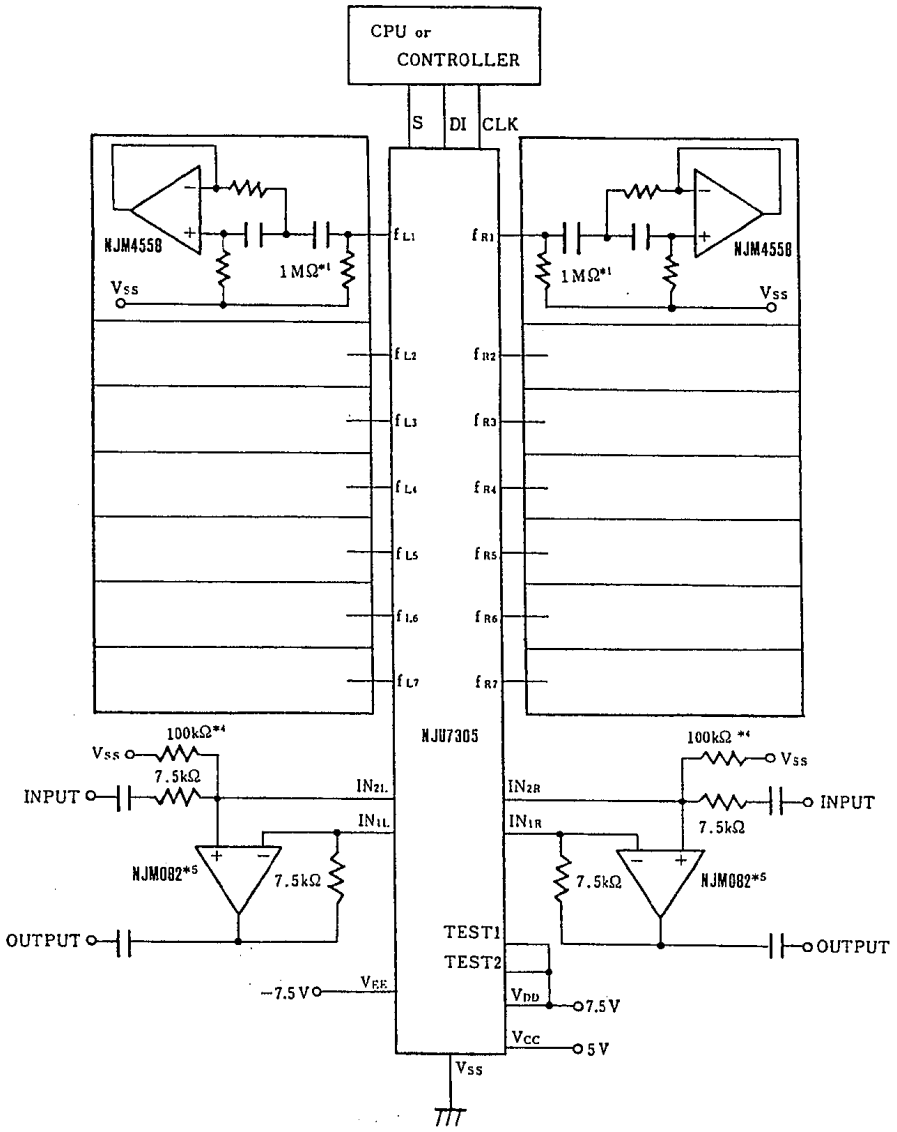
< Single power supply operation >



*1) In order to reduce the pop-noise, connecting $f_L1 \sim f_L7$, $f_R1 \sim f_R7$ to 1/2 V_{DD} by 1MΩ resistance is recommended.
*2) The best conditions for 2dB/step are as follows:
V_{DD} = 15V
OP-amp feedback resistance: 7.5kΩ
Equivalent LC resonant impedance: 1kΩ
*3) TEST1 and TEST2 terminals are normally connecting to the V_{DD} terminal.
*4) In order to keep off noise input, connecting to 1/2 V_{DD} by 100kΩ resistance is recommended.
*5) J-FET input OP-AMP is recommended.

■ APPLICATION CIRCUIT 2

< Dual power supply operation >



*1) In order to reduce the pop-noise, connecting $f_L1 \sim f_L7$, $f_R1 \sim f_R7$ to V_{SS} by 1MΩ resistance is recommended.
*2) The best conditions for 2dB/step are as follows:
V_{DD} = 7.5V, V_{EE} = -7.5V
OP-amp feedback resistance: 7.5kΩ
Equivalent LC resonant impedance: 1kΩ
*3) TEST1 and TEST2 terminals are normally connecting to the V_{DD} terminal.
*4) In order to keep off noise input, connecting to 1/2 V_{DD} by 100kΩ resistance is recommended.
*5) J-FET input OP-AMP is recommended.

MEMO