PRELIMINARY

11-BIT PARALLEL TO SERIAL CONVERTER

■ GENERAL DESCRIPTION

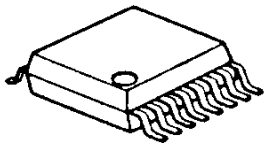
The **NJU3754** is an 11-bit parallel to serial converter especially applying to MCU input port expander. It can operate from 2.7V to 5.5V.

The **NJU3754** requires only 3-port of MCU for data transmission and realizes the effective input port assignment.

The status of the input ports is output through a latch circuit, a shift register and a 3-state buffer as the serial data synchronizing with the serial clock. The hysteresis input circuit of the serial clock terminal realizes 5MHz and more operation.

Furthermore, pull-up resistors on chip of P0 to P10 terminals reduce external components for key-scan circuit, etc.

■ PACKAGE OUTLINE

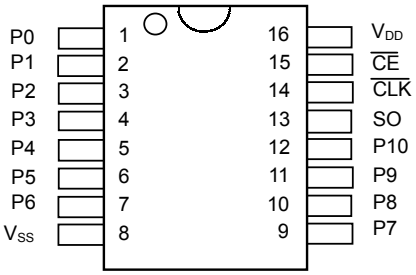


NJU3754V

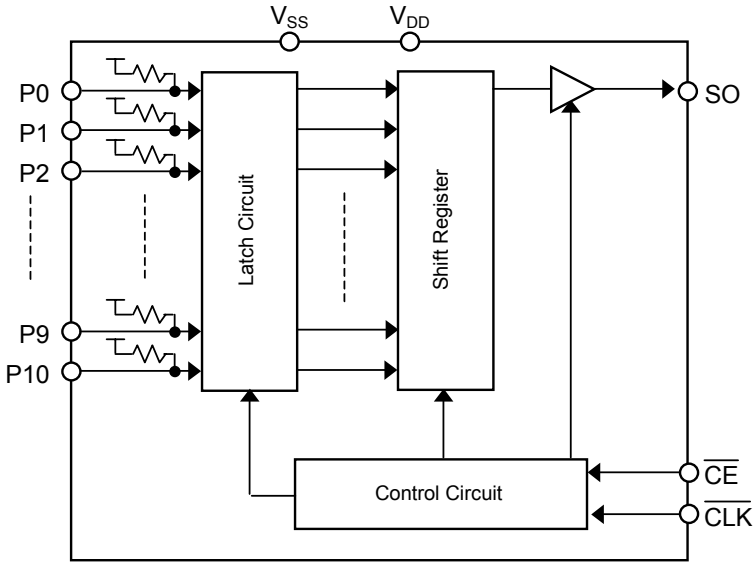
■ FEATURES

- 11-Bit Parallel In Serial Out
- 3-line Serial Interface Output
- Hysteresis Input 0.5V typ at 5V
- Maximum Operating Frequency 5MHz and more
- Operating Voltage 2.7 to 5.5V
- C-MOS Technology
- Package Outline SSOP16

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

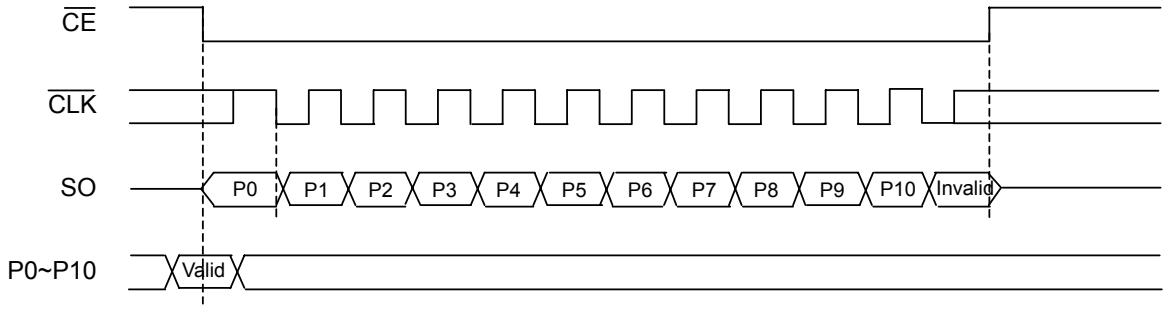
No.	SYMBOL	I/O	FUNCTION
1	P0	I	Parallel Data Input Terminals (with pull-up resistors)
2	P1	I	
3	P2	I	
4	P3	I	
5	P4	I	
6	P5	I	
7	P6	I	
8	V_{SS}	-	Ground
9	P7	I	Parallel Data Input Terminals (with pull-up resistors)
10	P8	I	
11	P9	I	
12	P10	I	
13	SO	O	Serial Data Output Terminal
14	$\overline{CLK}$	I	Serial Clock Input Terminal
15	$\overline{CE}$	I	Chip Enable Input Terminal
16	V_{DD}	-	Power Supply Terminal (2.7 to 5.5V)

■ FUNCTIONAL DESCRIPTION

At the falling edge of $\overline{CE}$ terminal, the status of P0 to P10 terminal is latched and transferred to the shift register. At the mean time, the P0 data is output from SO terminal. While $\overline{CE}$ terminal is “L”, the data from P1 to P10 in the shift register are synchronized with the falling edge of $\overline{CLK}$ terminal and output from SO terminal.

When $\overline{CE}$ terminal is “H”, SO terminal is high impedance.

Note 1) If the 11th falling edge and later are input to $\overline{CLK}$ terminal while $\overline{CE}$ is “L”, the 12th and the following data are invalid.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Range	V_{DD}	-0.3 ~ +7.0	V
Input Voltage Range	V_I	V_{SS}-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	300 (SSOP)	mW
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-65 ~+150	°C

Note 2) All voltage are relative to V_{SS}=0V reference.

Note 3) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC is used in the range specified in the DC electrical characteristics, or the electrical stress may cause malfunctions and impact on the reliability.

Note 4) To stabilize the IC operation, place decoupling capacitor between V_{DD}-V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS

(V_{DD}=2.7~5.5V, V_{SS}=0V, Ta=25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}			2.7	-	5.5	V
Operating Current	I_{DD}	V_{DD}=5.5V P0~P10=Open $\overline{CE}$=H, $\overline{CLK}$=L SO=No load		-	-	10	μA
Input Voltage	V_{IH}	P0~P10, $\overline{CLK}$, $\overline{CE}$ Terminals		0.7V_{DD}	-	V_{DD}	V
	V_{IL}			V_{SS}	-	0.3V_{DD}	V
High-level Input Current	I_{IH}	V_{DD}=5V, V_I=5V P0~P10, $\overline{CLK}$, $\overline{CE}$ Terminals		-	-	1	μA
Low-level Input Current 1	I_{IL1}	V_{DD}=5V, V_I=0V $\overline{CLK}$, $\overline{CE}$ Terminals		-1	-	-	μA
Low-level Input Current 2	I_{IL2}	V_{DD}=5V, V_I=0V P0~P10 Terminals		-100	-40	-15	μA
Output Voltage	V_{OH}	I_{OH}=-0.4mA	SO Terminal	V_{DD}-0.4	-	V_{DD}	V
	V_{OL}	I_{OL}=+3.2mA		V_{SS}	-	0.4	V
3-State Leakage Current	I_{TSL}	SO Terminal $\overline{CE}$=H		-2	-	2	μA

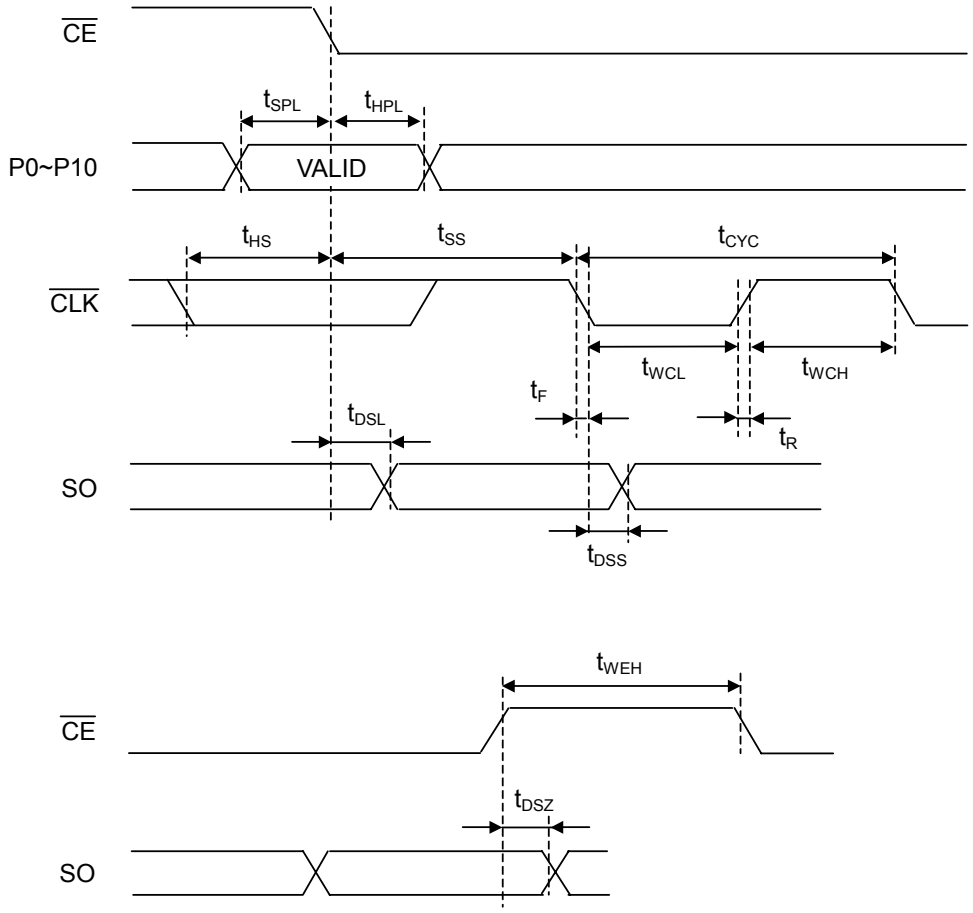
■ SWITCHING CHARACTERISTICS

(V_{DD}=2.7~5.5V, V_{SS}=0V, Ta=25°C, unless otherwise noted)

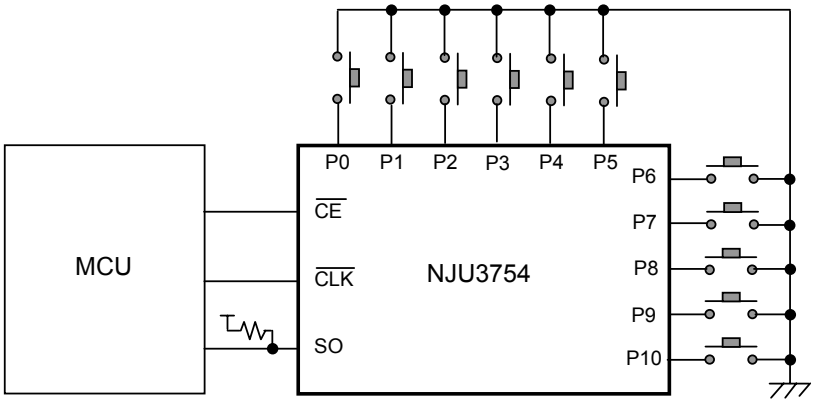
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
$\overline{CLK}$ Cycle Time	t_{CYC}	$\overline{CLK}$	200	-	-	ns
$\overline{CLK}$ Pulse Width (H)	t_{WCH}	$\overline{CLK}$	90	-	-	ns
$\overline{CLK}$ Pulse Width (L)	t_{WCL}	$\overline{CLK}$	90	-	-	ns
$\overline{CE}$ Pulse Width (H)	t_{WEH}	$\overline{CE}$	100	-	-	ns
$\overline{CE}$ Set-up Time before $\overline{CLK}$ Falling	t_{SS}	$\overline{CE}$ - $\overline{CLK}$	100	-		ns
$\overline{CE}$ Hold Time after $\overline{CLK}$ Falling	t_{HS}	$\overline{CLK}$ - $\overline{CE}$	100	-		ns
Parallel Data Set-up Time	t_{SPL}	P0~P10 - $\overline{CE}$	50	-	-	ns
Parallel Data Hold Time	t_{HPL}	$\overline{CE}$ - P0~P10	50	-	-	ns
SO Delay Time after $\overline{CE}$ Falling	t_{DSL}	$\overline{CE}$ - SO (Note 6)	-	-	50	ns
SO Delay Time after $\overline{CLK}$ Falling	t_{DSS}	$\overline{CLK}$ - SO (Note 6)	-	-	50	ns
SO Hold Time after $\overline{CE}$ Rising	t_{DSZ}	$\overline{CE}$ - SO (Note 6)	-	-	20	ns
Rise Time	t_R	$\overline{CLK}$ Terminal	-	-	20	ns
Fall Time	t_F	$\overline{CLK}$, $\overline{CE}$ Terminals	-	-	20	ns

Note 5) A 15kΩ pull-up or pull-down resistor and a 50pF capacitor on the SO terminal.
Note 6) All timings are based on 30% and 70% voltage level of V_{DD}.

■ TIMING CHARTS



■ APPLICATION CIRCUIT



[CAUTION]
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