DOLBY® PRO LOGIC II

Dolby Pro Logic II Decoder

■ General Description

The NJU26203A is a digital signal processor that provides the function of Dolby Pro Logic II, Bass Management, Multi channel input, and 5-band PEQ function.
The applications of NJU26203A are suitable for multi channel products such as Car Audio, DVD Receiver and speakers system.

■Package

NJU26203AV

■ Features

-Software

- Dolby Pro Logic II (Max 5.1ch Output)
- Bass Management
- Multi channel input
- 5-band PEQ
- Center Mixer, Rear Center Mixer
- Master Volume

-Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 4 Output ports
- Digital Audio Format : I^2S 24bit, left-justified, right-justified, BCK : 32fs/64fs
- Master / Slave Mode
- Microcomputer Interface
  I^2C Bus (Standard-mode/100kbps, Fast-mode/400kbps)
  4-Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Operating Voltage : V_{DD} = V_{DDPLL} = 1.8V
  : V_{DDIO} = 3.3V
- Input Terminal : +5.0V Input tolerant
- Package : SSOP44 (Pb-Free)

* The detail hardware specification of the NJU26203A is described in the " NJU26200 Series Hardware Data Sheet".

■ Hardware Block Diagram

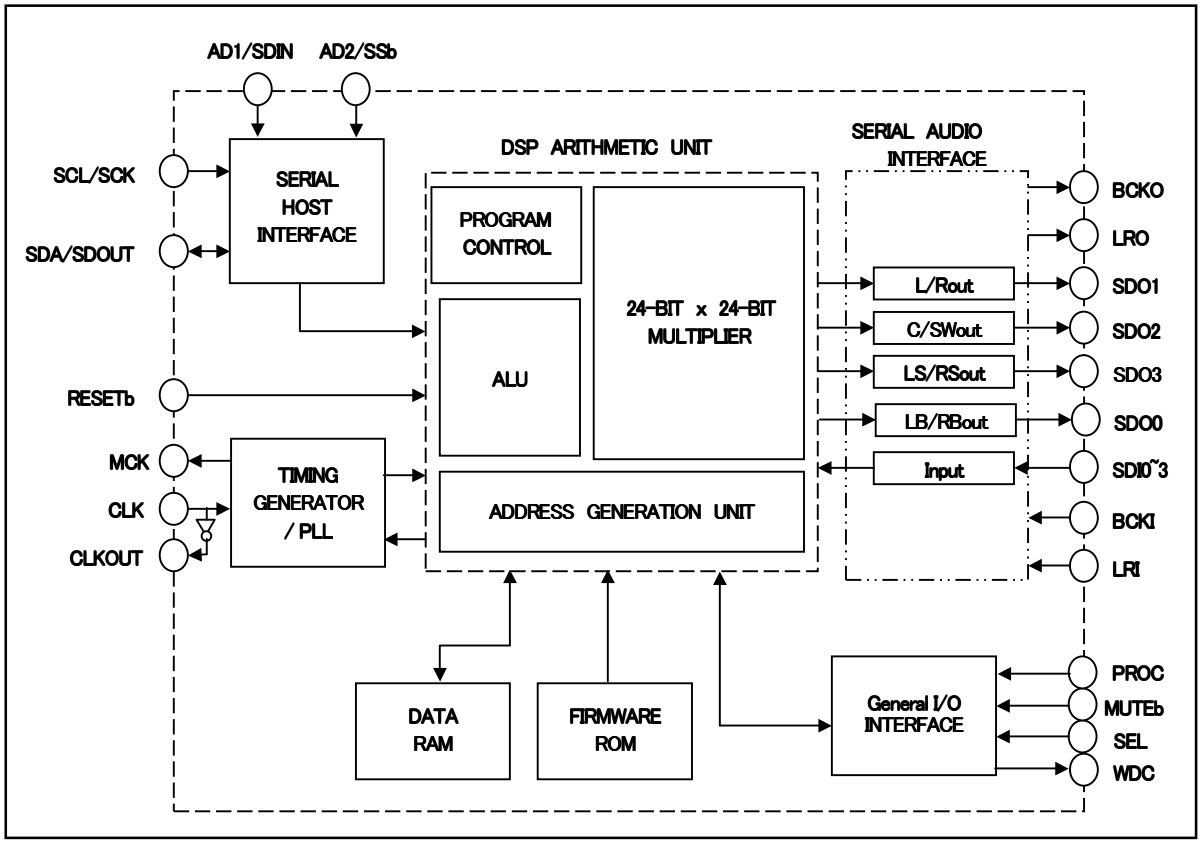
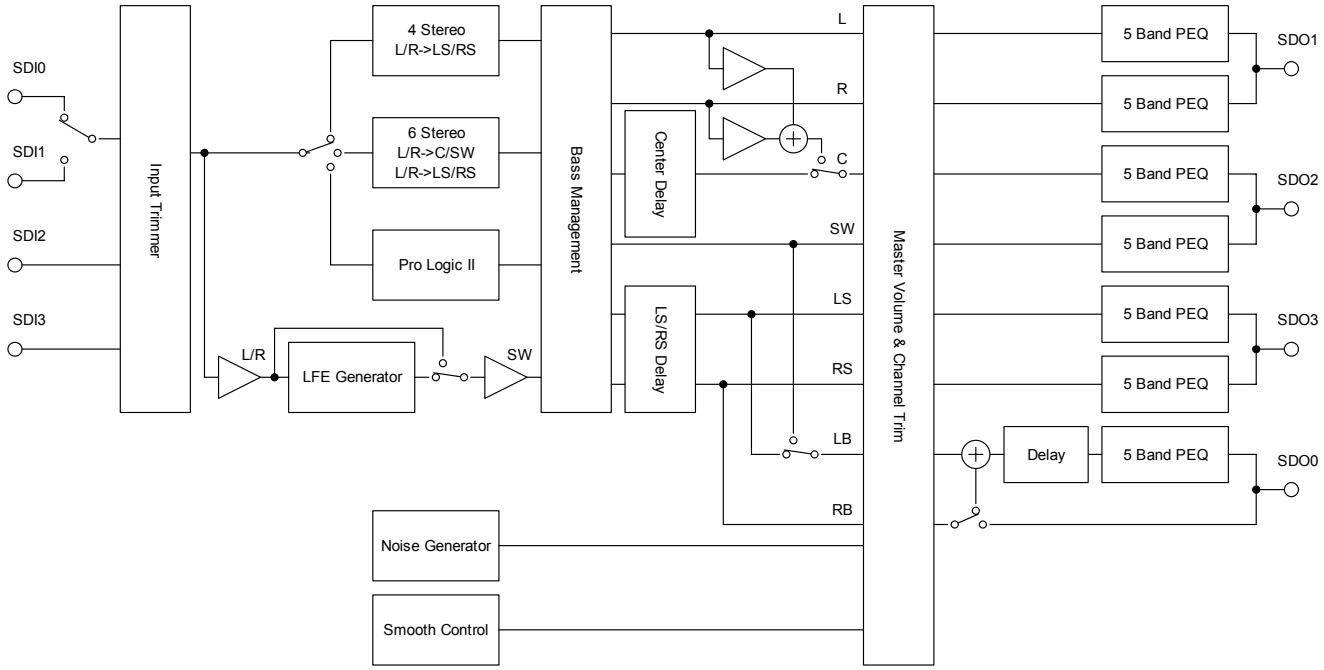


Fig. 1 NJU26203A Hardware Block Diagram

■ Function Block Diagram



*Center Mix is effective only at the time of 4ch Stereo Mode or Multi Input Mode choice.

*LFE Generator ON/OFF is effective only at the time of 4ch Stereo Mode choice.

Fig. 2 NJU26203A Function Block Diagram (Firmware)

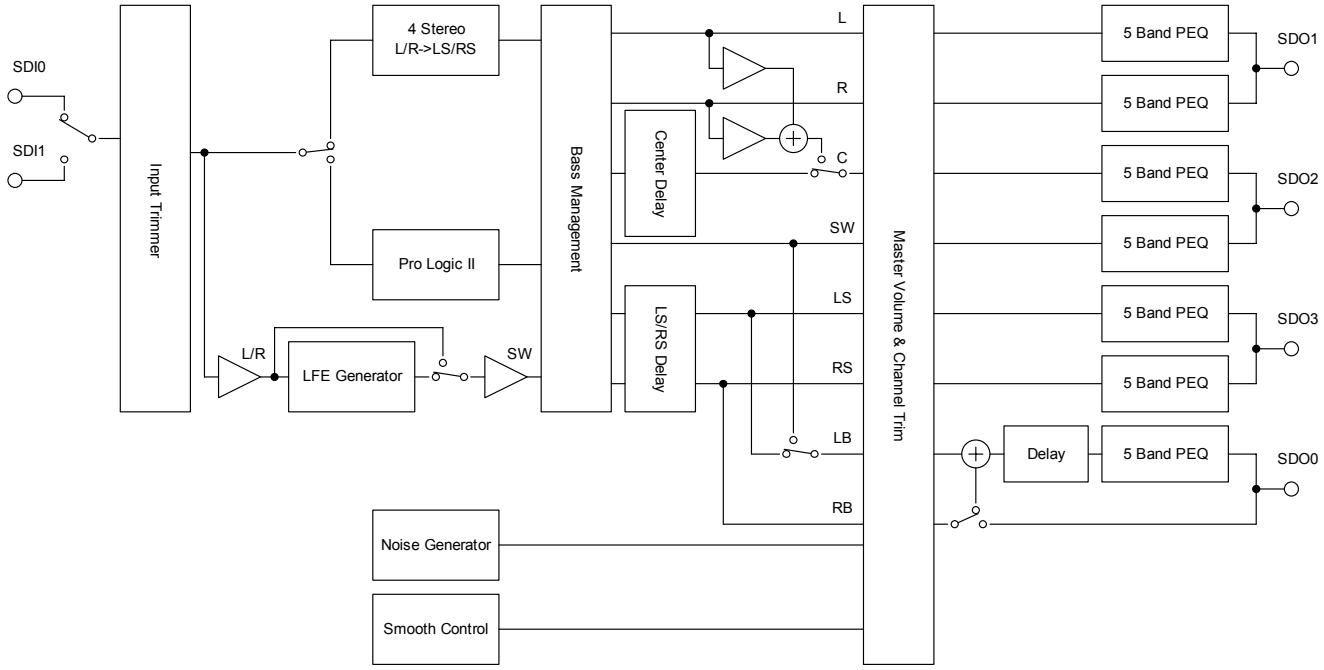


Fig. 3 NJU26203A Function Block Diagram (Stereo Input)

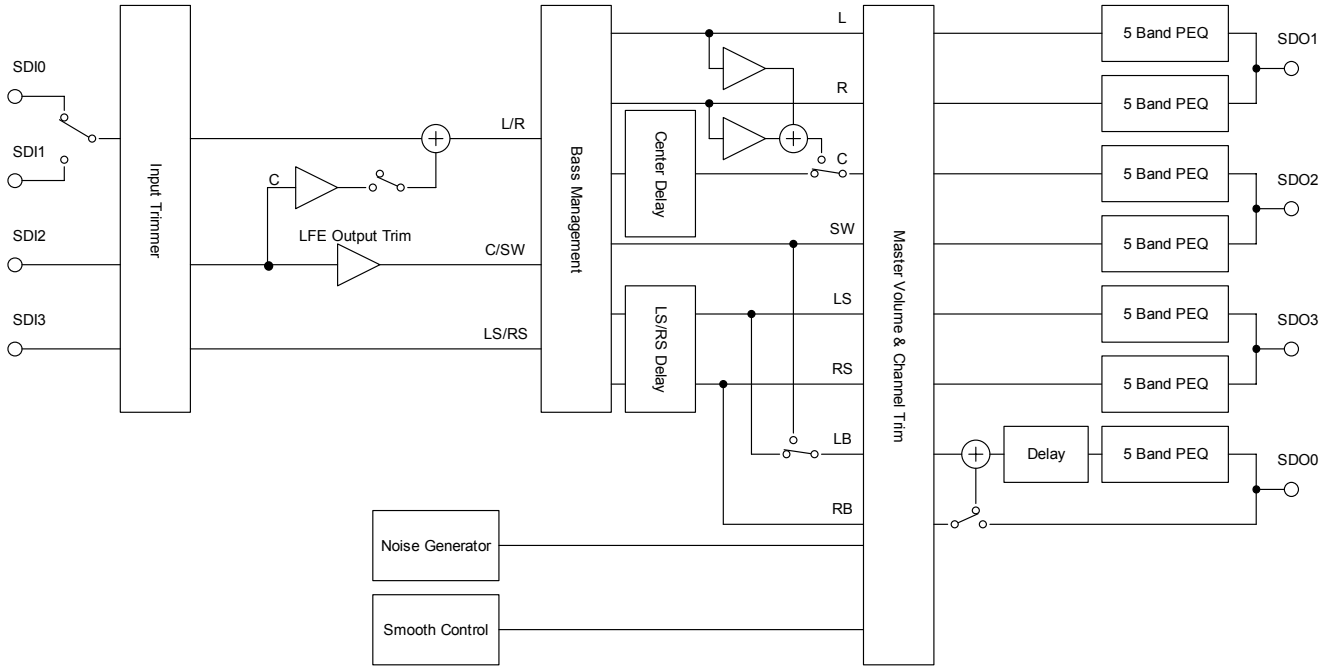


Fig. 4 NJU26203A Function Block Diagram (Multi channel input)

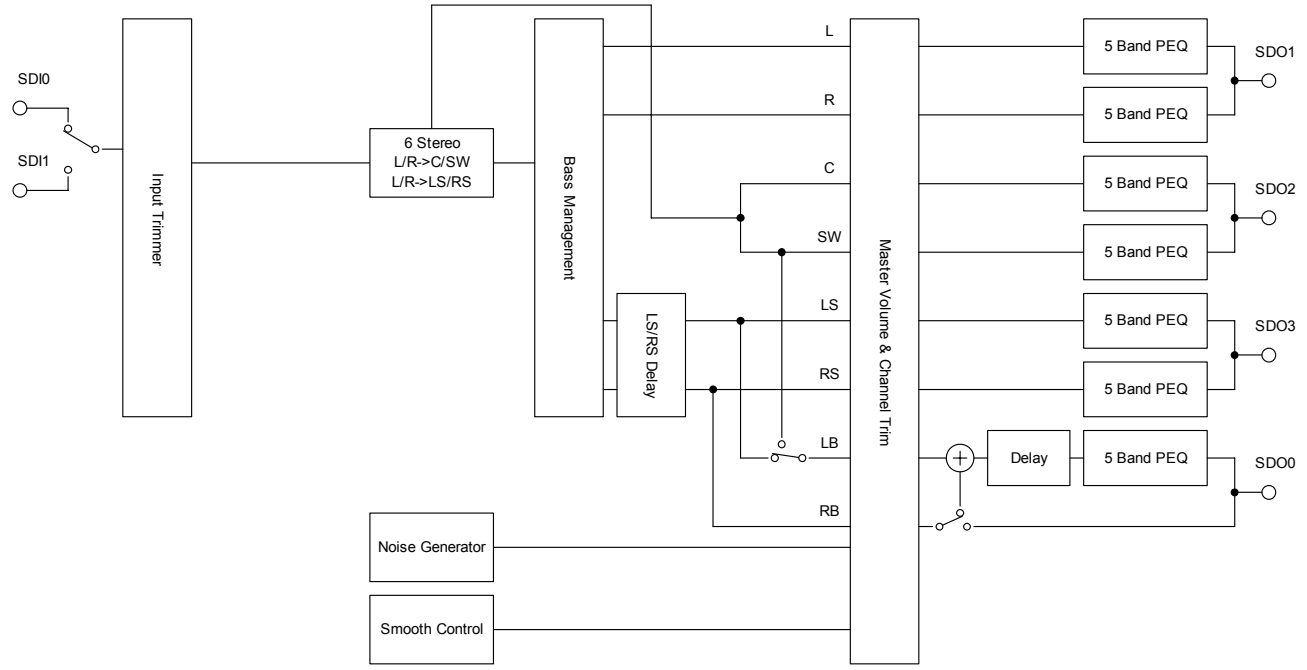


Fig. 5 NJU26203A Function Block Diagram (Stereo Input, NON-FADER (6ch Stereo))

Pin Configuration

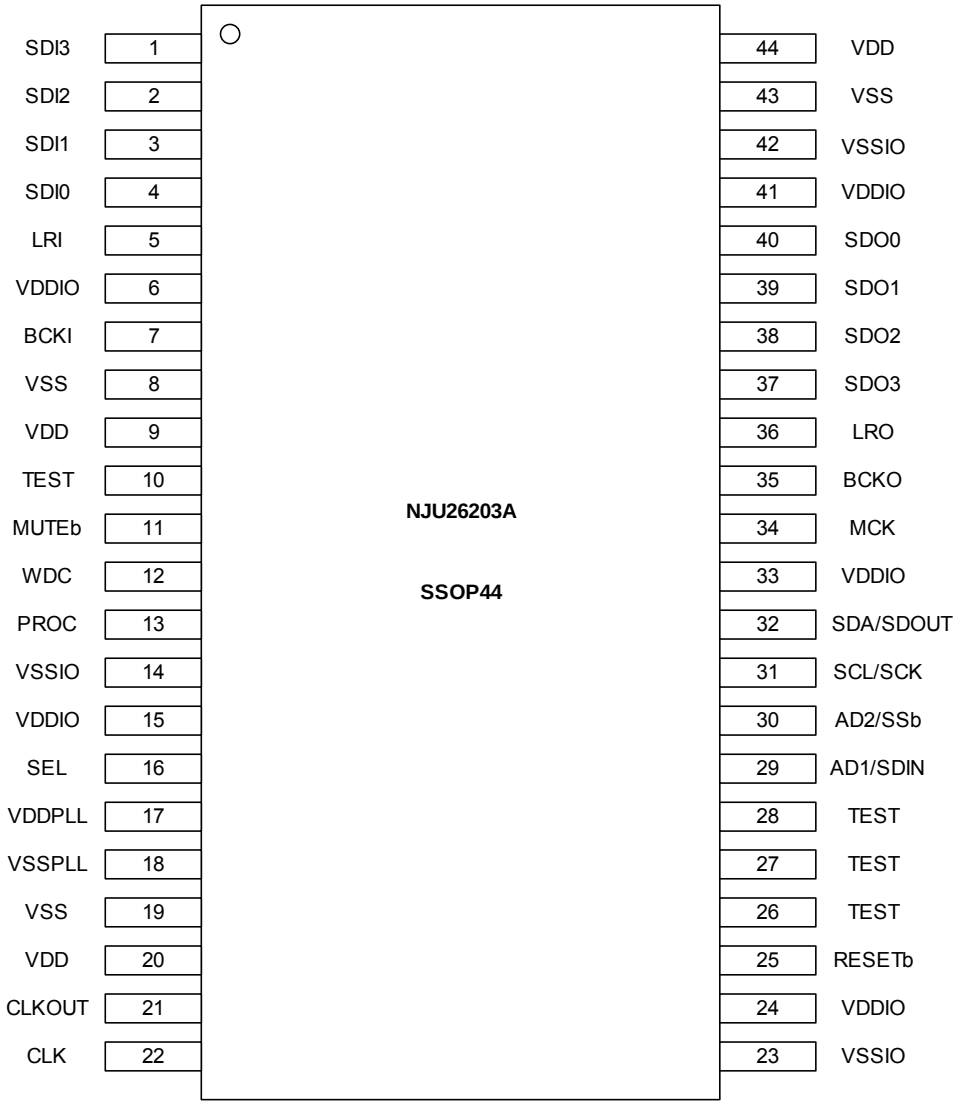


Fig. 6 NJU26203A Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Function
1	SDI3	I	Audio Data Input ch.3 (LS/RS)
2	SDI2	I	Audio Data Input ch.2 (C/SW)
3	SDI1	I	Audio Data Input ch.1 (L/R)
4	SDI0	I	Audio Data Input ch.0 (L/R)
5	LRI	I	LR Clock Input
6	VDDIO	-	I/O Power Supply +3.3V
7	BCKI	I	Bit Clock Input
8	VSS	-	DSP Core Power Supply GND
9	VDD	-	DSP Core Power Supply +1.8V
10	TEST *	I	for test connect with VSSIO through 3.3-ohm resistance.
11	MUTEb *	I	Master Volume Status after reset '1': 0dB, '0': Mute
12	WDC *	OD	Watchdog Clock output pin (Open drain output)
13	PROC *	I	Signal Processing after reset '1': Normal Processing, '0': Waiting for a Command without Processing
14	VSSIO	-	I/O Power Supply GND
15	VDDIO	-	I/O Power Supply +3.3V
16	SEL	I	Host Interface Selection '1': Serial Interface, '0': I^2C bus
17	VDDPLL	-	PLL Power Supply +1.8V
18	VSSPLL	-	PLL Power Supply GND
19	VSS	-	DSP Core Power Supply GND
20	VDD	-	DSP Core Power Supply +1.8V
21	CLKOUT	O	OSC Clock Output
22	CLK	I	OSC Clock Input (12.288MHz)
23	VSSIO	-	I/O Power Supply GND
24	VDDIO	-	I/O Power Supply +3.3V
25	RESETb	I	Reset (RESETb='0': DSP Reset)
26	TEST	I	for test (connect to VDDIO)
27	TEST	I	for test (connect to VSSIO)
28	TEST	I	for test (connect to VSSIO)
29	AD1/SDIN	I	I^2C Address (I^2C mode) / Serial In (4-wire serial mode)
30	AD2/SSb	I	I^2C Address (I^2C mode) / Serial enable (4-wire serial mode)
31	SCL/SCK	I	I^2C SCL (I^2C mode) / Serial clock (4-wire serial mode)
32	SDA/SDOUT	I/O	I^2C SDA (I^2C mode) / Serial Out (4-wire serial mode)
33	VDDIO	-	I/O Power Supply +3.3V
34	MCK	O	A/D, D/A clock output (buffer output of a CLK pin)
35	BCKO	O	Bit Clock Output
36	LRO	O	LR Clock Output
37	SDO3	O	Audio Data Output ch.3 (LS/RS)
38	SDO2	O	Audio Data Output ch.2 (C/SW)
39	SDO1	O	Audio Data Output ch.1 (L/R)
40	SDO0	O	Audio Data Output ch.0 (LB/RB)
41	VDDIO	-	I/O Power Supply +3.3V
42	VSSIO	-	I/O Power Supply GND
43	VSS	-	DSP Core Power Supply GND
44	VDD	-	DSP Core Power Supply +1.8V

Note : I : Input
O : Output
OD : Open Drain Output
I/O : Bi-directional
Pins symbol with * : Connect with VDDIO or VSSIO through 3.3kΩ resistance

■ Audio Interface

The NJU26203A audio interface provides industry serial data formats of I^2S, MSB-first Left-justified or MSB-first Right-justified. The NJU26203A audio interface provides four data inputs, SDI0, SDI1, SDI2 and SDI3, and four data outputs, SDO0, SDO1, SDO2 and SDO3 as shown in table 2 and 3. The input serial data is selected by the firmware command.

Table 2 Serial Audio Input Pin

Pin No.	Symbol	Description	
		Stereo input	Multi channel input
4	SDI0	Audio Data Input (L/R)	Audio Data Input (L/R)
3	SDI1	(SDI0/SDI1 pin select)	(SDI0/SDI1 pin select)
2	SDI2	None	Audio Data Input 2 (C/SW)
1	SDI3	None	Audio Data Input 3 (LS/RS)

Table 3 Serial Audio Output Pin

Pin No.	Symbol	Description
40	SDO0	Audio Data Output 0 (LB/RB)
39	SDO1	Audio Data Output 1 (L/R)
38	SDO2	Audio Data Output 2 (C/SW)
37	SDO3	Audio Data Output 3 (LS/RS)

■ Host Interface

The NJU26203A can be controlled via Serial Host Interface (SHI) using either of two serial bus formats : I^2C bus or 4-Wire serial bus. Data transfers are in 8 bits packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The detail I^2C bus and 4-Wire Serial bus information are described in the 'NJU26200 Series Hardware Data Sheet'.

Table 4 Serial Host Interface Pin Descriptions

Pin No.	Symbol	Setting	Host Interface
16	SEL	Low	I^2C Bus Interface
		High	4-Wire Serial Interface

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C /Serial)	I^2C bus Interface	4-Wire Serial Interface
29	AD1/SDIN	I^2C Address Select Bit1	Serial data input
30	AD2/SSb	I^2C Address Select Bit2	Slave select
31	SCL/SCK	Serial Clock	Serial Clock
32	SDA/SDOUT	Serial Data Input/Output (Open Drain output)	Serial data output (CMOS Output)

Note: When I^2C Bus is selected, the SDA/SDOUT pin is a bi-directional Open Drain output. This pin, which is assigned for I^2C Bus, requires a pull-up resistance.
When 4-Wire Serial bus is selected, the SDA/SDOUT pin is CMOS output.
The SDA/SDOUT pin isn't 5.0V Input tolerant.

■ I²C Bus

When the NJU26203A is configured for I²C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. The SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6)

Table 6 I²C Bus Interface Slave address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	

* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".
* SLAVE address is 0 when R/W is "W". SLAVE address is 1 when R/W is "R".

Note:
Both "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" data transfer rate are supported.

■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. SDOUT is always CMOS output. SDOUT does not require a pull-up resistance.

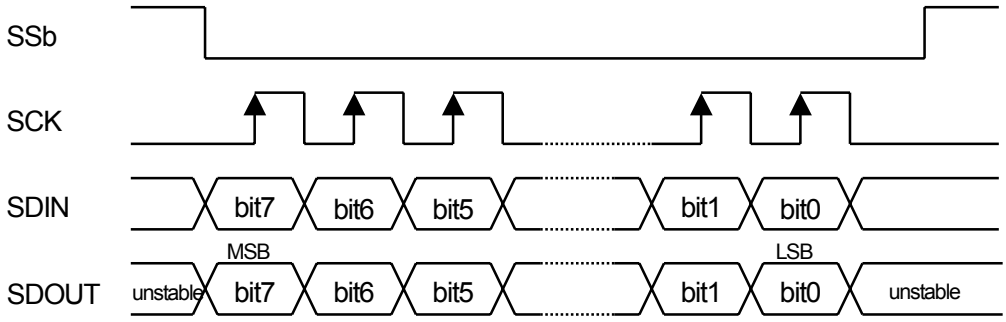


Fig. 7 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High".
When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.
After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High".

■ Pin setting

The NJU26203A operates default command setting after resetting the NJU26203A. In addition, the NJU26203A restricts operation at power on by setting PROC pin and MUTEb pin. These pins are input pin. However, these pins operate as bi-directional pins. Connect with V_{DDIO} or V_{SSIO} through 3.3kΩ resistance.

Table 7 Pin setting

Pin No.	Symbol	Setting	Function
13	PROC	"High"	The NJU26203A operates default setting after reset.
		"Low"	The NJU26203A does not operate after reset. Sending start command is required for starting operation.
11	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26203A outputs clock pulse through WDC (Pin No.12) during normal operation. The WDC clock is useful to check the status of the NJU26203A operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26203A. When the WDC clock pulse is lost or not normal clock cycle, the NJU26203A does not operate correctly. Then reset the NJU26203A and set up the NJU26203A again. The WDC clock is able to be variable for 0msec to 100msec by command. Default setting of WDC clock is 100msec.

The WDC pin is open drain output. The WDC pin setting (Table 8)

Table 8 WDC pin setting

Pin No.	Symbol	Setting	
12	WDC	WDC pin is used.	Connect with V_{DDIO} through 3.3kΩ resistance.
		WDC pin is not used.	Connect with V_{SSIO} through 3.3kΩ resistance. Do not open WDC pin.

Note: The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing.
In slave mode, when there is no input of BCKI/LRI, WDC can't output.
It is required to set up a sampling rate correctly.

■ Firmware Command Table

Host processor can control the NJU26203A via I^2C bus or 4-Wire serial bus interface. The following table summarizes the available user commands.

Table 9 Command Table

No.	Command Description
1	Set Task Command
2	System State Command
3	Sample rate Select Command
4	Smooth Control Config Command
5	Master Volume Control Command
6	Channel Trim Control Command
7	Input Trim Control Command
8	LFE Trim Control Command
9	Center Mix Trim Control Command
10	Pro Logic II Mode Command
11	Center Delay Control Command
12	Surround Delay Control Command
13	Bass Management Config Command
14	PNG Mode Command
15	EQ Channel Select Command
16	EQ Mode Select Command
17	EQ f0 Control Command
18	EQ Q Control Command
19	EQ Gain Control Command
20	Watch Dog Timer Command
21	LB ch Output Select Command
22	LFE f0 Control Command
23	LB Delay Control Command
24	Firmware Version Number Request Command
25	DSP Reset Command
26	Start Command
27	Nop Command

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (Dolby) is required.

■ Response of status

NJU26203A returns the response of 4 types to the host controller.

Table 10 Response of status

Response	Command	Remark
Status : Command Accepted	0x80	Reception OK
Status : Command Error	0x81	Reception ERROR
Status : Command Process	0x82	Command processing
Status : Not Ready	0x83	Initialization

■ License Information

The Word “DOLBY”, “Pro Logic II” and the double D mark are trademarks of Dolby Laboratories.
The NJU26203A can only be delivered to licensees of Dolby Laboratories.
Please refer to the licensing application manual issued by Dolby Laboratories.