PM5364

TUPP™ 2488

SONET/SDH Tributary Unit Payload Processor for 2488.32 Mbit/s Interfaces

Data Sheet

Released

Issue No. 7: August 2004

Legal Information

Copyright

PMC-2011334(R7), ref PMC-2011064(P6)

Disclaimer

None of the information contained in this document constitutes an express or implied warranty by PMC-Sierra, Inc. as to the sufficiency, fitness or suitability for a particular purpose of any such information or the fitness, or suitability for a particular purpose, merchantability, performance, compatibility with other parts or systems, of any of the products of PMC-Sierra, Inc., or any portion thereof, referred to in this document. PMC-Sierra, Inc. expressly disclaims all representations and warranties of any kind regarding the contents or use of the information, including, but not limited to, express and implied warranties of accuracy, completeness, merchantability, fitness for a particular use, or non-infringement.

In no event will PMC-Sierra, Inc. be liable for any direct, indirect, special, incidental or consequential damages, including, but not limited to, lost profits, lost business or lost data resulting from any use of or reliance upon the information, whether or not PMC-Sierra, Inc. has been advised of the possibility of such damage.

Trademarks

For a complete list of PMC-Sierra's trademarks, see our web site at http://www.pmc-sierra.com/legal/.

Other product and company names mentioned herein may be the trademarks of their respective owners.

Patents

The technology discussed in this document may be protected by one or more of the following patent grants:

U.S. Patent No. 6,603,776. Other relevant patent grants and patent applications may also exist.

Contacting PMC-Sierra

PMC-Sierra
8555 Baxter Place
Burnaby, BC
Canada V5A 4V7

Tel: +1 (604) 415-6000
Fax: +1 (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Revision History

Issue No.	Issue Date	Details of Change
7	August 2004	Updated section 22 Mechanical Information. Updated section 16.1 Power Requirement. Updated Section 19.8 Transmitter Electrical Characteristics. Updated Section 19.9 Receiver Electrical Characteristics. Updated Section 10.6.7 VTPA description to indicate overhead transparency is not supported. Updated section 13.12 RASIO™ CML Reset Sequence. Updated section 13.16 Loopbacks. Updated section 13.22 JTAG Support. Updated The TUPP 2488 Microprocessor Interface Read Access table located in Section 18: Microprocessor Interface Timing Characteristics. Added order information. Updated RTOP336 description in the Payload Processor Subsystem functional description. Updated Table 40 Overwrite Function Lookup Table. Updated section 10.5.1 Receive High Order Path Processor (RHPP_R) description. Removed some contents in section 10.8.1 SONET/SDH High Order Pointer Interpreter (SHPI) because it duplicates with the contents in section 10.5.1. Updated section 13.9.11 SARC-48 Operation. Added VTPA IPAIS configurations in AU3 to AU4 Tributary Mode 2 in the operation section. Updated section 13.9 HPOH Subsystem Operation. Updated 14.9 High Order Receive Path Alarm description. Added “The two opportunities are mostly identical, but they could be different when HRALM transitions in a frame depending on the frame timing.” Added performance monitor clock description in the operation section. Changed STS48_EN_TST bit read and write address. Changed CML receive differential return loss. The 10.5dB value should be the MIN differential return loss. The MAX and Typical values are left blank. Changed VIH ranges from 1.7 (min) to 3.6 (max) in the DC Characteristic for 2.5V LVCMOS table. Fixed the table Serial TelecomBus Character Encoding. Added K28.4 encoding. Removed LPT mode. Updated Table Boundary Scan Register. Reserved pin number D26, C26, B26, A26, AP10, AN10, AM10, and AL10 were changed to be left floating. Disclosed the SCANB pin. It is required that this pin is tied to VDDO.
6	December 2003	Issue 6 data sheet created. Reflects revision B of the TUPP2488. Refer to Issue 5 for revision A. Changes made: Updated patent info Updated feature description, Section 2.2.2, to reflect new TASR (formerly TSNCPP) functionality: added bullet to describe per STS-1 LOM

Issue No.	Issue Date	Details of Change
		indication, added bullet to describe SF alarm summary, removed bullet describing tributary level sub network connection protocol SD and SF, removed bullets describing severely errored second support. Added a bullet in the feature description, Section 2.2.2, to describe TBER functionality. Added a bullet in the feature description, Section 2.1, to describe the TOH overwrite feature on the egress line side. Added PMC-2012008 and PMC-2021098 to references section. Updated block diagrams (Figure 4, Figure 6, Figure 7, Figure 8, Figure 9 and Figure 10) to include TBER and TASR blocks within the PP subsystem. Removed timing FIFO between the DCRU and receive slice in Figure 12. Updated the description of the ALIGN_FIFO and DMUX FIFO. Updated the description of the Payload Processor Subsystem (Section 10.6) to add the TBER block and TASR blocks, removed the TSNCPP block. Removed support for STSI bypass, write passthru switch settings to bypass the STSI blocks. Updated package drawings. Removed support for metallic and diagnostic loopback of the CML links. Updated the device power sequencing requirements; ordering is no longer important (revision B of the device only). Added TBER configuration to the operations section. Updated device max power consumption estimate. Added a description of the SHPI pointer interpreter state machines. Added Table 13 to specify priority for encoding RDI / ERDI when insertion is enabled. Added a description of limited capability to detect REFCLK anomalies to the DLL operations section. Added receive link electrical monitoring section. Updated AC timing specifications. Updated applications diagrams.
5	August 2003	Document updated to reflect latest view of device.
4	March 2003	Ball diagram added Pin locations updated Mechanical info added
3	July 2002	Removed Tandem Connection functions. Added detail throughout the document.
2	December 2001	Added functional description, registers, operation, functional timing and implementation. Added 2.4G serial link, STS-1 bypass path, HOPOH, egress SVCA, 1:2 multicast, CML. Added DC/AC characteristics and FIT timing along with some other updates

Issue No.	Issue Date	Details of Change
		Added Tandem Connection features and trib SF SD generation features.
1	June 2001	Document created

Table of Contents

List of Registers

List of Figures

List of Tables

1 Definitions

Table 1 defines terms and abbreviations used in this document.

Table 1 Definitions

Term	Definition
ADM	Add-Drop Mux
CML	PMC Current-Mode Logic
ELVDS	Enhanced Low-Voltage Differential Signaling
Hair-pinning	Term used to describe a loop-back to the line side after payload processing and grooming
LVDS	Low-Voltage Differential Signaling
NSE	Narrowband Switch Element
SBS	SBI Bus Serializer
SPECTRA	SONET/SDH Payload Extractor/Aligner
TBS	Telecom Bus Serializer
TSE	Transmission Switch Element
TUPP	Tributary Unit Payload Processor
VTPA	VT/TU Payload Aligner
VTPI	VT/TU Pointer Interpreter

2 Features

2.1 General Features

- Configurable, multi-channel, payload processor for aligning SONET virtual tributaries (VTs) or SDH tributary units (TUs) in an STS-48/STM-16 or four STS-12/STM-4 byte serial data streams.
- Integrates 4 x STS-12/STM-4 VT level payload processors, 2 x ingress and egress STS-1/STM-0 granular time slot interchanges, 8 x ingress and egress STS-12/STM-4 VT level time switches and an STS-192/STM-64 VT level space switch (cross bar).
- Integrated crossbar allows for hair-pinning and OC-48 add-drop mux (ADM) functionality.
- Four TUPP 2488s may be used in parallel to support STS-192/STM-64 applications.
- Can be setup to operate in 1 of four applications:
    - Hair-pinning (from line ingress to line egress)
    - OC-48 ADM with internal crossbar
    - NxOC-48 ADM with external crossbar (internal crossbar is bypassed)
    - Payload Processing Configuration
- In hair-pinning applications from line ingress to line egress, provides an internal VT granularity Time:Space:Time switch fabric.
- In OC-48 ADM applications, the internal VT level time switches and crossbar can be used with external time switches (e.g. PM8610 SBS or PM8611 SBS-Lite devices) on the system side to implement a VT granularity Time:Space:Time switch and provide 2488.32 Mbit/s full-duplex switching.
- In NxOC-48 ADM, VT level cross connect applications, internal crossbar is bypassed. An external crossbar (e.g. PM8620 NSE device) and external time switches on the system side can be used instead in conjunction with the internal VT level time switches.
- Supports 1:2 multicast for drop and continue.
- Provides independent time-slot interchange blocks on the line side ingress and egress interfaces to allow arbitrary arrangement of time-slots at STS-1/STM-0 granularity. Time-slot interchange blocks are independently provided for working and protect links.
- On the line side, provides a 4 x 8-bit or 32-bit 77.76 MHz TelecomBus interface for direct connection to the PM5315 SPECTRA2488. This interface is referred to as the Ingress and Egress Byte-Wide TelecomBus Interface in this document.
- Robust signal integrity over high speed links using PMC-Sierra's RASIO™ CML I/O.
- Alternatively on the line side, provides redundant working and protect ingress and egress Serial RASIO™ CML links. This interface is referred to as the Line Ingress and Egress Serial RASIO™ CML Interface in this document. These links are configurable as either:
    - 4 x STS-12/STM-4 622.08 MHz SONET/SDH Framed Interfaces, or
    - 4 x STS-12/STM-4 777.6 MHz 8B/10B Encoded TelecomBus Interfaces, or

  - 1x STS-48/STM-16 2.488 GHz SONET/SDH Framed Interface. This is tied to one link and the other 3 links are unused.

- On the system side, provides redundant working and protect ingress and egress Serial RASIO™ CML links. This interface is referred to as the System Ingress and Egress Serial CML Interface in this document. These links are configurable as either:
  - 8 x STS-12/STM-4 622.08 MHz SONET/SDH Framed Interfaces, or
  - 8 x STS-12/STM-4 777.6 MHz 8B/10B Encoded TelecomBus Interfaces.
- Independently configurable line and system interfaces. Line ingress and line egress interfaces must be configured with the same type of interface as each other. Similarly, system ingress and system egress interfaces must be configured with the same type of interface as each other.
- Provides capacity to carry an STS-12/STM-4 stream in each Serial RASIO™ CML link. Four links can be aggregated to form an STS-48/STM-16 stream. Alternatively, on the line side, one of the Serial RASIO™ CML links can carry an STS-48/STM-16 stream and the other three links are unused.
- Provides capacity to carry an STS-12/STM-4 stream in each 8-bit bus of the Byte-Wide TelecomBus stream. Four 8-bit buses can be aggregated to carry an STS-48/STM-16 stream.
- Provides optional PRBS (unframed PRBS or framed PRBS, STS-48c/VC-4-16c SPE for 2.488G links and STS-12c/VC-4-4c for 622M links) generation for each Line Egress and System Ingress Serial RASIO™ CML stream for off-line link verification. Provides PRBS monitoring for each Line Ingress and System Egress Serial RASIO™ CML stream for off-line link verification.
- Detects 8B/10B line code violations (LCVs) on the Serial RASIO™ CML 777.6 MHz TelecomBus interfaces and accumulates them in internal registers.
- Provides an inband communication channel in the system side RASIO™ CML links to allow for centralized control and configuration when operating with a centralized fabric (e.g. NSE).
- Performs H1/H2 processing and generation to compensate for offsets in line ingress and line egress J0(C1) frame alignment. Allows for separate ingress and egress J0(C1) frame alignment via external frame alignment signals and programmable offsets.
- On the line side 777.6 MHz links, provides encoding of TelecomBus control signals at the multiplex section termination (MST) point and high-order path termination (HPT) point.
- On the system side 777.6 MHz links, provides encoding of TelecomBus control signals at the multiplex section termination (MST) point and high-order path termination (HPT) point.

Note: Refer to Table 6 for the difference between MST and HPT.

- In ADM applications, provides maximum steady-state latency of 38.73 µs from line ingress to system ingress for VT1.5 and maximum steady state latency of 22.56 µs from system egress to line egress for VT1.5. In pure payload processing applications provides maximum steady state latency of 19.69 µs from line ingress to line egress for VT1.5. In hair-pinning applications provides maximum steady state latency of 56.9 µs from line ingress to line egress for VT1.5.
- Supports contiguously concatenated payloads (STS-3c, STS-12c/AU-4-4c, STS-48c/AU-4-16c).
- Provides the ability to overwrite a line side transport overhead byte prior to egress.
- On egress path, provides optional SDH payload conversions as follows:
  - **3x** AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3
  - **3x** AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2

    Note: Mixing AU3/VC3/C3 and AU3/VC3/TUG2 payloads in an AU4 during AU3 to AU4 conversion is not supported.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan test purposes.
- Implemented in 1.2 V core and 2.5 V I/O 0.13 µm CMOS technology. Inputs are 3.3 V tolerant. The MPIF data bus, Egress Parallel TelecomBus, and REFCLK input are programmable to 2.5 V or 3.3 V. REFCLK and the Egress Parallel TelecomBus voltage are programmed from the same source.
- 580-ball CSBGA+ package.

2.2 Payload Processing Features

The payload-processing blocks are provided in the ingress path of TUPP 2488 and perform payload processing on traffic from the line ingress path before it is output on either the system ingress (via the switch matrix) or line egress paths.

2.2.1 General Payload-Processing Features

The following features are available to both VT/TU mapped traffic and also bypass traffic. Bypass traffic consists of non VT-TU mapped payloads i.e. STS-1, AU3/VC3/C3, AU4/VC4/C4, and contiguous concatenated payloads STS-3c, STS-12c/AU4-4c, STS-48c/AU4-16c.

- Aligns the synchronous payloads of a SONET/SDH STS-48/STM-16 or four STS-12/STM-4 byte serial streams to a new transport frame reference (J0).
- Inserts valid high order pointer bytes (H1, H2), framing bytes (A1, A2).
- Allows the following SDH payload conversions:
  - **3x** AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3
  - **3x** AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2

- AU4/VC4/TUG3/TU3/VC3/C3 to **3x** AU3/VC3/C3
- AU4/VC4/TUG3/TUG2 to **3x** AU3/VC3/TUG2

Note: Mixing AU3/VC3/C3 and AU3/VC3/TUG2 payloads in an AU4 during AU3 to AU4 or AU4 to AU3 conversion is not supported.

2.2.2 Tributary Traffic Payload-Processing Features

The following additional payload processing features are available for VT/TU mapped payloads:

- Translates pointer justifications in high order payloads (STS-1/STM-0, AU4, AU3) to pointer justifications in low order payloads (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, or TU11), resulting in all VT/TUs being located in fixed columns of the transport frame.
- Configurable to enforce a minimum three multiframe spacing between consecutive inserted outgoing low order tributary pointer justifications.
- Provides software configurable offset between the payload frame boundaries (J1) and the H3 byte of the transport overhead (H1, H2 pointer = 0 or 522).
- Supports any legal mix of VT1.5, VT2, VT3, VT6, TU11, TU12, TU2, or TU3 tributaries. Each VT group or TUG2 can be configured to carry one of four tributary types. TUG2s can be multiplexed into VC3s or TUG3s. Each TUG3 can also be configured to carry a single TU3.
- Supports 16-byte or 64-byte format tributary path trace messages (tributary trail trace identifiers).
- Supports H4 framing to determine tributary multiframe boundaries. Inserts internally generated H4 bytes with tributary multiframe indicator.
- Extracts and serializes the entire tributary path overhead of each tributary (VT1.5, VT2, VT3, VT6, TU11, TU12, TU2, or TU3) into serial streams.
- Extracts tributary size (SS) bits of each tributary into internal registers.
- Detects tributary loss of pointer (LOP) and re-acquisition for each tributary and optionally generates interrupts.
- Detects tributary path alarm indication signal (AIS) and return to normal state for each tributary and optionally generates interrupts.
- Optionally translates high order path AIS to tributary AIS.
- Detects tributary elastic store underflow and overflow errors and optionally generates interrupts.
- Extracts tributary path trace message (trail trace identifier) of each tributary into internal buffers.
- Provides individual tributary path trace message buffer that holds the expected message and detects tributary path trace mismatch (trail trace identifier mismatch) alarms (TIM) and return to matched state for each tributary and optionally generates interrupts.

- Detects tributary path trace unstable (trail trace identifier unstable) alarms (TIU) and return to stable state for each tributary and optionally generates interrupts.
- Extracts tributary path signal label for each tributary into internal registers and detects change of tributary path signal label events (COPSL) of each tributary and optionally generates interrupts.
- Provides individual tributary path signal label register that hold the expected label and detects tributary path signal label mismatch alarms (PSLM) and return to matched state for each tributary and optionally generates interrupts.
- Detects tributary path signal label unstable alarms (PSLU) and return to stable state for each tributary and optionally generates interrupts.
- Detects tributary unequipped defect (UNEQ) and tributary path defect indication (PDI-V).
- Detects assertion and removal of tributary extended remote defect indications (RDI) for each tributary and optionally generates interrupts.
- Calculates and compares the tributary path BIP-2 error detection code for each tributary and is configurable to accumulate the BIP-2 errors, on a block or bit basis, in internal registers.
- Calculates and compares the TU3 path BIP-8 error detection code for each TU3 stream and accumulates the BIP-8 errors, on block or bit basis, in internal registers.
- Accumulates TU11, TU12, TU2, and TU3 tributary remote error indications (REI) on a bit or a block basis, in internal registers.
- Allows insertion of all-zeros or all-ones tributary idle code with unequipped indication (UNEQ) and valid pointer into any tributary under software control. Identifies tributaries on the Egress Byte-Wide TelecomBus that are in an idle state by an output signal.
- Identifies tributaries on the Egress Byte-Wide TelecomBus that are in AIS state by an output signal. Allows software to force the AIS insertion on a per tributary basis.
- Supports inband error reporting by updating the REI, RDI, and auxiliary RDI bits in the V5 byte (G1 in TU3) with the status of the ingress stream.
- Detects ingress positive and negative pointer justifications and provides positive and negative justification counts on a per tributary basis.
- Reports per STS-1/STM-0 LOM (Loss of Multiframe) interrupts.
- Provides an excessive error defect (DEXC) and signal degrade (SD) alarm status for each tributary path.
- Provides per-TU (VT) user programmable BER thresholds for each DEXC / SD test that range from 10^{-3} to 10^{-12} .
- Processes Low Order (LO) tributary defects of a SONET/SDH data stream in order to generate Signal Failure (SF) conditions. LO includes TU3, VT1.5/TU11, VT2/TU12, VT3 or VT6/TU2 payloads. Signal fail detection is configurable on a per tributary basis to include or exclude LOP, AIS, an aggregated form of AIS, UNEQ, TIM, TIU, PSLM, PSLU, LOM, SD, and DEXC. Optionally generates an interrupt on a change in signal fail status.

2.3 High Order Path Overhead Termination Features

- Supports path termination for any legal mix of STS-1/AU-3, STS-3c/AU-4, STS-12c/AU-4-4c, and STS-48c/AU-4-16c.
- Processes the path overhead from the line ingress stream. Inserts the path overhead into the line egress stream.
- Detects received path BIP-8 (B3) byte and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Generates transmit path BIP-8 (B3) byte. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ), and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.
- Extracts a 64-byte or 16-byte message from the received path trace (J1) byte, and stores into an internal register bank. Detects an unstable message or mismatched message compared to an expected message. Provides access to the captured, accepted and expected message via the microprocessor port. Inserts a 64-byte or 16-byte path trace (J1) message using an internal register bank for the transmit stream.
- Processes bits 1-4 of the path status (G1) byte to count received path remote error indications (REI's) for performance monitoring. Optionally insert the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block basis independent of the accumulation of BIP-8 errors.
- Supports insertion of bit 5 of the path status (G1) byte for automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI);
- Supports insertion of path AIS following detection of various received alarms (LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI).
- All high order path overhead bytes in raw form are exported over the received path overhead bus. All path overhead bytes may be inserted from the transmit path overhead bus. VC4 path overhead bytes are exported and inserted when processing AU4/VC4/TUG3/TU3.

3 Applications

- SONET/SDH Add-Drop Multiplexer (ADM)
- SONET/SDH Digital Cross-Connect (DCC)
- Multiservice Provisioning Platforms (MSPP)
- Multiservice ADM (MS-ADM)
- Multiservice Switch
- Optical Access Mux
- Terminal Multiplexers

4 References

1. American National Standard for Telecommunications – Synchronous Optical Network (SONET) – Basic Description Including Multiplex Structures, Rates, and Formats, ANSI T1.105-1995.

2. Committee T1 Contribution, "Draft of T1.105 - SONET Rates and Formats", T1X1.5/94-033R2-1994.

3. Committee T1 Contribution, "Payload Defect Indication (PDI): triggers, Switch Priorities, Timing and Proposed Text", T1X1.5/94-135R1, 1994.

4. Committee T1 Contribution, "Proposed ITU-T Contribution on Enhanced Path RDI for SDH", T1X1.5/94-117, 1994.

5. ITU, Recommendation G.782 - "Types and general characteristics of synchronous digital hierarchy (SDH) equipment", January 1994.

6. ITU, Recommendation G.783 - "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks", April 1997.

7. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-TSY-000253, Issue 2, December 1991.

8. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, September 2000.

9. Bell Communications Research - SONET Add-Drop Multiplex Equipment (SONET ADM) Generic Criteria, GR-496, Issue 1, December 1998.

10. Bell Communications Research - SONET Dual-Fed Unidirectional Path Switched Ring (UPSR) Equipment Generic Criteria, GR-1400-CORE, Issue 2, January 1999.

11. European Telecommunications Standards Institute, Transmission and Multiplexing (TM); Generic Functional Requirements for SDH Transmission Equipment, Part 1, Generic Process and Performance, ETS 300 417-1-1, January 1996.

12. ITU, Recommendation G.707 – “Network Node Interface For The Synchronous Digital Hierarchy”, 2000.

13. Electronic Industries Association. Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device): EIA/JESD51. December 1995.

14. Electronic Industries Alliance 1999. Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8. October 1999.

15. Telcordia Technologies. Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE. Issue 1. October 1995.

16. SEMI (Semiconductor Equipment and Materials International). SEMI G30-88 Test Method for Junction-to-Case *Thermal Resistance Measurements of Ceramic Packages*. 1988.

17. PMC-2020188, TUPP 2488 Register Description, Issue 6

18. Digital Power Supply Bypass Guidelines, Issue 2, PMC-2012008.

19. Optimizing Pre-emphasis and Receive Equalization for Backplanes, Issue 1, PMC-2021098.

20. TUPP 2488 Hardware Design Guidelines, Issue 4, PMC-2020238

21. TUPP 2488 Configuration Guide, Issue 2, PMC-2020239

5 Application Examples

Figure 1 shows how the TUPP™ 2488 can be used in a one-armed application. This application is also referred to as hair-pinning.

Figure 1 OC-48 One Armed VT Grooming Application

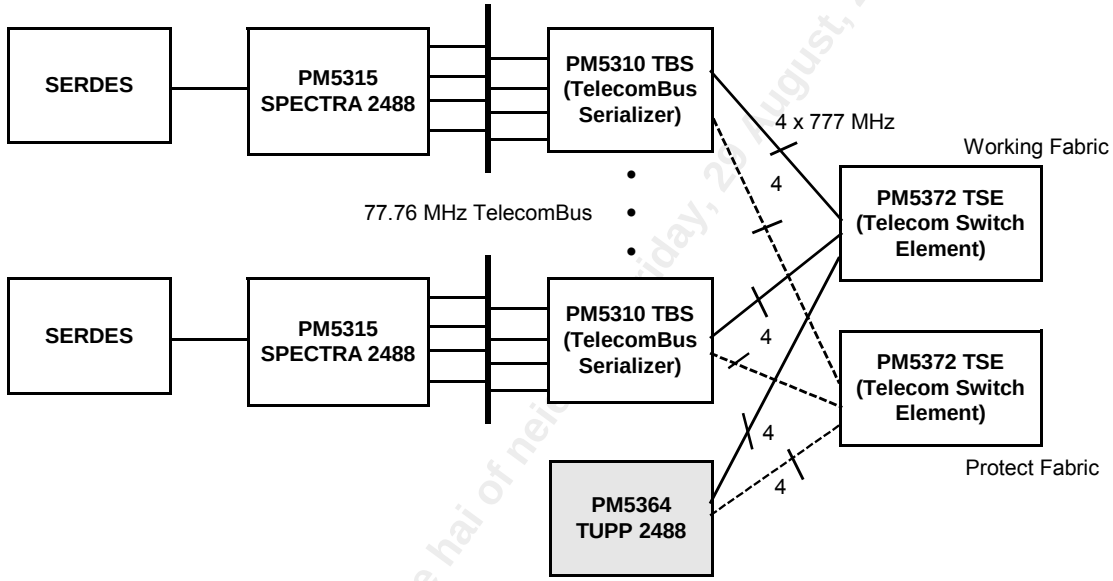


Figure 2 shows how the TUPP 2488 can be used in an OC-48 Add-Drop Multiplexer application.

In this application, the internal crossbar in the TUPP 2488 device is used. The TUPP 2488 provides the space stage and one of the time stages of the Time:Space:Time switch fabric. The external SBS-Lite™ devices provide the remaining time stage to complete the Time:Space:Time switch fabric.

Figure 2 OC-48 Add-Drop Multiplexer Application

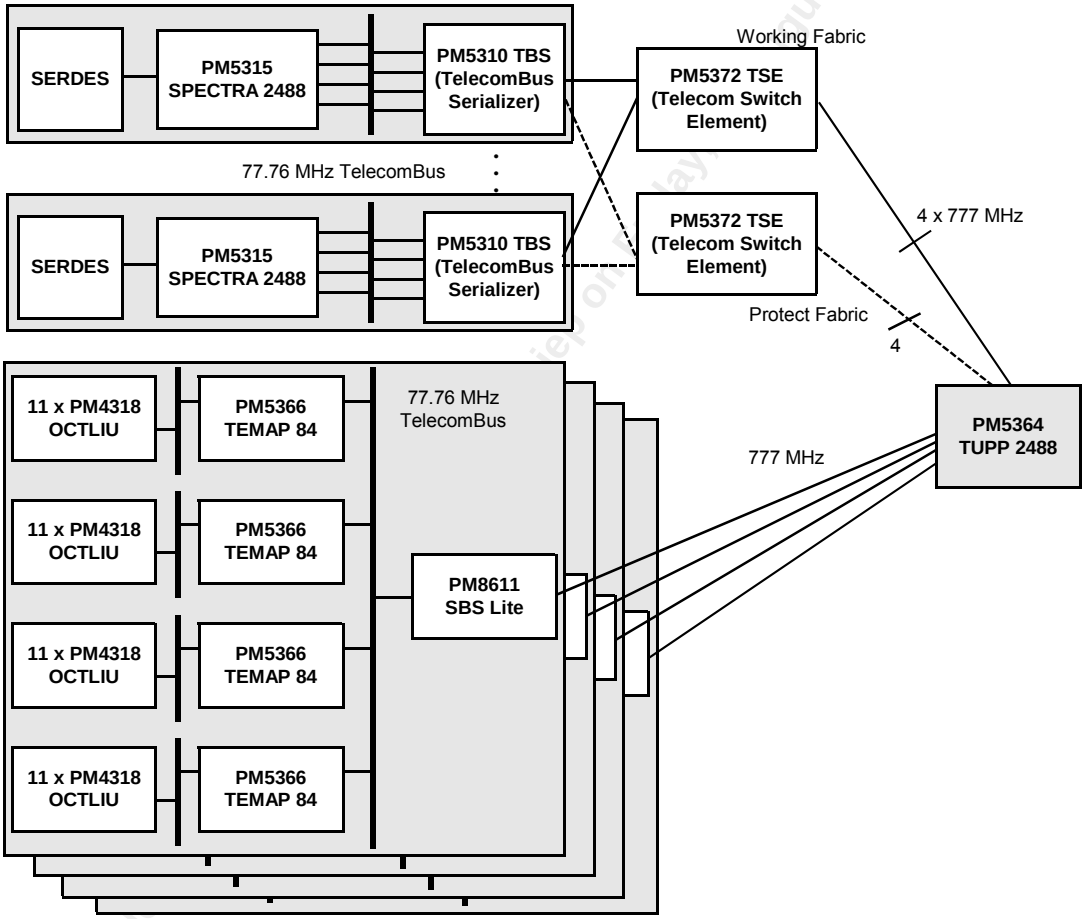
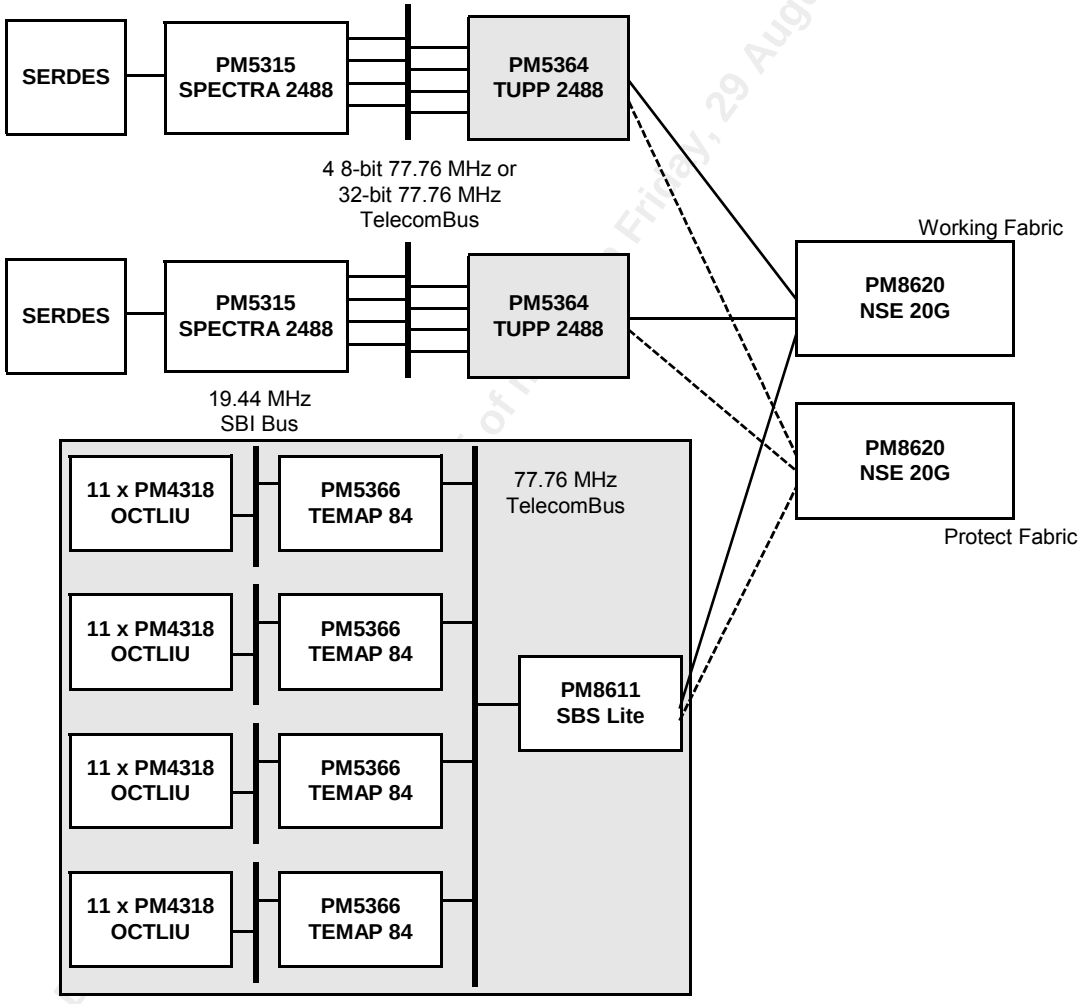


Figure 3 shows how the TUPP 2488 can be used with the SPECTRA™ 2488 in an N x OC-48 ADM, VT level cross-connect application.

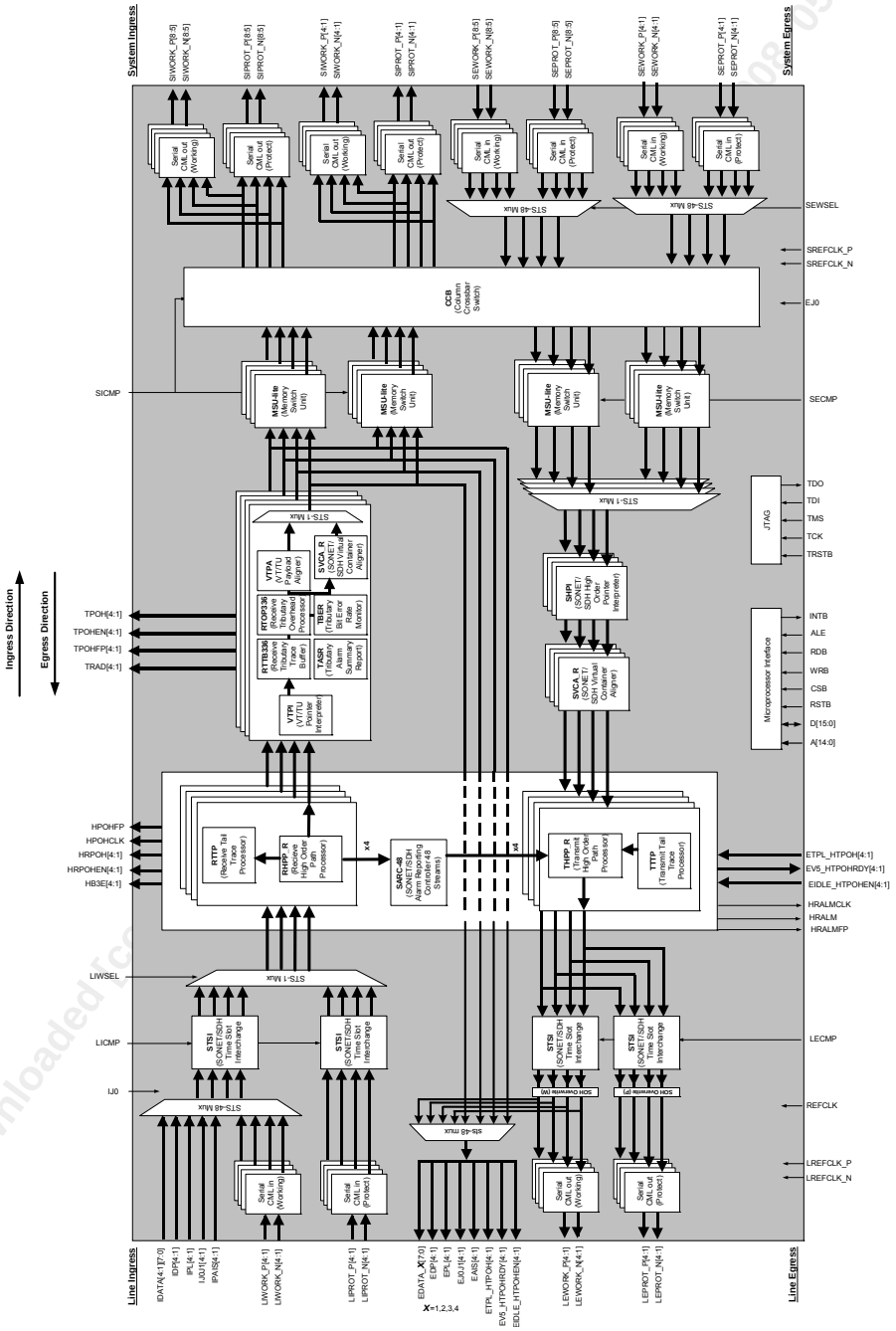
In this application, the internal crossbar in TUPP 2488 is bypassed and the external NSE™ 20G devices provide the crossbar function. The TUPP 2488 provides one of the time stages of the Time:Space:Time switch fabric. The external NSE provides the space stage, and the external SBS devices provide the remaining time stage to complete the Time:Space:Time switch fabric.

Figure 3 NxOC-48 ADM, VT Level Cross Connect Application



6 Block Diagram

Figure 4 Block Diagram



Note

See notes in pin description for ETPL_HTPOH, EIDLE_HTPOHEN, and EV5_HTPOHRDY.

Figure 5 Data Flow

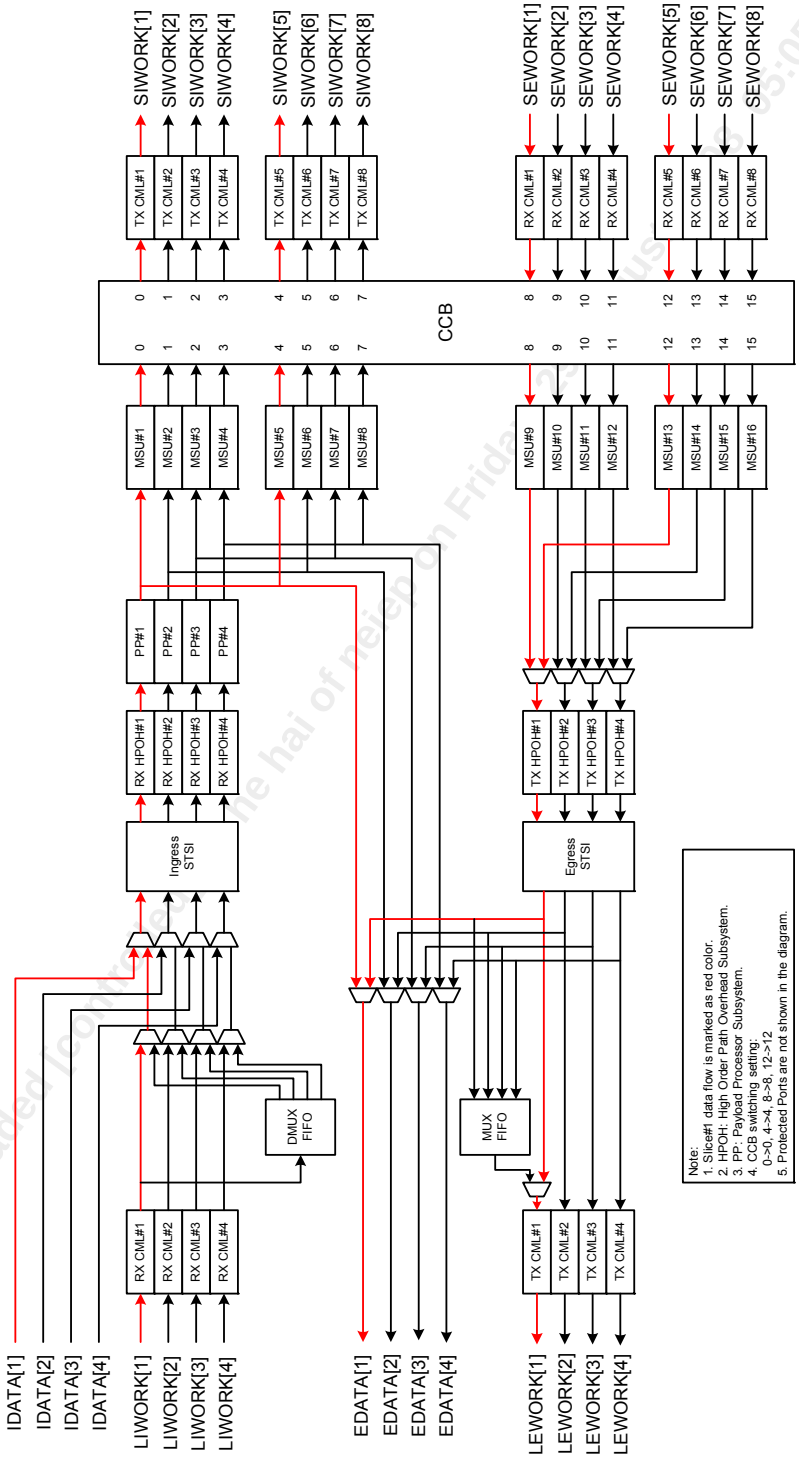
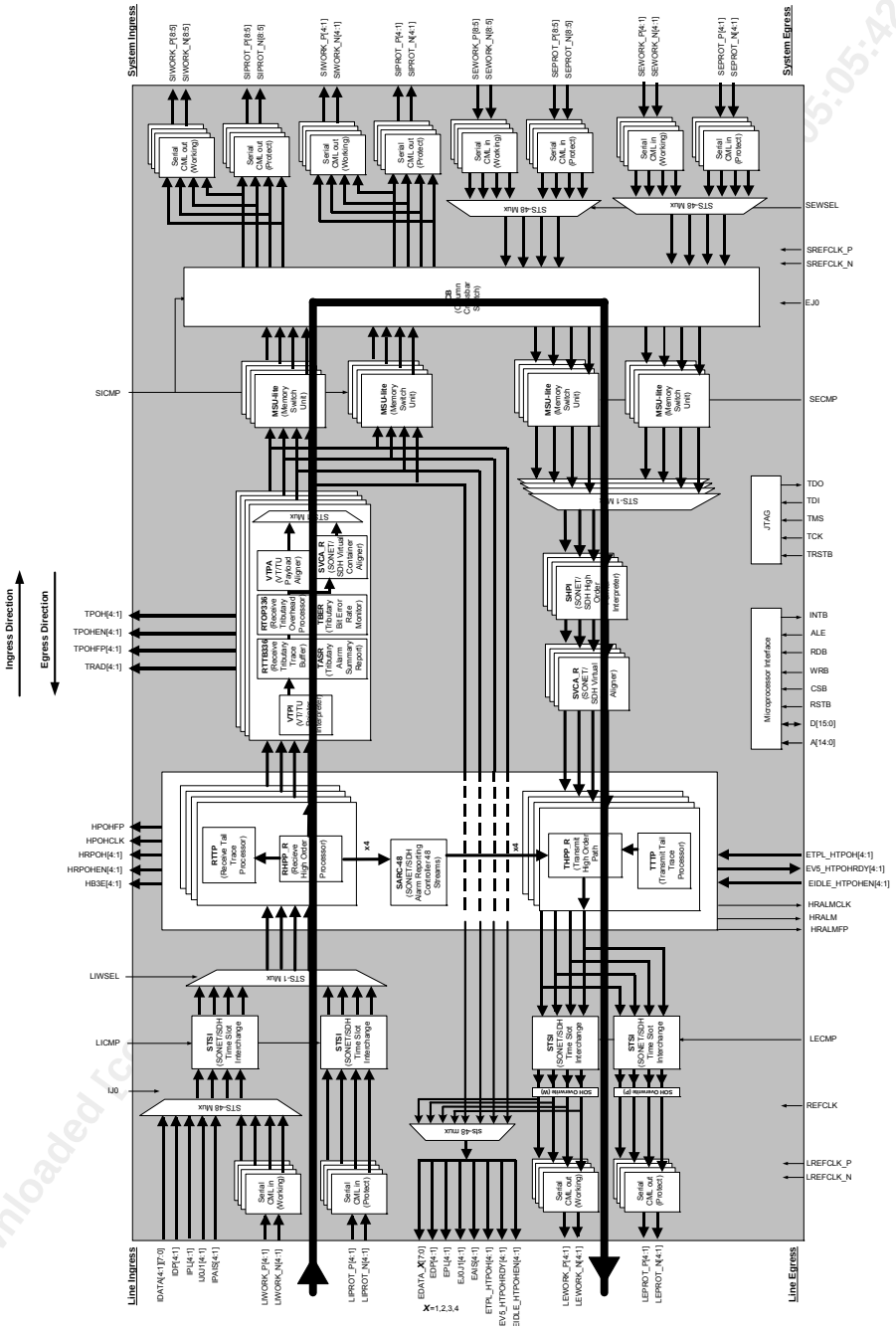


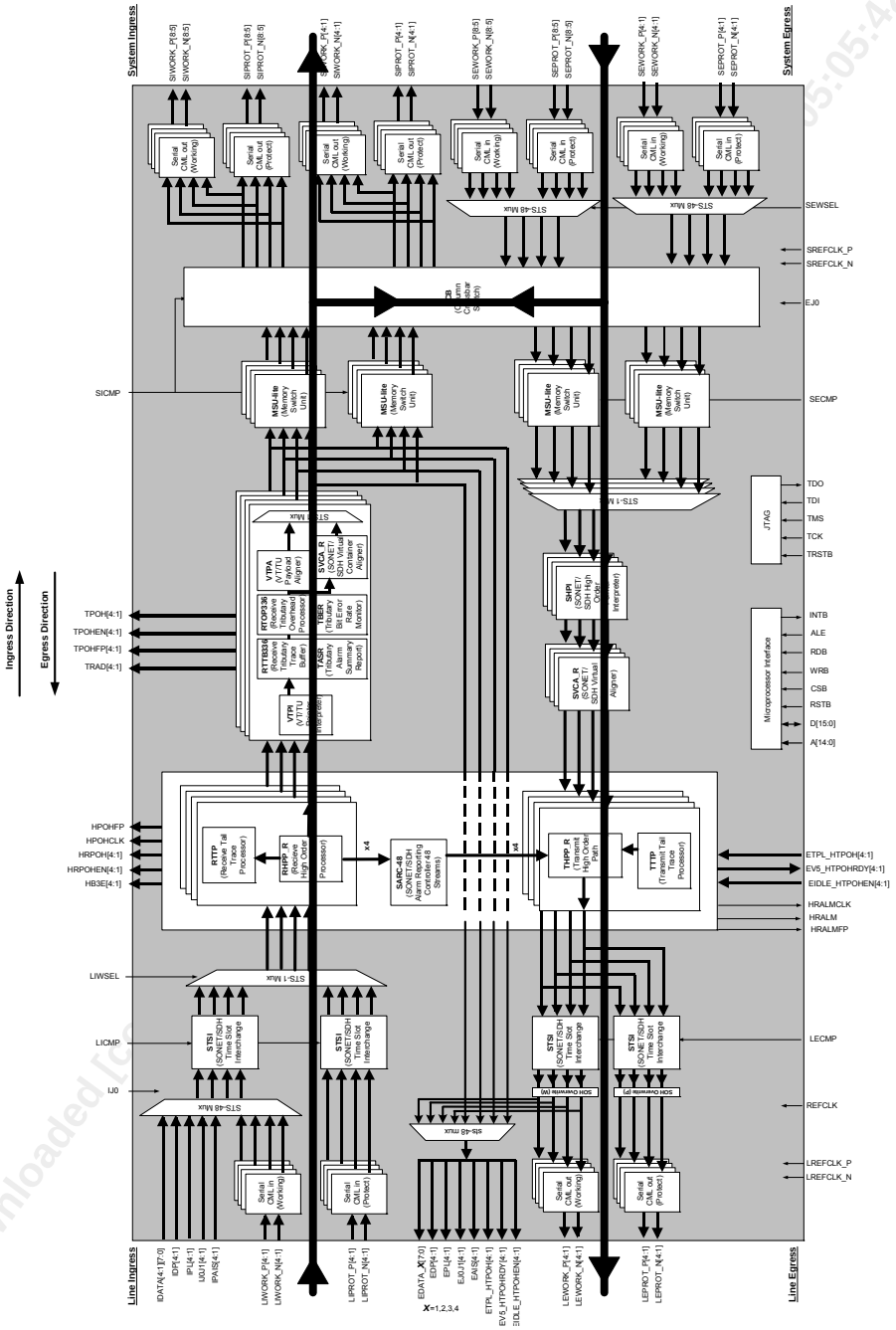
Figure 6 Block Diagram - Hair Pinning Application



Notes

1. In this case, ETPL_HTPOH and EIDLE_HTPOHEN are inputs. See pin description for details.
2. Internal Time:Space:Time switch fabric provided.

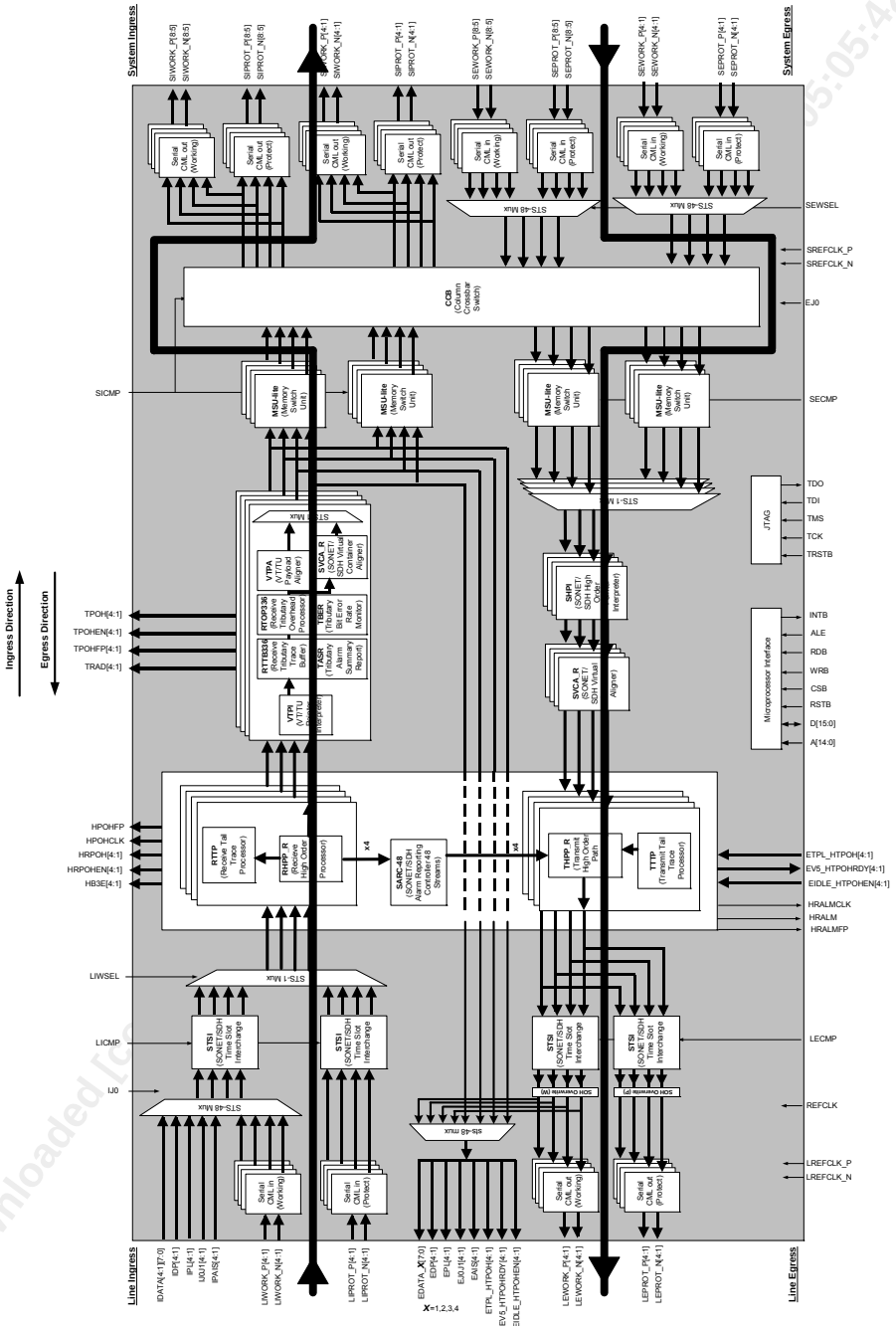
Figure 7 Block Diagram - OC-48 ADM Application Using Internal Crossbar



Notes

1. In this case, ETPL_HTPOH and EIDLE_HTPOHEN are inputs. See pin description for details.
2. External time stage switches are required on the system side.

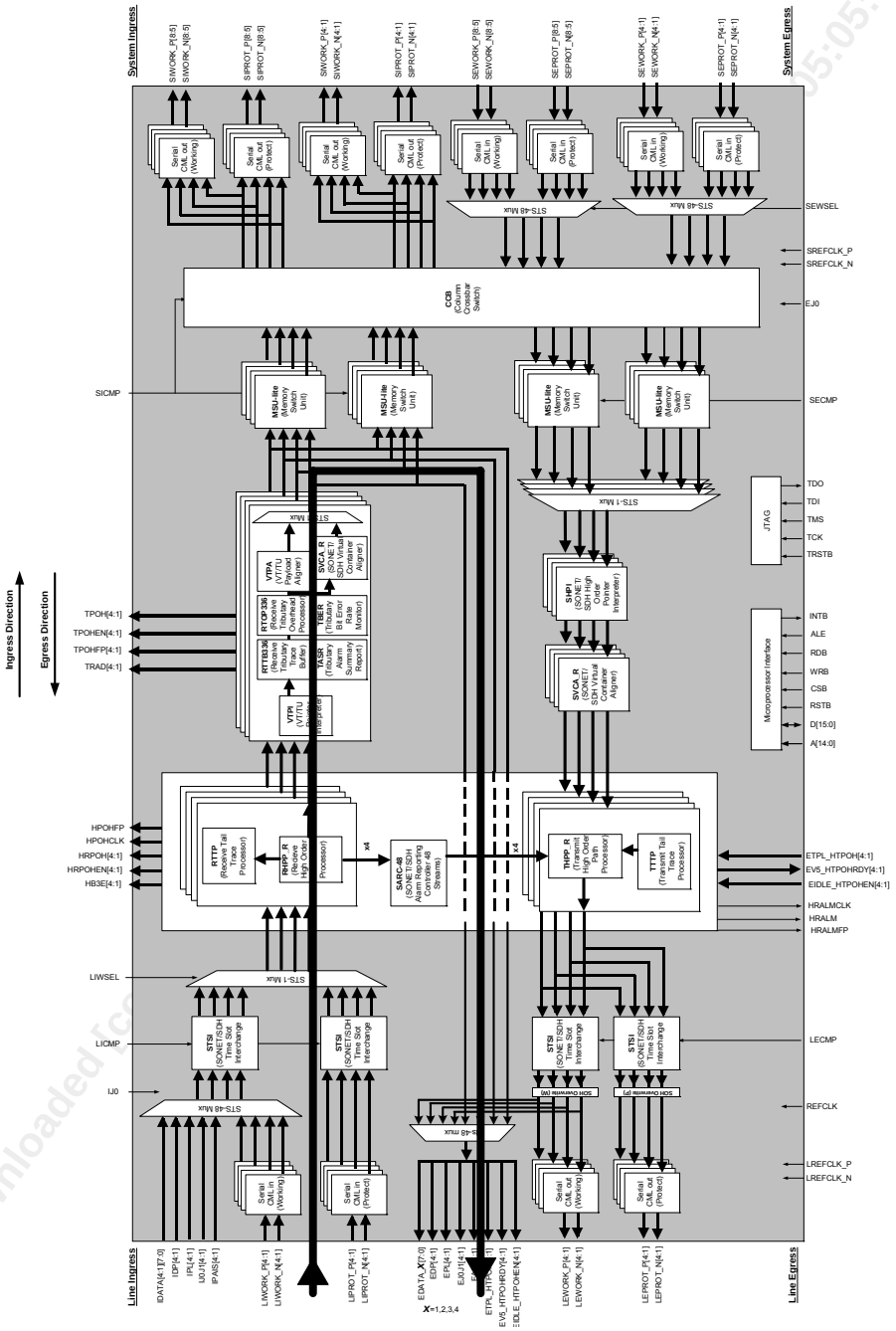
Figure 8 Block Diagram - NxOC-48 ADM Using External Crossbar



Notes

1. In this case, ETPL_HTPOH and EIDLE_HTPOHEN are inputs. See pin description for details.
2. Internal crossbar is bypassed. External time stage switches and an external crossbar are required on the system side.

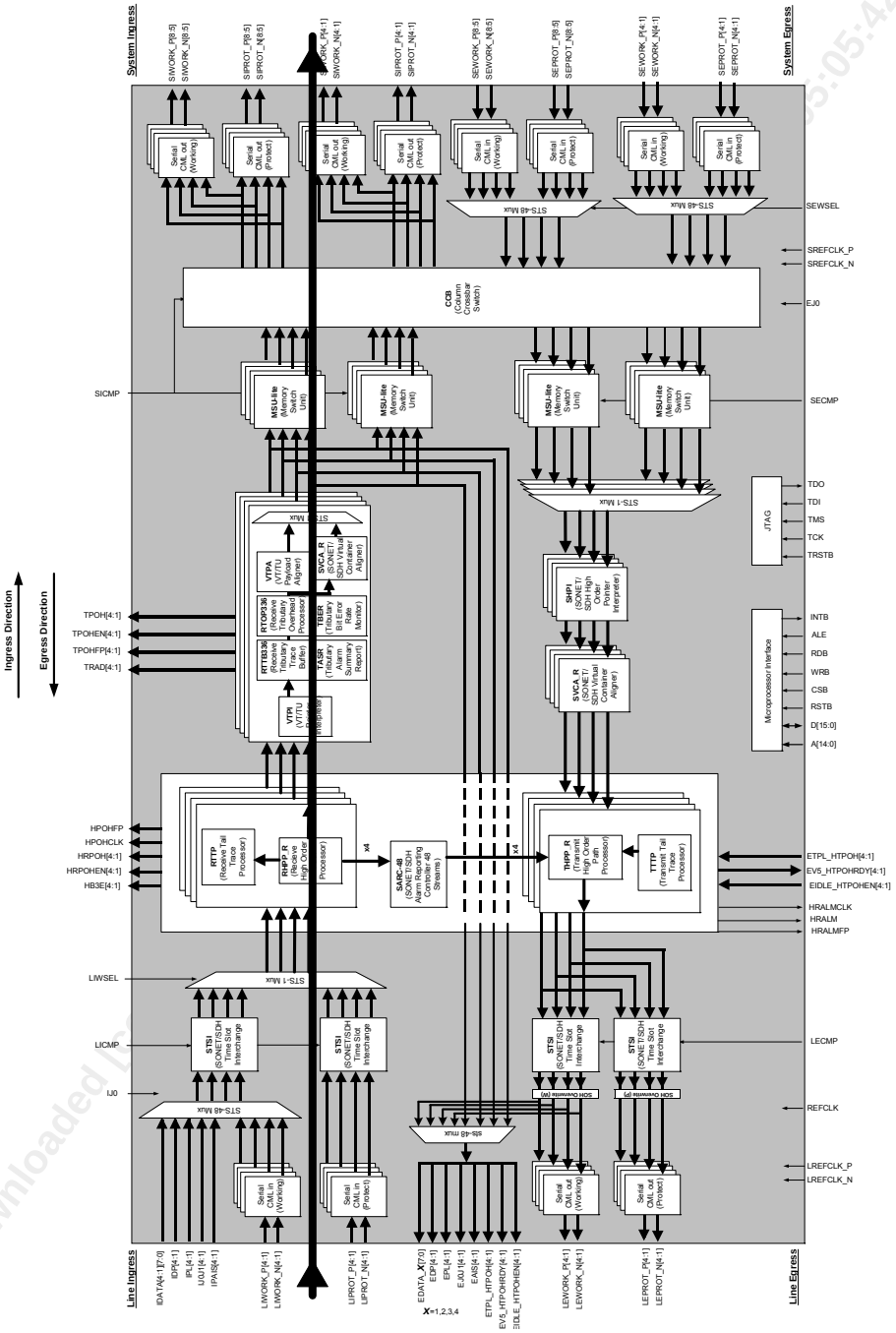
Figure 9 Block Diagram - Payload Processing Configuration using Parallel I/Os (PP Loopback)



Note

- In this case, ETPL_HTPOH and EIDLE_HTPOHEN are outputs. See pin description for details.

Figure 10 Payload Processing Configuration Using Serial I/Os



Further loopbacks to aid device debug are explained in the Operation Section, including:

- Loopback from Line Ingress RASIO™ CML output to Line Egress RASIO™ CML and Line Egress Parallel Bus.
- Loopback from System Egress RASIO™ CML output to System Ingress RASIO™ CML input.
- Loopback from Ingress STSI output to Egress STSI input.
- Loopback from Ingress High Order Path Overhead output to Egress High Order Path Overhead input.

7 Description

The PM5364 TUPP 2488 SONET/SDH Tributary Unit Payload Processor for 2488.32 Mbit/s Interfaces is a monolithic integrated circuit that implements a configurable, multi-channel, payload processor that aligns and monitors performance of SONET virtual tributaries (VTs) or SDH tributary units (TUs).

The TUPP 2488 integrates 4 x STS-12/STM-4 VT level payload processors in the ingress path. On the line side, it provides 2 x ingress and egress STS-1/STM-0 granular time slot interchanges. On the system side it provides 8 x ingress and egress STS-12 VT-level time switches and an STS-192/STM-64 VT-level space switch (cross bar). The internal crossbar allows for hair-pinning and OC-48 ADM. The TUPP 2488 supports 1:2 multicast for drop and continue.

The TUPP 2488 architecture should be viewed as two separate switch fabrics – system side (VT/TU level) and line side (STS-1). The line side and system side fabrics have independent switching control. The TUPP 2488 provides a full or partial fabric depending on the application it is used in.

In hair-pinning applications from line ingress to line egress, the system side of TUPP 2488 provides an internal VT granularity Time:Space:Time switch fabric. No separate time or space stage switches are required on the system side.

In OC-48 ADM applications, the internal VT level time switches and crossbar can be used with external time switches (e.g. SBS devices) on the system side to implement a VT granularity Time:Space:Time switch and provide 2488.32 Mbit/s full-duplex switching.

In NxOC-48 ADM, VT level cross connect applications, the internal crossbar is bypassed. An external crossbar (e.g. NSE device) and external time switches on the system side can be used instead in conjunction with the internal VT level time switches.

The TUPP 2488 provides independent timeslot interchange blocks on the line side ingress and egress interfaces to allow arbitrary arrangement of timeslots at STS1/STM-0 granularity. Time-slot interchange blocks are independently provided for working and protect links. These blocks can provide the time stage of a line side Time:Space:Time switch fabric using TBS and TSE devices.

On the line side, the TUPP 2488 provides a 4 x 8-bit or 32-bit 77.76 MHz Telecom Bus interface for direct connection to the SPECTRA 2488. Alternatively provides 4 redundant Serial RASIO™ CML STS-12/STM-4 622.08 MHz SONET/SDH framed interfaces or 777.6 MHz 8B/10B encoded TelecomBus interfaces or one redundant Serial RASIO™ CML STS-48/STM-16 2.488 GHz SONET/SDH framed interface.

On the system side, the TUPP 2488 provides eight redundant Serial RASIO™ CML 622.08 MHz SONET/SDH framed interfaces or 777.6 MHz 8B/10B encoded TelecomBus interfaces.

The line and system interfaces are configurable independently. Line ingress and line egress interfaces must be configured with the same type of interface as each other. Similarly, system ingress and system egress interfaces must be configured with the same type of interface as each other.

When configured for SONET compatible operation, the TUPP 2488 processes all tributaries in the forty-eight STS-1 synchronous payload envelopes of an STS-48 or four STS-12 byte serial streams. Similarly, when configured for SDH compatible operation, the TUPP 2488 processes all tributaries in the sixteen AU4 or forty-eight AU3 administrative units of an STM-16 or four STM-4 byte serial streams.

The TUPP 2488 translates pointer justifications in high order payloads (STS-1/STM-0, AU4, AU3) to pointer justifications in low order payloads (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, or TU11), resulting in all VT/TUs being located in fixed columns of the transport frame.

The TUPP 2488 is configurable to process any legal mix of tributaries. Each VT group can be configured to carry any one of the four tributary types (VT1.5, VT2, VT3, or VT6) and each TUG2 can be configured to carry any one of three tributary types (TU11, TU12, or TU2). TUG2s can be multiplexed into a VC3 or a TUG3. Alternatively, each TUG3 can be configured to carry a TU3.

The TUPP 2488 monitors VT/TU path bit error rates (BIP-2). Two independent monitors are provided per tributary, one for an excessive error defect (DEXC) alarm and one for a signal degrade (SD) alarm. Programmable thresholds allow the monitors to declare an alarm for bit error rates from 10^{-3} to 10^{-12}. The DEXC and SD alarms are optionally aggregated with other alarms to declare a signal fail (SF) condition.

The TUPP 2488 provides useful maintenance functions. They include, for each tributary, detection of loss of pointer, detection of AIS alarm, detection of tributary path signal label mismatch and unstable alarms, detection of tributary path trace mismatch and unstable alarms. Optionally, interrupts can be generated due to the assertion and removal of any of the above alarm conditions. The TUPP 2488 counts received tributary path BIP-2 (BIP-8 for TU3) errors on a block or bit basis and counts REI indications. The TUPP 2488 also allows insertion of tributary path AIS as a consequence of any of the above alarm conditions. In addition, the TUPP 2488 may insert tributary idle (unequipped) into any tributary. Ingress tributary path trace messages and path signal labels are stored in a set of microprocessor accessible registers. The TUPP 2488 can also insert inverted new data flag fields that can be used to diagnose downstream pointer processing elements.

The TUPP 2488 provides a bypass path around the payload processor blocks for non VT-TU mapped payloads i.e. STS-1, AU3/VC3/C3, AU4/VC4/C4 and contiguous concatenated payloads STS-3c, STS-12c/AU4-4c, STS-48c/AU4-16c.

The ingress path of TUPP 2488 allows the following SDH payload conversions:

- AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3
- AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2

- AU4/VC4/TUG3/TU3/VC3/C3 to AU3/VC3/C3
- AU4/VC4/TUG3/TUG2 to AU3/VC3/TUG2

Note: Mixing AU3/VC3/C3 and AU3/VC3/TUG2 payloads in an AU4 during AU3 to AU4 or AU4 to AU3 conversion is not supported.

The ingress path also extracts the tributary path overhead bytes and alarm information into serial streams.

The egress path of TUPP 2488 provides optional SDH payload conversions as follows:

- AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3.
- AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2

Note: Mixing AU3/VC3/C3 and AU3/VC3/TUG2 payloads in an AU4 during AU3 to AU4 conversion is not supported.

The TUPP 2488 terminates the path overhead of any legal mix of STS-1/3c/12c/48c (VC-3/4/4-4c/4-16c) payloads in a SONET/SDH STS-48/STM-16 stream. In the receive direction, the TUPP 2488 detects path alarm conditions, detects and accumulates path BIPs (B3). It extracts Remote Error Indications (REIs) from path status (G1), and monitors and accumulates path Remote Error Indications (REIs) for performance monitoring. It accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result. It extracts the received path payload label (C2). All path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead along with alarm information, if desired. In the transmit direction, the TUPP 2488 creates and inserts the path BIPs (B3), optionally inserts a 16 or 64 byte path trace (J1) message, optionally inserts the path status byte (G1) and the path payload label (C2) byte into the transmit stream. In addition to its basic processing of the transmit SONET/SDH path overhead, the TUPP 2488 provides convenient access to all path overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of path overhead if desired. The TUPP 2488 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, pointer errors and BIP errors, which are useful for system diagnostics and tester applications.

The TUPP 2488 does not support STS-1 (VC3/VC4) path overhead transparency.

8 Pin Diagram

The TUPP 2488 is packaged in a 580-ball CSBGA+ package having a body size of 35 mm x 35 mm and a ball pitch of 1 mm. See Section 9 for the pin descriptions.

Figure 11 Pin Diagram (Bottom View)

Top Left

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19
A	VSS	VSS	VDDI	VSS	EDATA_4[4]	EDATA_4[6]	VSS	LREFCLK_P	]	VSS		LEPROT_N[4]	LEPROT_N[3]	LEPROT_N[2]	LEPROT_N[1]	LIPROT_N[1]
B	VSS	VSS	VDDI	VDDOPROG_E	EDATA_4[3]	EDATA_4[5]	EDATA_4[7]	LREFCLK_N		LQAVD		LEPROT_P[4]	LEPROT_P[3]	LEPROT_P[2]	LEPROT_P[1]	LIPROT_P[1]
C	VDDI	VDDI	VDDI	VSS	VDDOPROG_E		LAVDH	LC_AVDL[2]			LAVDL	VSS	LAVDL	VSS	LAVDL	VSS
D	VSS	VDDOPROG_E	VSS	VDDI	VSS	VDDOPROG_E		LAVDL			LC_AVDH[0]	LEWORK_N [4]	LEWORK_N [3]	LEWORK_N [2]	LEWORK_N[1]	LIWORK_N[1]
E	VSS	EDATA_4[2]	VDDOPROG_E	VSS	VDDI	VSS	VDDO	LC_AVDH[1]	LC_AVDL[1]	LAVDH	LC_AVDL[0]	LEWORK_P [4]	LEWORK_P [3]	LEWORK_P [2]	LEWORK_P[1]	LIWORK_P[1]
F	EDP[4]	EDATA_4[0]	EDATA_4[1]	VDDOPROG_E	VSS											
G	EAIS[4]	EJ0J1[4]	EPL[4]	VSS	VSS											
H	VSS	ETPL_HTPOH[4]	VDDOPROG_E	VSS	VSS											
J	EDATA_3[7]	EIDLE_HTPOHEN[4]	EV5_HTPOHRDY [4]	VSS	VSS											
K	EDATA_3[4]	EDATA_3[5]	EDATA_3[6]	VSS	VDDOPROG_E											
L	EDATA_3[1]	EDATA_3[2]	EDATA_3[3]	VSS	VDDI											
M	VSS	EDATA_3[0]	VDDOPROG_E	VSS	VSS											
N	EJ0J1[3]	EPL[3]	EDP[3]	VSS	VSS											
P	EV5_HTPOHRDY [3]	ETPL_HTPOH[3]	EAIS[3]	VSS	VDDOPROG_E											
R	VSS	EDATA_2[7]	EIDLE_HTPOHEN[3]	VSS	VDDO											
T	EDATA_2[6]	REFCLK	VDDOPROG_E	VSS	VSS											
U	VSS	EDATA_2[3]	EDATA_2[5]	EDATA_2[4]	VDDI											

Top Right

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
LIPROT_N[2]	LIPROT_N[3]	LIPROT_N[4]	IPAIS[1]	VSS	IDATA_1[4]	IPAIS[2]	IDATA_2 [1]	VSS	IDATA_2 [5]	IPL[3]	IDATA_3 [0]	VSS	IJ0J1[4]	IDP[4]	VDDI	VSS	VSS	A
LIPROT_P[2]	LIPROT_P[3]	LIPROT_P[4]	IJ0	IDP[1]	IDATA_1[3]	IDATA_1 [5]	IJ0J1[2]	IDATA_2 [2]	IDATA_2 [6]	IDP[3]	IDATA_3 [3]	IDATA_3 [5]	IPL[4]	VDDO	VDDI	VSS	VSS	B
LAVDL	VSS	LAVDL	LIWSEL	IPL[1]	IDATA_1[0]	VDDO	IPL[2]	IDATA_2 [3]	IDATA_2 [7]	VDDO	IDATA_3 [4]	IPAIS[4]	VDDO	VSS	VDDI	VDDI	VDDI	C
LIWORK_N[2]	LIWORK_N[3]	LIWORK_N[4]	LICMP	VDDO	IDATA_1[1]	IDATA_1 [6]	IDP[2]	IDATA_2 [4]	IPAIS[3]	IDATA_3 [1]	IDATA_3 [6]	VDDO	VSS	VDDI	VSS	VDDO	VSS	D
LIWORK_P[2]	LIWORK_P[3]	LIWORK_P[4]	LECMP	IJ0J1[1]	IDATA_1[2]	IDATA_1 [7]	IDATA_2[0]	VDDO	IJ0J1[3]	IDATA_3 [2]	IDATA_3 [7]	VSS	VDDI	VSS	VDDO	IDATA_4 [0]	VSS	E
													VSS	IDATA_4[1]	IDATA_4 [2]	IDATA_4 [3]	IDATA_4 [4]	F
														VSS	IDATA_4 [5]	IDATA_4 [6]	IDATA_4 [7]	G
													VSS	VSS	VDDO	HB3E[1]	VSS	H
													VSS	VSS	HB3E[2]	HRPOH[1]	HRPOHEN[1]	J
													VSS	VSS	HB3E[3]	HRPOH[2]	HRPOHEN[2]	K
													VDDI	VSS	HB3E[4]	HRPOH[3]	HRPOHEN [3]	L
													VSS	HPOHFP	VDDO	HRPOHEN[4]	VSS	M
													VSS	TPOHFP [1]	TRAD[1]	HPOHCLK	HRPOH[4]	N
													VDDO	TPOHFP [2]	TRAD[2]	TPOH[1]	TPOHEN [1]	P
													VSS	TRAD[3]	TPOH[2]	TPOHEN [2]	VSS	R
													VSS	TPOH[3]	VDDO	TPOHEN [3]	TPOHFP [3]	T
													VDDI	TPOHEN [4]	TPOHFP [4]	TRAD[4]	VSS	U

Bottom Left

V	VSS	EDATA_2[2]	EDATA_2[0]	EDATA_2[1]	VSS											
W	EDP[2]	EPL[2]	VDDOPROG_E	VSS	VSS											
Y	VSS	EJ0J1[2]	EAIS[2]	VSS	VSS											
AA	ETPL_HTPOH[2]	EV5_HTPOHRDY [2]	EIDLE_HTPOHEN[2]	VSS	VDDOPROG_E											
AB	EDATA_1[7]	EDATA_1[6]	EDATA_1[5]	VSS	VDDI											
AC	VSS	EDATA_1[4]	VDDOPROG_E	VSS	VDDOPROG_E											
AD	EDATA_1[3]	EDATA_1[2]	EDATA_1[1]	VSS	VSS											
AE	EDATA_1[0]	EDP[1]	EPL[1]	VSS	VSS											
AF	EJ0J1[1]	EAIS[1]	ETPL_HTPOH[1]	VSS	VSS											
AG	VSS	EV5_HTPOHRDY [1]	VDDOPROG_E	VSS	VSS											
AH	EIDLE_HTPOHEN[1]	HRALMCLK	VSS	VSS	VSS											
AJ	HRALMFP	HRALM	VSS	VDDO	VSS											
AK	VSS	LCLK	VDDO	VSS	VDDI	VSS	SEWORK_N [1]	SEWORK_N [3]	SIWORK_N [1]	SIWORK_N [3]	SEWORK_N [5]	SEWORK_N [7]	SIWORK_N [5]	SIWORK_N [7]	SEPROT_N [1]	SEPROT_N [3]
AL	VSS	VDDO	VSS	VDDI	VSS	VDDO	SEWORK_P [1]	SEWORK_P [3]	SIWORK_P[1]	SIWORK_P[3]	SEWORK_P [5]	SEWORK_P [7]	SIWORK_P[5]	SIWORK_P [7]	SEPROT_P [1]	SEPROT_P [3]
AM	VDDI	VDDI	VDDI	VSS	VDDO	SCANB	VSS	SAVDL	VSS	SAVDL	VSS	SAVDL	VSS	SAVDL	VSS	SAVDL
AN	VSS	VSS	VDDI	VDDO	SEWSEL	VSS	SEWORK_N [2]	SEWORK_N [4]	SIWORK_N [2]	SIWORK_N [4]	SEWORK_N [6]	SEWORK_N [8]	SIWORK_N [6]	SIWORK_N [8]	SEPROT_N [2]	SEPROT_N [4]
AP	VSS	VSS	VDDI	SECMP	RSTB	VSS	SEWORK_P [2]	SEWORK_P [4]	SIWORK_P[2]	SIWORK_P[4]	SEWORK_P [6]	SEWORK_P [8]	SIWORK_P[6]	SIWORK_P [8]	SEPROT_P [2]	SEPROT_P [4]
	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19

Bottom Right

													VSS	D[0]	INTB	TPOH[4]	VSS	V
													VDDO	D[3]	VDDO PROG_M	D[2]	D[1]	W
													VSS	D[6]	D[5]	D[4]	VSS	Y
													VDDO PROG_M	VSS	D[9]	D[8]	D[7]	AA
													VSS	VSS	D[12]	D[11]	D[10]	AB
													VDDI	VSS	VDDO PROG_M	D[13]	VSS	AC
													VSS	VSS	TDO	D[15]	D[14]	AD
													VSS	VSS	TCK	TDI	TRSTB	AE
													VSS	A[2]	A[1]	A[0]	TMS	AF
													VSS	VSS	VDDO	A[3]	VSS	AG
													VSS	VSS	A[6]	A[5]	A[4]	AH
													VSS	A[11]	A[9]	A[8]	A[7]	AJ
SIPROT_N[1]	SIPROT_N[3]	SEPROT_N[5]	SEPROT_N[7]	SIPROT_N[5]	SIPROT_N[7]		SC_AVDL [0]	SAVDH	SC_AVDL [1]	SC_AVDH [1]		VSS	VDDI	VSS	VDDO	A[10]	VSS	AK
SIPROT_P[1]	SIPROT_P[3]	SEPROT_P[5]	SEPROT_P[7]	SIPROT_P[5]	SIPROT_P[7]		SQAVD		SC_AVDL [2]	SAVDL	RDB	A[13]	VSS	VDDI	VSS	VDDO	VSS	AL
VSS	SAVDL	VSS	SAVDL	VSS	SAVDL	VSS			VSS	SAVDH		A[14]	VDDO	VSS	VDDI	VDDI	VDDI	AM
SIPROT_N[2]	SIPROT_N[4]	SEPROT_N[6]	SEPROT_N[8]	SIPROT_N[6]	SIPROT_N[8]	SC_AVDH[0]			SREFCLK_N	EJ0	VDDO	ALE	A[12]	VDDO	VDDI	VSS	VSS	AN
SIPROT_P[2]	SIPROT_P[4]	SEPROT_P[6]	SEPROT_P[8]	SIPROT_P[6]	SIPROT_P[8]	SAVDH	VSS		SREFCLK_P	SICMP	CSB	WRB	VSS	VSS	VDDI	VSS	VSS	AP
18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9 Pin Description

Table 2 Pin Description

Pin Name	Type	Pin No.	Function
Control, Clocking and Microprocessor Bus Interfaces (47 pins)			
REFCLK	Input	T33	**Reference Clock.** The Reference Clock, REFCLK, is an externally generated 77.76 MHz +/-20ppm clock with a nominal 50% duty cycle. REFCLK must be frequency locked to the analog differential reference clock chip inputs LREFCLK_P/N and SREFCLK_P/N. REFCLK pin is implemented with programmable drive I/O. It is controlled by VDDOPROG_E.
RSTB	Input	AP30	**Reset Enable Bar.** The active low reset signal, RSTB, provides an asynchronous TUPP 2488 reset. RSTB is a Schmitt triggered input with an internal pull-up resistor of 30 to 50 kOhms. It is recommended to use an external pull-up resistor of 4.7 kOhms The device must be reset after power up.
CSB	Input	AP7	**Chip Select Bar.** The active low chip select signal, CSB, controls microprocessor access to registers in the TUPP 2488 device. CSB is set low during TUPP 2488 Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses. If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.
RDB	Input	AL7	**Read Enable Bar.** The active low read enable bar signal, RDB, controls microprocessor read accesses to registers in the TUPP 2488 device. RDB is set low and CSB is also set low during TUPP 2488 Microprocessor Interface Port register read accesses. The TUPP 2488 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	AP6	**Write Enable Bar.** The active low write enable bar signal, WRB, controls microprocessor write accesses to registers in the TUPP 2488 device. WRB is set low and CSB is also set low during TUPP 2488 Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.

Pin Name	Type	Pin No.	Function
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AD2 AD1 AC2 AB3 AB2 AB1 AA3 AA2 AA1 Y4 Y3 Y2 W4 W2 W1 V4	**Microprocessor Data Bus.** The bi-directional data bus, D[15:0], is used during TUPP 2488 Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit. D[15:0] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_M.
A[14]/TRS A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	AM6 AL6 AN5 AJ4 AK2 AJ3 AJ2 AJ1 AH3 AH2 AH1 AG2 AF4 AF3 AF2	**Microprocessor Address Bus.** The microprocessor address bus, A[14:0], selects specific Microprocessor Interface Port registers during TUPP 2488 register accesses. A[14] is also the Test Register Select (TRS) address pin and selects between normal and test mode register accesses. TRS is set high during test mode register accesses, and is set low during normal mode register accesses.
ALE	Input	AN6	**Address Latch Enable.** The address latch enable signal, ALE, is active high and latches the address bus (A[14:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the TUPP 2488 to interface to a multiplexed address/data bus. ALE has an internal pull-up resistor of 30 to 50 kOhms. It is recommended to use an external pull-up resistor of 4.7 kOhms.
INTB	Open Drain Output	V3	**Interrupt Request Bar**. The active low interrupt enable signal, INTB, output goes low when a TUPP 2488 interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output. It is recommended to use an external pull-up resistor of 4.7 kOhms on this output signal.

Pin Name	Type	Pin No.	Function
LICMP	Input	D15	**Line Ingress Connection Memory Page.** The line ingress connection memory page select signal LICMP, in combination with an internal register bit, controls the selection of the connection memory page in the ingress line side Time Slot Interchange blocks. LICMP is logically XORed with the internal page select bit and the result is used to select the active connection memory page. When this result is set high, connection memory page 1 is selected. When this result is set low, connection memory page 0 is selected. LICMP is sampled at the J0(C1) byte position of every frame on the ingress bus. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the frame following the next transport frame (i.e. two frame boundaries after LICMP is sampled). LICMP is sampled on the rising edge of REFCLK.
SICMP	Input	AP8	**System Ingress Connection Memory Page.** The system ingress connection memory page select signal, SICMP, controls the selection of the connection memory page in the ingress system side Memory Switch Units (MSUs) and Column Crossbar Switch (CCB). When SICMP is set high, connection memory page 0 is selected in the MSUs and connection memory page 1 is selected in the CCB. When SICMP is set low, connection memory page 1 is selected in the MSUs and connection memory page 0 is selected in the CCB. SICMP is sampled at the J0(C1) byte position of every frame on the ingress bus. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame. SICMP is sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
LECMP	Input	E15	**Line Egress Connection Memory Page.** The line egress connection memory page select signal LECMP, in combination with an internal register bit, controls the selection of the connection memory page in the egress line side Time Slot Interchange blocks. LECMP is logically XORed with the internal page select bit and the result is used to select the active connection memory page. When this result is set high, connection memory page 1 is selected. When this result is set low, connection memory page 0 is selected. LECMP is sampled at the J0(C1) byte position of every frame on the egress bus. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the frame following the next transport frame (i.e. two frame boundaries after LECMP is sampled). LECMP is sampled on the rising edge of REFCLK.
SECMP	Input	AP31	**System Egress Connection Memory Page.** The system egress connection memory page select signal, SECMP, controls the selection of the connection memory page in the egress system Memory Switch Units. When SECMP is set high, connection memory page 0 is selected. When SECMP is set low, connection memory page 1 is selected. SECMP is sampled at the J0(C1) byte position of every frame on the egress bus. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame. SECMP is sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
LIWSEL	Input	C15	**Line Side Ingress Working Serial Data Select.** The line side ingress working serial data select signal, LIWSEL, selects between sourcing line ingress data from the line ingress working serial data link, LIWORK_P[4:1]/LIWORK_N[4:1], or the line ingress protect serial data link, LIPROT_P[4:1]/LIPROT_N[4:1]. When LIWSEL is set low, the working serial bus is selected. When LIWSEL is set high, the protect serial bus is selected. LIWSEL is sampled at the J0(C1) byte location as defined by the ingress serial interface frame pulse signal, IJ0, in serial mode. LIWSEL is sampled at the J0 position indicated by IJ0 and LINE_INGRESS_REF_DLY[13:0] in parallel mode. Changes to the selection of the working and protect serial streams are synchronized to the transport frame boundary of the next frame following the next frame (i.e. two frame boundaries after LIWSEL is sampled). LIWSEL is sampled on the rising edge of REFCLK.
SEWSEL	Input	AN30	**System Side Egress Working Serial Data Select.** The system side egress working serial data select signal, SEWSEL, selects between sourcing system egress data from the system egress working serial data link, SEWORK_P[8:1]/SEWORK_N[8:1], or the system egress protect serial data link, SEPROT_P[8:1]/SEPROT_N[8:1]. When SEWSEL is set low, the working serial bus is selected. When SEWSEL is set high, the protect serial bus is selected. SEWSEL is sampled at the J0(C1) byte location as defined by the egress serial interface frame pulse signal, EJ0. Changes to the selection of the working and protect serial streams are synchronized to the frame boundary of the next frame. SEWSEL must not be changed within two clocks of the sample point (J0 byte location defined by EJ0). SEWSEL is sampled on the rising edge of REFCLK.
IJ0	Input	B15	**Ingress J0(C1) Frame Pulse.** The ingress bus timing signal, IJ0, is a system reference J0(C1) pulse that uses a programmable offset to locate line ingress J0(C1) when using the Line Serial Inputs and the line ingress J0 when using the parallel bus. IJ0 should occur every frame or multiple thereof. IJ0 is sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
EJ0	Input	AN8	**Egress J0(C1) Frame Pulse.** The egress bus timing signal, EJ0, is a system reference J0(C1) pulse that uses a programmable offset to locate system egress J0(C1). EJ0 should occur every 4 frames or multiple thereof. EJ0 is also used to control tributary multiframe alignment (H4) in the VTPA block. EJ0 is sampled on the rising edge of REFCLK.
LCLK	Input	AK33	Performance Monitor 1 second clock. The accuracy of the clock is application dependent, correct operation of the device does not require a specific tolerance. The LCLK input allows external logic to control the PMON transfers within the TUPP 2488 device. A rising edge on LCLK initiates the transfer of PMON statistics within the device. Minimum clock high time is 1.286us. Minimum clock low time is 1.285us. LCLK is an asynchronous input.
Tributary Overhead and Alarm Interface (16 pins)			
TPOH[4] TPOH[3] TPOH[2] TPOH[1]	Output	V2 T4 R3 P2	**Tributary Path Overhead Data.** The tributary path overhead data signal (TPOH[4:1]) contains the tributary path overhead bytes (V5, J2, Z6/N2 and Z7/K4) of all the tributaries extracted from the corresponding line ingress STS-12/STM-4 data stream in non-TU3 mode. In TU-3 mode, TPOH[4:1] contains the tributary path overhead byes (J1, B3, C2, G1, F2, H4, Z3/F3, Z4/K3, and Z5/N1 of all the tributaries extracted from the corresponding line ingress STS-12/STM-4 data stream. TPOH[4:1] is updated on the rising edge of REFCLK.
TPOHEN[4] TPOHEN[3] TPOHEN[2] TPOHEN[1]	Output	U4 T2 R2 P1	**Tributary Path Overhead Enable.** The tributary path overhead enable (TPOHEN[4:1]) signals may be used to identify tributary path overhead bytes that are being presented on the TPOH stream of the corresponding STS-12/STM-4 for the first time. Each TPOHEN signal is set high when a fresh overhead byte is available on the corresponding POH stream. TPOHEN is set low when the tributary path overhead byte available on the corresponding TPOH stream has already been shifted out in a previous frame. TPOHEN[4:1] is updated on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
TPOHFP[4] TPOHFP[3] TPOHFP[2] TPOHFP[1]	Output	U3 T1 P4 N4	**Tributary Path Overhead Frame Pulse.** The tributary path overhead frame pulse (TPOHFP[4:1]) signals may be used to locate the individual path overhead bits of each tributary for the corresponding STS-12/STM-4 stream. Each TPOHFP signal is set high to mark bit 1 (the most significant bit) of the V5 byte of the first tributary. TPOHFP[4:1] is updated on the rising edge of REFCLK.
TRAD[4] TRAD[3] TRAD[2] TRAD[1]	Output	U2 R4 P3 N3	**Tributary Remote Alarm Port.** The remote alarm port (TRAD[4:1]) contains the tributary path BIP error count, the RDI status and the PDI status of each tributary in the corresponding STS-12/STM-4 when the TRAD_BIPE_SEL register is '0'. In this case the BIP-8 count for TU3s is output over 4 timeslots. When TRAD_BIPE_SEL is '1' the BIP-8 count for TU3s is output in one timeslot. Refer to Section 14.6 for a detailed description of the TRAD port. TRAD[4:1] is updated on the rising edge of REFCLK.
High Order Path Overhead and Alarm Interface (17 pins)			
HPOHFP	Output	M4	**High Order Path Overhead Frame Pulse.** The high order path overhead frame pulse signal provides frame reference timing for serial path overhead extraction and insertion streams. HPOHFP is used to indicate the most significant bit (MSB) of the J1 byte on HRPOH[4:1] and the first possible path BIP error on HB3E[4:1]. HPOHFP can be sampled on the rising edge of HPOHCLK. HPOHFP is updated on the falling edge of HPOHCLK.
HPOHCLK	Output	N2	**High Order Path Overhead Clock.** The high order path overhead clock signal provides timing for the serial path overhead extraction and insertion streams. This clock is a nominal 20.736 MHz clock generated by dividing down and gapping the 77.76 MHz reference clock (REFCLK). HPOHCLK has a 33% high duty cycle.

Pin Name	Type	Pin No.	Function
HRPOH[4] HRPOH[3] HRPOH[2] HRPOH[1]	Output	N1 L2 K2 J2	**High Order Receive Path Overhead.** The high order receive path overhead signals contain the received path overhead bytes (J1, B3, C2, G1, F2, H4, F3, K3, and N1) extracted from the high order SONET/SDH path overhead. The HRPOHEN[4:1] signal is set high to indicate new path overhead bytes on HRPOH[4:1]. HRPOH[4:1] is updated on the falling edge of HPOHCLK.
HRPOHEN[4] HRPOHEN[3] HRPOHEN[2] HRPOHEN[1]	Output	M2 L1 K1 J1	**High Order Receive Path Overhead Enable.** The high order receive path overhead enable signals indicates new path overhead bytes on HRPOH[4:1]. When HRPOHEN[4:1] signal is set high, the corresponding path overhead byte presented on HRPOH[4:1] are available for the first time. When HRPOHEN[4:1] is set low, the corresponding path overhead byte presented on HRPOH[4:1] have already been available. HRPOHEN[4:1] is updated on the falling edge of HPOHCLK.
HB3E[4] HB3E[3] HB3E[2] HB3E[1]	Output	L3 K3 J3 H2	**High Order Bit Interleaved Parity Error.** The high order bit interleaved parity error signal carries the path BIP-8 errors detected for each high order SONET/SDH payload. Path BIP-8 errors are detected by XORing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. HB3E[4:1] is updated on the falling edge of HPOHCLK.
HRALM	Output	AJ33	**High Order Receive Alarm bus.** The HRALM signal outputs the high order receive path alarm. The alarm represents the logical OR of the LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PLM, PDI-P, TIU-P, TIM-P status of up to 48 high order SONET/SDH paths. The selection of alarms to be reported is controlled by the TUPP 2488 SARC48 Path RALM Enable registers. HRALM is set low when none of the enabled defects is active. HRALM is time multiplexed among the STS-1/STM-0 paths. HRALM is updated on the falling edge of HRALMCLK.

Pin Name	Type	Pin No.	Function
HRALMCLK	Output	AH33	**High Order Receive Path Alarm Clock.** HRALMCLK is used to externally sample HRALM and HRALMFP. HRALMCLK is a nominal 20.736MHz clock or 2592-clock pulse at each 125-us. This clock is derived from a 77.76 MHz clock divided by three and the low level is gapped by an addition of 6 REFCLK cycles to produce the 20.736 MHz. During 8 cycles the high duty cycle is 33%.
HRALMFP	Output	AJ34	**High Order Receive Path Alarm Frame Pulse.** HRALMFP is used to identify the bit position of HRALM. HRALMFP is asserted for one HRALMCLK clock cycles every 125 µs, and identifies the first alarm position. HRALMFP is updated on the falling edge of HRALMCLK.
Ingress and Egress Byte-Wide TelecomBus Interface (96 pins: 48 Ingress, 48 Egress)			
IDATA_4[7] IDATA_4[6] IDATA_4[5] IDATA_4[4] IDATA_4[3] IDATA_4[2] IDATA_4[1] IDATA_4[0] IDATA_3[7] IDATA_3[6] IDATA_3[5] IDATA_3[4] IDATA_3[3] IDATA_3[2] IDATA_3[1] IDATA_3[0] IDATA_2[7] IDATA_2[6] IDATA_2[5] IDATA_2[4] IDATA_2[3] IDATA_2[2] IDATA_2[1] IDATA_2[0] IDATA_1[7] IDATA_1[6] IDATA_1[5] IDATA_1[4] IDATA_1[3] IDATA_1[2] IDATA_1[1] IDATA_1[0]	Input	G1 G2 G3 F1 F2 F3 F4 E2 E7 D7 B6 C7 B7 E8 D8 A7 C9 B9 A9 D10 C10 B10 A11 E11 E12 D12 B12 A13 B13 E13 D13 C13	**Ingress Bus Data.** The Ingress Bus data, carries the 32-bit serial STS-48c/STS-36c/STS-24c/STS-12c/STS-3c/STS-1 SONET payload or AU4-16c/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3 SDH payload when the device is configured in STS-48/STM-16 mode or carries the four byte serial STS-12c/STS-3c/STS-1 SONET payload or AU4-4c/AU4/AU3/TU3 SDH payload when the device is configured in quad STS-12/STM-4 mode. IDATA_N[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit received first. IDATA_N[0] is the least significant bit, corresponding to bit 8 of each serial word, the bit received last. IDATA_N[7:0] is sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
IDP[4] IDP[3] IDP[2] IDP[1]	Input	A4 B8 D11 B14	**Ingress Bus Data Parity.** The Ingress Bus data parity signal, IDP[4:1], carries the parity of the ingress signals. The parity calculation encompasses the IDATA_N[7:0] bus and optionally the IJ0J1[N] and IPL[N] signals. IJ0J1[N] and IPL[N] can be included in the parity calculation by setting the INGJ0J1PAREN and INGPLPAREN bits in the Parity Control register high, respectively. Odd parity is selected by setting the INGODDPAREN bit in the Parity Control register high and even parity is selected by setting the INGODDPAREN bit low. IDP[4:1] is sampled on the rising edge of REFCLK.
IPL[4] IPL[3] IPL[2] IPL[1]	Input	B5 A8 C11 C14	**Ingress Bus Payload.** The active high Ingress Bus payload signal, IPL[4:1], indicates when the IDATA[4:1][7:0] bus is carrying a payload byte. IPL[4:1] identifies the bytes on the incoming stream IDATA[4:1][7:0] that are part of the synchronous payload envelope. IPL[4:1] is set high during path overhead and payload bytes and low during transport overhead bytes. When the H3 byte contains part of the synchronous payload envelope due to a negative pointer justification, IPL[4:1] is set high; when a byte is a dummy byte due to a positive pointer justification, IPL[4:1] is set low. Also, IPL[4:1] is set high during bytes of the two fixed stuff columns in an STM-1 containing TU3's, as these stuff bytes are aligned relative to the VC4's J1 byte). IPL[4:1] is sampled on the rising edge of REFCLK.
IJ0J1[4] IJ0J1[3] IJ0J1[2] IJ0J1[1]	Input	A5 E9 B11 E14	**Ingress J0/J1 Frame Pulse.** The Ingress J0/J1 frame pulse, IJ0J1[4:1], identifies the transport envelope and synchronous payload envelope frame boundaries on the ingress SONET/SDH stream. IJ0J1[N] is set high while IPL[N] is low to mark the first J0(C1) byte of the transport envelope frame on the IDATA_N[7:0] bus. IJ0J1[N] is set high while IPL[N] is high to mark each J1 byte of the synchronous payload envelope(s) on the IDATA_N[7:0] bus. IJ0J1[N] must be present at every occurrence of the first J0(C1) and all J1 bytes. The J0 byte on all 4 streams must be coincident. IJ0J1[4:1] is sampled on the rising edge of REFCLK.

Pin Name	Type	Pin No.	Function
IPAIS[4] IPAIS[3] IPAIS[2] IPAIS[1]	Input	C6 D9 A12 A15	**Ingress High Order Path AIS.** The Ingress high order path alarm bus, IPAIS[4:1], identifies STS/STM streams on the corresponding ingress data bus (IDATA[4:1][7:0]) that are in high order path AIS state. IPAIS[N] is set high when the stream on IDATA_N[7:0] is in AIS and is set low when the stream is out of AIS state. IPAIS[4:1] is sampled on the rising edge of REFCLK.
EDATA_4[7] EDATA_4[6] EDATA_4[5] EDATA_4[4] EDATA_4[3] EDATA_4[2] EDATA_4[1] EDATA_4[0] EDATA_3[7] EDATA_3[6] EDATA_3[5] EDATA_3[4] EDATA_3[3] EDATA_3[2] EDATA_3[1] EDATA_3[0] EDATA_2[7] EDATA_2[6] EDATA_2[5] EDATA_2[4] EDATA_2[3] EDATA_2[2] EDATA_2[1] EDATA_2[0] EDATA_1[7] EDATA_1[6] EDATA_1[5] EDATA_1[4] EDATA_1[3] EDATA_1[2] EDATA_1[1] EDATA_1[0]	Output	B28 A29 B29 A30 B30 E33 F32 F33 J34 K32 K33 K34 L32 L33 L34 M33 R33 T34 U32 U31 U33 V33 V31 V32 AB34 AB33 AB32 AC33 AD34 AD33 AD32 AE34	**Egress Bus Data.** The Egress Bus data, carries the 32-bit serial STS-48c/STS-36c/STS-24c/STS-12c/STS-3c/STS-1 SONET payload or AU4-16c/AU4-12c/ AU4-8c/AU4-4c/AU4/AU3/TU3 SDH payload to be transmitted when the device is configured in STS-48/STM-16 mode or carries the four byte serial STS-12c/STS-3c/STS-1 SONET payload or AU4-4c/AU4/AU3/TU3 SDH payload to be transmitted when the device is configured in quad STS-12/STM-4 mode. EDATA_N[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. EDATA_N[0] is the least significant bit, corresponding to bit 8 of each serial word, the bit transmitted last. EDATA_N[7:0] is updated on the rising edge of REFCLK. EDATA_N[7:0] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.

Pin Name	Type	Pin No.	Function
EDP[4] EDP[3] EDP[2] EDP[1]	Output	F34 N32 W34 AE33	**Egress Bus Data Parity.** The Egress Bus data parity signal, EDP[4:1], carries the parity of the egress signals. The parity calculation encompasses the EDATA[N][7:0] bus and optionally the EJ0J1 [N] and EPL[N] signals. EJ0J1[N] and EPL[N] can be included in the parity calculation by setting the EGJ0J1PAREN and EGPLPAREN register bits in the Parity Control register high, respectively. Odd parity is selected by setting the EGODDPAREN register bit in the same register high and even parity is selected by setting the EGODDPAREN bit low. EDP[4:1] is updated on the rising edge of REFCLK. EDP[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.
EPL[4] EPL[3] EPL[2] EPL[1]	Output	G32 N33 W33 AE32	**Egress Bus Payload Active.** The Egress Bus payload active signal, EPL[4:1], identifies the payload bytes on EDATA[4:1][7:0]. EPL[4:1] identifies the bytes on the egress stream EDATA[4:1][7:0] that are part of the synchronous payload envelope. EPL[4:1] is set high during path overhead and payload bytes and low during transport overhead bytes. When the H3 byte contains part of the synchronous payload envelope due to a negative pointer justification, EPL[4:1] is set high; when a byte is a dummy byte due to a positive pointer justification, EPL[4:1] is set low. Also, EPL[4:1] is set high during bytes of the two fixed stuff columns in an STM-1 containing TU3's, as these stuff bytes are aligned relative to the VC4's J1 byte). EPL[4:1] is updated on the rising edge of REFCLK. EPL[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.

Pin Name	Type	Pin No.	Function
EJ0J1[4] EJ0J1[3] EJ0J1[2] EJ0J1[1]	Output	G33 N34 Y33 AF34	**Egress Bus Composite Timing Signal.** The Egress Bus composite timing signal, EJ0J1[4:1], identifies the frame, payload and tributary multiframe boundaries on the Egress Data bus EDATA[4:1][7:0]. EJ0J1[4:1] pulses high with the Egress Bus Payload Active signal EPL[4:1] set low to mark the first STS-1 (STM-0/AU3) identification byte or equivalently the STM identification byte J0(C1). Optionally the EJ0J1[4:1] signal pulses high with EPL[4:1] set high to mark the path trace byte J1. The J0 byte on all 4 streams will be coincident. Optionally the EJ0J1[4:1] signal pulses high on the V1 byte to indicate tributary multiframe boundaries. The V1 indicator on this bus is only valid in Payload-Processor Loopback in TUPP 2488. Disable indication of the V1 byte when connecting the TUPP 2488 to a TUPP 622 or TEMUX 84 devices, as these devices do not require V1 indication. EJ0J1 [4:1] is updated on the rising edge of REFCLK. EJ0J1[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.
EAIS[4] EAIS[3] EAIS[2] EAIS[1]	Output	G34 P32 Y32 AF33	**Egress Alarm Indication Signal.** The Egress Alarm Indication Signal bus, EAIS[4:1], identifies bytes of STS-N/STM-M streams that are in high-order path AIS alarm on the corresponding egress data bus (EDATA[4:1][7:0]). EAIS[N] is set high to mark the stream in AIS alarm on the EDATA[N][7:0] bus except during STS-N/STM-M J0 and Z0 byte locations when the contents of EAIS[4:1] is invalid. EAIS[4:1] also identifies bytes of tributary unit streams that are in low-order path AIS alarm on the corresponding egress data bus (EDATA[4:1][7:0]). EAIS[N] is set high to mark the stream in AIS alarm on the EDATA[N][7:0] bus. EAIS[4:1] indicates tributary AIS for all traffic that is processed through the tributary path of the Payload and indicates high order path AIS for STS-1s processed through the payload processor bypass path. EAIS[4:1] is updated on the rising edge of REFCLK. EAIS[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.

Pin Name	Type	Pin No.	Function
Egress Low Order and High Order Path Overhead Insertion Shared Pins (12 pins)			
ETPL_HTPOH[4] ETPL_HTPOH[3] ETPL_HTPOH[2] ETPL_HTPOH[1]	Bidi Output for PP Only mode Input otherwise	H33 P33 AA34 AF32	**Egress Tributary Payload Active and High Order Transmit Path Overhead ETPL_HTPOH[4:1].** **Note:** When the device is configured in Payload Processor Loopback Only mode, High Order Transmit Path overhead insertion is not supported and low order egress telecom bus signals are supported. In this mode the pin functions as **ETPL[4:1]** output bus. **Note:** When the device is **not** configured in Payload Processor Loopback Only mode the low order egress telecom bus signals are not supported and High Order Transmit Path overhead insertion is supported. In this mode the pin functions as **HTPOH[4:1]** input bus **Egress Tributary Payload Active (ETPL[4:1]).** The Egress tributary payload active bus, ETPL[4:1], is set high to mark each tributary synchronous payload / low order virtual container byte in the corresponding egress data bus (EDATA[4:1][7:0]). ETPL[N] is set low at STS/STM transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1, V2, V3 and V4). When the V3 byte of the tributary transport overhead contains part of the tributary SPE due to a negative pointer justification, ETPL[4:1] is set high; when a byte is a dummy byte due to a positive tributary pointer justification, ETPL[4:1] is set low. When a TUG3 contains TUG2's, ETPL[4:1] is set low during the columns containing the NPI byte and the fixed stuffing byte of the TUG3). In Payload Processor Loopback Only mode ETPL_HTPOH[4:1] is an output (ETPL[4:1]) and is updated on the rising edge of REFCLK. **High Order Transmit Path Overhead. (HTPOH[4:1)** The high order transmit path overhead signal contains the path overhead bytes (J1, B3, C2, G1, F2, H4, F3, K3, and N1) to be transmitted in the high order SONET/SDH path overhead. A path overhead byte is accepted for transmission when the external source indicates a valid byte (EIDLE_HTPOHEN[4:1] set high) and the TUPP 2488 indicates ready (EV5_HTPOHRDY[4:1] set high). The EV5_HTPOHRDY[4:1] is set low to indicate the TUPP 2488 is not ready, and the byte must be re-presented at the next opportunity.

Pin Name	Type	Pin No.	Function
			When not in Payload Processor Loopback Only mode ETPL_HTPOH[4:1] is an input (HTPOH[4:1]) and is sampled on the rising edge of HPOHCLK. ETPL_HTPOH[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.
EV5_HTPOHRDY[4] EV5_HTPOHRDY[3] EV5_HTPOHRDY[2] EV5_HTPOHRDY[1]	Output	J32 P34 AA33 AG33	**Egress Tributary Payload Frame Pulse and High Order Transmit Path Overhead Insert Ready EV5_HTPOHRDY[4:1].** **Note:** When the device is configured in Payload Processor Loopback Only mode, High Order Transmit Path overhead insertion is not supported and low order egress telecom bus signals are supported. In this mode the pin functions as **EV5[4:1]** output bus. **Note:** When the device is **not** configured in Payload Processor Loopback Only mode the low order egress telecom bus signals are not supported and High Order Transmit Path overhead insertion is supported. In this mode the pin functions as **HTPOHRDY[4:1]** output bus. **Egress Tributary Payload Frame Pulse.** The egress tributary payload frame pulse bus, EV5[4:1], identifies the tributary synchronous payload envelope / low order virtual container frame boundaries on the corresponding egress data bus (EDATA[4:1][7:0]). EV5[N] is set high to mark the various V5 bytes on the EDATA[N][7:0] bus. In Payload Processor Loopback Only mode EV5_HTPOHRDY [4:1] is an output (EV5) and is updated on the rising edge of REFCLK. **High Order Transmit Path Overhead Insert Ready**. HTPOHRDY[4:1] is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the ETPL_HTPOH[4:1] input. This byte will be accepted if EIDLE_HTPOHEN[4:1] is also set high. When not in Payload Processor Loopback Only mode EV5_HTPOHRDY[4:1] is an output (HTPOHRDY[4:1]) and is updated on the falling edge of HPOHCLK.TUPP 2488. EV5_HTPOHRDY[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.

Pin Name	Type	Pin No.	Function
EIDLE_HTPOHEN[4] EIDLE_HTPOHEN [3] EIDLE_HTPOHEN [2] EIDLE_HTPOHEN [1]	Bidi Output for PP Only mode Input otherwise	J33 R32 AA32 AH34	**Egress Tributary Idle Indication Signal and High Order Transmit Path Overhead Insert Enable EIDLE_HTPOHEN[4:1].** **Note:** When the device is configured in Payload Processor Loopback Only mode, High Order Transmit Path overhead insertion is not supported and low order egress telecom bus signals are supported. In this mode the pin functions as **EIDLE[4:1]** output bus. **Note:** When the device is **not** configured in Payload Processor Loopback Only mode the low order egress telecom bus signals are not supported and High Order Transmit Path overhead insertion is supported. In this mode the pin functions as **HTPOHEN[4:1]** input bus. **Egress Tributary Idle Indication Signal.** The egress tributary idle indication signal, EIDLE[4:1], identifies tributaries on the egress data bus (EDATA[4:1][7:0]) that are in idle state. EIDLE[N] is set high when idle code is inserted in the associated tributary on the EDATA[N][7:0] bus, and is set low when the idle code is not inserted (EIDLE can be asserted due to UNEQ condition for bytes in the VC only). In Payload Processor Loopback Only mode EIDLE_HTPOHEN[4:1] is an output (EIDLE) and is updated on the rising edge of REFCLK. **High Order Transmit Path Overhead Insert Enable.** The high order transmit path overhead insert enable signal HTPOHEN[4:1], controls the insertion of the transmit path overhead data which is inserted in the outgoing stream. HTPOHEN[4:1] shall be set high during the most significant bit of a POH byte to indicate valid data on the ETPL_HTPOH[4:1] input. This byte will be accepted for transmission if EV5_HTPOHRDY[4:1] is also set high. When not in Payload Processor Loopback Only mode EIDLE_HTPOHEN[4:1] is an input (HTPOHEN[4:1]) and is sampled on the rising edge of HPOHCLK. When the HTPOH port is not used, this pins must be tied to low. EIDLE_HTPOHEN[4:1] pins are implemented with programmable drive I/O. They are controlled by VDDOPROG_E.

Pin Name	Type	Pin No.	Function
Line Ingress and Line Egress Serial RASIO™ CML Interface (32 pins)			
LIWORK_P[4] LIWORK_N[4] LIWORK_P[3] LIWORK_N[3] LIWORK_P[2] LIWORK_N[2] LIWORK_P[1] LIWORK_N[1]	Analog CML Input	E16 D16 E17 D17 E18 D18 E19 D19	**Line Ingress Working Serial Data.** IWORK_P[4:1]/LIWORK_N[4:1] carries the ingress STS-12/STM-4 stream from a working source on the line side, in bit serial format. LIWORK_P[4:1]/LIWORK_N[4:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is expected first and the bit 'j' is expected last. Alternatively, LIWORK_P[4:1]/LIWORK_N[4:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs. Alternatively, LIWORK_P[1]/LIWORK_N[1] are 2.488 Gbit/s STS-48/STM-16 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs and LIWORK_P[4:2]/LIWORK_N[4:2] are unused.
LIPROT_P[4] LIPROT_N[4] LIPROT_P[3] LIPROT_N[3] LIPROT_P[2] LIPROT_N[2] LIPROT_P[1] LIPROT_N[1]	Analog CML Input	B16 A16 B17 A17 B18 A18 B19 A19	**Line Ingress Protect Serial Data.** LIPROT_P[4:1]/LIPROT_N[4:1] carries the ingress STS-12/STM-4 stream from a protection source on the line side, in bit serial format. LIPROT_P[4:1]/LIPROT_N[4:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is expected first and the bit 'j' is expected last. Alternatively, LIPROT_P[4:1]/LIPROT_N[4:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs. Alternatively, LIPROT_P[1]/LIPROT_N[1] are 2.488 Gbit/s STS-48/STM-16 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs and LIPROT_P[4:2]/LIPROT_N[4:2] are unused.

Pin Name	Type	Pin No.	Function
LEWORK_P[4] LEWORK_N[4] LEWORK_P[3] LEWORK_N[3] LEWORK_P[2] LEWORK_N[2] LEWORK_P[1] LEWORK_N[1]	Analog CML Output	E23 D23 E22 D22 E21 D21 E20 D20	**Line Egress Working Serial Data.** LEWORK_P[4:1]/LEWORK_N[4:1] carries the egress STS-12/STM-4 stream to a working sink on the line side, in bit serial format. LEWORK_P[4:1]/LEWORK_N[4:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Alternatively, LEWORK_P[4:1]/LEWORK_N[4:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs. Alternatively, LEWORK_P[1]/LEWORK_N[1] are 2.488 Gbit/s STS-48/STM-16 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs and LEWORK_P[4:2]/LEWORK_N[4:2] are unused.
LEPROT_P[4] LEPROT_N[4] LEPROT_P[3] LEPROT_N[3] LEPROT_P[2] LEPROT_N[2] LEPROT_P[1] LEPROT_N[1]	Analog CML Output	B23 A23 B22 A22 B21 A21 B20 A20	**Line Egress Protect Serial Data.** LEPROT_P[4:1]/LEPROT_N[4:1] carries the egress STS-12/STM-4 stream to a protection sink on the line side, in bit serial format. LEPROT_P[4:1]/LEPROT_N[4:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Alternatively, LEPROT_P[4:1]/LEPROT_N[4:1] are 622.08 Mbit/s STS-12/STM-4 data streams, using A1, A2 framing with scrambling and B1 BIPs. Alternatively, LEPROT_P[1]/LEPROT_N[1] are 2.488 Gbit/s STS-48/STM-16 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs and LEPROT_P[4:2]/LEPROT_N[4:2] are unused.

Pin Name	Type	Pin No.	Function
System Ingress and System Egress Serial RASIO™ CML Interface (64 pins)			
SEWORK_P[8] SEWORK_N[8] SEWORK_P[7] SEWORK_N[7] SEWORK_P[6] SEWORK_N[6] SEWORK_P[5] SEWORK_N[5] SEWORK_P[4] SEWORK_N[4] SEWORK_P[3] SEWORK_N[3] SEWORK_P[2] SEWORK_N[2] SEWORK_P[1] SEWORK_N[1]	Analog CML Input	AP23 AN23 AL23 AK23 AP24 AN24 AL24 AK24 AP27 AN27 AL27 AK27 AP28 AN28 AL28 AK28	**System Egress Working Serial Data.** SEWORK_P[8:1]/SEWORK_N[8:1] carries the egress STS-12/STM-4 stream from a working source on the system side, in bit serial format. SEWORK_P[8:1]/SEWORK_N[8:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit ‘a’ is expected first and the bit ‘j’ is expected last. Alternatively, SEWORK_P[8:1]/SEWORK_N[8:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs.
SEPROT_P[8] SEPROT_N[8] SEPROT_P[7] SEPROT_N[7] SEPROT_P[6] SEPROT_N[6] SEPROT_P[5] SEPROT_N[5] SEPROT_P[4] SEPROT_N[4] SEPROT_P[3] SEPROT_N[3] SEPROT_P[2] SEPROT_N[2] SEPROT_P[1] SEPROT_N[1]	Analog CML Input	AP15 AN15 AL15 AK15 AP16 AN16 AL16 AK16 AP19 AN19 AL19 AK19 AP20 AN20 AL20 AK20	**System Egress Protect Serial Data.** SEPROT_P[8:1]/SEPROT_N[8:1] carries the egress STS-12/STM-4 stream from a protection source on the system side, in bit serial format. SEPROT_P[8:1]/SEPROT_N[8:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit ‘a’ is expected first and the bit ‘j’ is expected last. Alternatively, SEPROT_P[8:1]/SEPROT_N[8:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs.

Pin Name	Type	Pin No.	Function
SIWORK_P[8] SIWORK_N[8] SIWORK_P[7] SIWORK_N[7] SIWORK_P[6] SIWORK_N[6] SIWORK_P[5] SIWORK_N[5] SIWORK_P[4] SIWORK_N[4] SIWORK_P[3] SIWORK_N[3] SIWORK_P[2] SIWORK_N[2] SIWORK_P[1] SIWORK_N[1]	Analog CML Output	AP21 AN21 AL21 AK21 AP22 AN22 AL22 AK22 AP25 AN25 AL25 AK25 AP26 AN26 AL26 AK26	**System Ingress Working Serial Data.** SIWORK_P[8:1]/SIWORK_N[8:1] carries the ingress STS-12/STM-4 stream to a working sink on the system side, in bit serial format. SIWORK_P[8:1]/SIWORK_N[8:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Alternatively, SIWORK_P[8:1]/SIWORK_N[8:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs.
SIPROT_P[8] SIPROT_N[8] SIPROT_P[7] SIPROT_N[7] SIPROT_P[6] SIPROT_N[6] SIPROT_P[5] SIPROT_N[5] SIPROT_P[4] SIPROT_N[4] SIPROT_P[3] SIPROT_N[3] SIPROT_P[2] SIPROT_N[2] SIPROT_P[1] SIPROT_N[1]	Analog CML Output	AP13 AN13 AL13 AK13 AP14 AN14 AL14 AK14 AP17 AN17 AL17 AK17 AP18 AN18 AL18 AK18	**System Ingress Protect Serial Data.** SIPROT_P[8:1]/SIPROT_N[8:1] carries the ingress STS-12/STM-4 stream to a protection sink on the system side, in bit serial format. SIPROT_P[8:1]/SIPROT_N[8:1] are 777.6 Mbit/s data streams encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Alternatively, SIPROT_P[8:1]/SIPROT_N[8:1] are 622.08 Mbit/s STS-12/STM-4 formatted data streams, using A1, A2 framing with scrambling and B1 BIPs.
JTAG Interface (5 pins)			
TCK	Input	AE3	**Test Clock.** The JTAG test clock signal, TCK, provides timing for test operations that are carried out using the IEEE P1149.1 test access port.

Pin Name	Type	Pin No.	Function
TMS	Input	AF1	**Test Mode Select.** The JTAG test mode select signal, TMS, controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor of 30 to 50 kOhms. It is recommended to use an external pull-up resistor of 4.7 kOhms.
TDI	Input	AE2	**Test Data Input.** The JTAG test data input signal, TDI, carries test data into the TUPP2488 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor of 30 to 50 kOhms. It is recommended to use an external pull-up resistor of 4.7 kOhms.
TDO	Tristate Output	AD3	**Test Data Output.** The JTAG test data output signal, TDO, carries test data out of the TUPP2488 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	AE1	**Test Reset Bar.** The active low JTAG test reset signal, TRSTB, provides an asynchronous TUPP2488 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an internal pull-up resistor of 30 to 50 kOhms. It is recommended to use an external pull-up resistor of 4.7 kOhms. Note that for normal device operation, the boundary scan state machine must be reset. This may be done by strobing TRSTB low at the same time as the active-low chip reset pin. If the boundary scan state machine is not reset, some or all device I/O pins may be held in test modes.
Test Interface (1 pin)			
SCANB	Input	AM29	This pin is for test purpose. For normal operation this pin should be tied to VDDO.
Analog Miscellaneous Signals (Line Side) (10 pins)			

Pin Name	Type	Pin No.	Function
LREFCLK_P LREFCLK_N	2.5 V LV-PECL externally AC-coupled input	A27 B27	**Line Side Analog Reference Clock.** These differential signals provide a reference clock for the clock synthesis unit on the line side of TUPP 2488. LREFCLK_P/N must be a 155.52 MHz clock, with a nominal 50% duty cycle. The reference frequency differential input signal should be derived from an external source. The signals are AC-coupled to a RASIO™ CML Receiver before being used by the CSU. The reference frequencies are expected to be PECL level signals for better jitter performance of the system. LREFCLK_P/N and SREFCLK_P/N must be frequency locked to the digital reference clock chip input REFCLK
Reserved	Analog Output	A24 B24	These pins are reserved and should be left floating.
Reserved	Analog I/O	D25 C25	These pins are reserved and should be left floating.
Reserved	Analog I/O	D26 C26 B26 A26	These pins are reserved and should be left floating.
Analog Miscellaneous Signals (System Side) (10 pins)			
SREFCLK_P SREFCLK_N	2.5 V LV-PECL externally AC-coupled input	AP9 AN9	**System Side Analog Reference Clock.** These differential signals provide a reference clock for the clock synthesis unit on the line side of TUPP 2488. SREFCLK_P/N must be a 155.52 MHz clock, with a nominal 50% duty cycle. The reference frequency differential input signal should be derived from an external source. The signals are AC-coupled to a RASIO™ CML Receiver before being used by the CSU. The reference frequencies are expected to be PECL level signals for better jitter performance of the system. LREFCLK_P/N and SREFCLK_P/N must be frequency locked to the digital reference clock chip input REFCLK
Reserved	Analog Output	AK12 AL12	These pins are reserved and should be left floating.
Reserved	Analog I/O	AN11 AM11	These pins are reserved and should be left floating.
Reserved	Analog I/O	AP10 AN10 AM10 AL10	These pins are reserved and should be left floating.

Pin Name	Type	Pin No.	Function
Analog Power and Ground (Line Side) (14 pins)			
LQAVD	Analog Power (2.5V)	B25	Quiet analog power (**LQAVD)** is a +2.5V power supply. **LQAVD** should be connected to a +2.5V power supply de-coupled externally to GROUND. Please refer to TUPP 2488 Board Design Guidelines (PMC-2020238) for decoupling information on this signal.
LC_AVDL[2] LC_AVDL[1] LC_AVDL[0]	Analog Power (1.2V)	C27 E26 E24	The line side quiet CSU analog power (**LC_AVDL[2:0]**) pins are connected to a +1.2V power supply for the quiet analog blocks. Please refer to TUPP 2488 Board Design Guidelines (PMC-2020238) for decoupling information on this signal.
LC_AVDH[1] LC_AVDH[0]	Analog Power (2.5V)	E27 D24	The line side quiet CSU analog power (**LC_AVDH[1:0]**) pins are connected to a +2.5V power supply for the quiet analog blocks. Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal.
LAVDL	1.2V Analog Power	D27 C24 C22 C20 C18 C16	This is a shared 1.2V power supply to all line side analog blocks on the chip. Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal
LAVDH	2.5V Analog Power	E25 C28	This is shared 2.5V power supply to all line side analog blocks in the chip. . Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal
Analog Power and Ground (System Side) (18 pins)			
SQAVD	Analog Power (2.5V)	AL11	Quiet analog power (**SQAVD)** is a +2.5V power supply. **SQAVD** should be connected to a +2.5V power supply de-coupled externally to GROUND via a 0.1μF ceramic decoupling capacitor for proper HF noise shunting.
SC_AVDL[2] SC_AVDL[1] SC_AVDL[0]	Analog Power (1.2V)	AL9 AK9 AK11	The system side quiet CSU analog power (**SC_AVDL[2:0]**) pins are connected to a +1.2V power supply for the quiet analog blocks Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal.
SC_AVDH[1] SC_AVDH[0]	Analog Power (2.5V)	AK8 AN12	The system side quiet CSU analog power (**SC_AVDH[1:0]**) pins are connected to a +2.5V power supply for the quiet analog blocks. Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal.

Pin Name	Type	Pin No.	Function
SAVDL	1.2V Analog Power	AM27 AM25 AM23 AM21 AM19 AM17 AM15 AM13 AL8	This is a shared 1.2V power supply to all system side analog blocks on the chip. Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal.
SAVDH	2.5V Analog Power	AP12 AM8 AK10	This is shared 2.5V power supply to all system side analog blocks in the chip. Please refer to TUPP 2488 Board Design Guidelines for decoupling information on this signal.
Digital Core Power (34 pins)			
VDDI	1.2V Power	A3 A32 AB30 AC5 AK5 AK30 AL4 AL31 AM1 AM2 AM3 AM32 AM33 AM34 AN3 AN32 AP3 AP32 B3 B32 C1 C2 C3 C32 C33 C34 D4 D31 E5 E30 L5 L30 U5 U30	The digital core power pins, VDDI, should be connected to a well-decoupled +1.2 V DC supply.

Pin Name	Type	Pin No.	Function
Digital I/O Power (47 pins)			
VDDO	2.5V Power	AG3 AJ31 AK3 AK32 AL2 AL29 AL33 AM5 AM30 AN4 AN7 AN31 B4 C5 C8 C12 D2 D6 D14 E3 E10 E28 H3 M3 P5 R30 T3 W5	The digital I/O power pins, VDDO, should be connected to a well-decoupled +2.5 V DC supply.
VDDOPROG_E	2.5V or 3.3V Power	AA30 AC30 AC32 AG32 B31 C30 D29 D33 E32 F31 H32 K30 M32 P30 T32 W32	This supply may be connected to either a 2.5V or 3.3V supply dependant on the application requirements for the egress telecom bus signals (including the pins shared with the High Order Transmit Path Overhead interface) i.e. EDATA, EDP, EPL, EAIS, EJ0J1, ETPL_HTPOH, EV5_HTPOHRDY, EIDLE_HTPOHEN. If a 3.3V device is being interfaced to these signals telecom bus the VDDOPROG_E should be 3.3V. If a 2.5V device is being interfaced to the egress TelecomBus the VDDOPROG_E should be 2.5V.
VDDOPROG_M	2.5V or 3.3V Power	AA5 AC3 W3	This supply may be connected to either a 2.5V or 3.3V supply dependant on the application requirements for the MPIF data signals (D[15:0]). If a 3.3V device is being interfaced to the MPIF, the VDDOPROG_M should be 3.3V. If a 2.5V device is being interfaced to the MPIF bus the VDDOPROG_M should be 2.5V

Pin Name	Type	Pin No.	Function
Ground (152 pins)			
VSS	Ground	A1 A2 A6 A10 A14 A25 A28 A31 A33 A34 AA4 AA31 AB4 AB5 AB31 AC1 AC4 AC31 AC34 AD4 AD5 AD30 AD31 AE4 AE5 AE30 AE31 AF5 AF30 AF31 AG1 AG4 AG5 AG30 AG31 AG34 AH4 AH5 AH30 AH31 AH32 AJ5	The ground pins, VSS, should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS	Ground	AJ30 AJ32 AK1 AK4 AK6 AK29 AK31 AK34 AL1 AL3 AL5 AL30 AL32 AL34 AM4 AM9 AM12 AM14 AM16 AM18 AM20 AM22 AM24 AM26 AM28 AM31 AN1 AN2 AN33 AN34 AP1 AP2 AP4 AP5 AP11 AP33 AP34	The ground pins, VSS, should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS	Ground	B1 B2 B33 B34 C4 C17 C19 C21 C23 C31 D1 D3 D5 D30 D32 D34 E1 E4 E6 E29 E31 E34 F5 F30 G4 G30 G31 H1 H4 H5 H30 H31 H34 J4 J5 J30 J31 K4 K5 K31 L4 L31	The ground pins, VSS, should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS	Ground	M1 M5 M30 M31 M34 N5 N30 N31 P31 R1 R5 R31 R34 T5 T30 T31 U1 U34 V1 V5 V30 V34 W30 W31 Y1 Y5 Y30 Y31 Y34 AN29AP29	The ground pins, VSS, should be connected to GND.
VSS	Ground	—	The ground pins, VSS, should be connected to GND.

Notes

1. All other BGA balls not listed above are NC pins.
2. All TUPP 2488 input and bi-directional pins except the RASIO™ CML links present minimum capacitive loading and operate at LVTTL and LVCMOS logic levels.
3. All TUPP 2488 I/O, excluding RASIO™ CML and programmable I/O are 2.5V but 3.3V tolerant.
4. Inputs RSTB, ALE, TMS, TDI and TRSTB have an internal pull-up resistor of 30 to 50 kOhms.
5. The VDDI, VDDOPROG_M, VDDO_PROG_E and VDDO power pins share a common ground.
6. Refer to the operations section for the recommended power supply sequencing.

10 Functional Description

This section describes the function of each entity on the TUPP 2488 block diagram.

10.1 CML Serial Interface Subsystems

This section describes the CML subsystems. There are two CML subsystems, one for the line side supporting four working and four protect links and one for the system side supporting eight working and eight protect links.

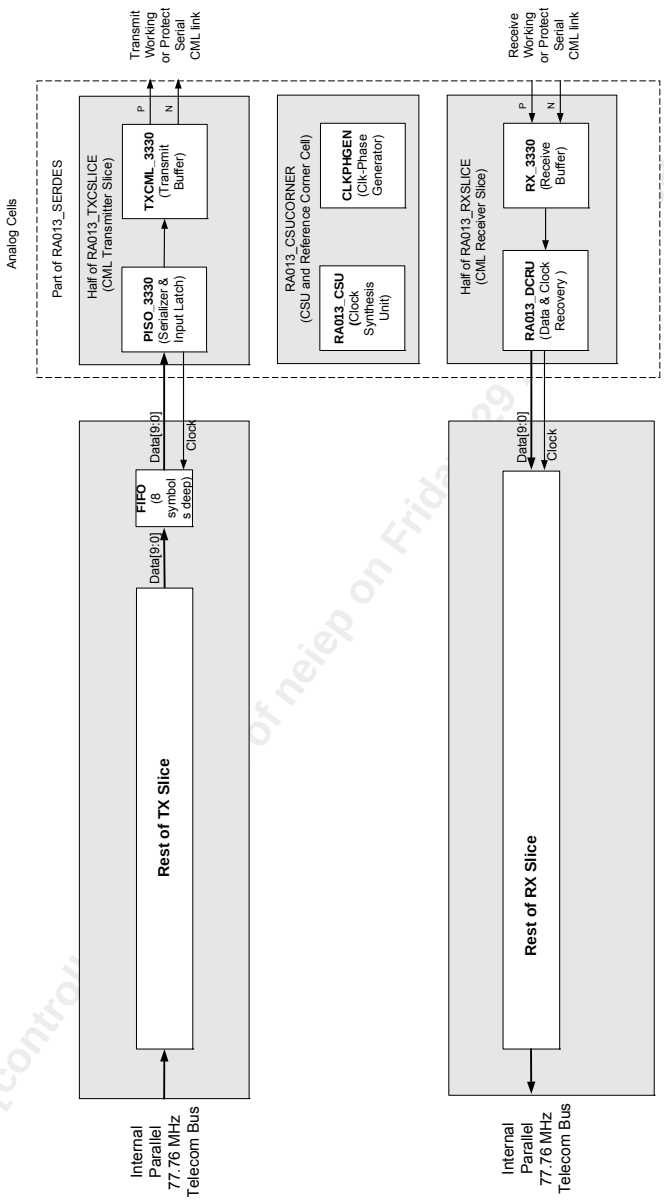
10.1.1 CML Interface Overview

RASIO™ CML voltage levels are used on the serial links of TUPP 2488. RASIO™ CML is compatible with LVDS.

Figure 12 illustrates how RASIO™ CML interface functionality is achieved in TUPP 2488. The digital blocks adapt between the internal parallel 77.76 MHz TelecomBus in TUPP 2488 and a high speed Rate Agnostic 1.2 V RASIO™ CML Serializer/Deserializer (RA013_SERDES).

Figure 12 shows the generic structure of the subsystem building blocks for the system and line side CML interfaces and their interface to the SERDES.

Figure 12 CML Subsystem Interface to SERDES



10.1.2 Rate Agnostic 1.2 V RASIO™ CML Serializer/Deserializer (RA013_SERDES)

The Rate-Agnostic 1.2 V RASIO™ CML Serializer/Deserializer (RA013_SERDES) is a high speed Serializer/Deserializer supporting a line-rate operation from 622 Mbit/s up-to 3.33 Gbit/s.

RA013_SERDES is composed of three different major analog design blocks. These are the RA013_RXSLICE which consists of the analog blocks for making two receive sides of the channel; the RA013_TXCSLICE which consists of the analog blocks for making two transmit sides of the channel and the RA013_CSUSLICE which consists of the CSU and the Clock Phase Generator. The RA013_CSUSLICE can be shared over several channels.

The line side RASIO™ CML links of TUPP 2488 can operate at a different rate than the system side RASIO™ CML links. For example, the line side RASIO™ CML links can operate at 2.488 Gbit/s while the system side RASIO™ CML links of TUPP 2488 can operate at 777.6 Mbit/s. For a 2.488 Gbit/s (or 622.08 Mbit/s) RASIO™ CML interface, the VCO inside the RA013_CSUSLICE needs generates a clock frequency of 2.488 GHz. For a 777.6 Mbit/s RASIO™ CML interface, the VCO inside the RA013_CSUSLICE generates a clock frequency of 3.111 GHz. Therefore, two separate RA013_CSUSLICE blocks are required in the TUPP 2488.

There are two RA013_SERDES blocks in TUPP 2488 — one on the line side and one on the system side. On the line side, the RA013_SERDES block contains four RA013_RXSLICE blocks, four RA013_TXCSLICE blocks, and one RA013_CSUSLICE block. On the system side, the RA013_SERDES block contains eight RA013_RXSLICE blocks, eight RA013_TXCSLICE blocks, and one RA013_CSUSLICE block. Therefore, in total there are 12 RA013_RXSLICE blocks, 12 RA013_TXCSLICE blocks, and two RA013_CSUSLICE blocks in the TUPP 2488 device.

The RA013_RXSLICE block consists of two RX_3330 blocks and two RA013_DCRU blocks to provide complete receiver side functionality for two links (i.e. working and protect).

The RA013_TXCSLICE block consists of two TX_3330 blocks and two PISO_3330 blocks to provide complete transmitter side functionality for two links (i.e. working and protect).

The RA013_CSUSLICE consists of the RA013_CSU block and the CLKPHASEGEN block.

The CSUI (CSU Interface) functional block provides a convenient interface to the RA013_CSUSLICE functions. The CSUI monitors clock synchronization between the RA013_CSUSLICE PLL divided clock and the system reference clock. The CSUI always shows that the two clocks are locked if the clocks differ by no more than 244 PPM. The CSUI always shows that the two clocks are not locked if the clocks differ by more than 1220 PPM. Any change in lock status causes the CSUI to generate a maskable interrupt.

Receive Buffer (RX_3330)

The RX_3330 block is a 3.33 Gbit/s RASIO™ CML/ELVDS receiver. Complete RASIO™ CML multi-rate configurable serial links operating at speeds up to 3.33 Gbit/s can be realized when the RX_3330 is combined with the TXCML_3330.

RX_3330 is a sensitive comparator and buffer that interfaces directly with the media and restores the amplitude of the degraded data. The RX_3330 presents a 100Ω differential termination (internally terminated) impedance to terminate the lines.

Data and Clock Recovery (RA013_DCRU)

RA013_DCRU takes in the restored amplified data from RX_3330 and recovers the phase and hence the clock and data. RA013_DCRU also deserializes the high-speed serial data to 8-bit or 10-bit low-speed parallel data and outputs it with a synchronized low speed clock.

Serializer and Input Latch (PISO_3330)

PISO_3330 is an input latch and parallel to serial converter. It samples and serializes the 8-bit or 10-bit parallel data format from the digital core to a serial data format. The PISO_3330 can output data streams at speeds up to 3.33 Gbit/s. The output data stream can then be accepted by a transmitter and transmitted over backplane.

Transmit Buffer (TXCML_3330)

TXCML_3330 is a buffer which launches the data on the transmission media with enough power to avoid degradation due to noise and limited bandwidth of the media before it reaches the receive side of the other chip.

Clock Synthesis Unit (RA013_CSU) and Clock Phase Generator (CLKPHASEGEN)

RA013_CSU along with CLKPHASEGEN generates differential clocks for use within PISO_3330, half line-rate quadrature clocks for use within RA013_DCRU, and CORECLK/CORECLKN for clocking the digital logic. RA013_CSU_CONER has to be configured for different line-rates of operation of the SERDES.

10.1.3 Line Side CML Digital Interface

The line side CML subsystem supports four links which each supports either 622 Mbit/sec scrambled SONET NRZ mode or 777 Mbit/sec 8B/10B encoded TelecomBus mode. Alternatively, one of the four links (link #1) can be run in 2.488 Gbit/sec scrambled SONET NRZ mode; in this mode the other three external links are unused. The block diagram for the links within the line side CML digital interfaces are shown in Figure 13 and Figure 14. Link#1 uses the STS-48 slices that support any of the three modes. Links #2, #3, and #4 support only the 622 Mbit/sec and 777 Mbit/sec modes using the STS-12 slice. For 2.488 Gbit/sec mode, the slices for links #2, #3, and #4 operate as slaves to link #1.

Figure 13 STS-12 CML Line Side Subsystem RX and TX Slices Block Diagram

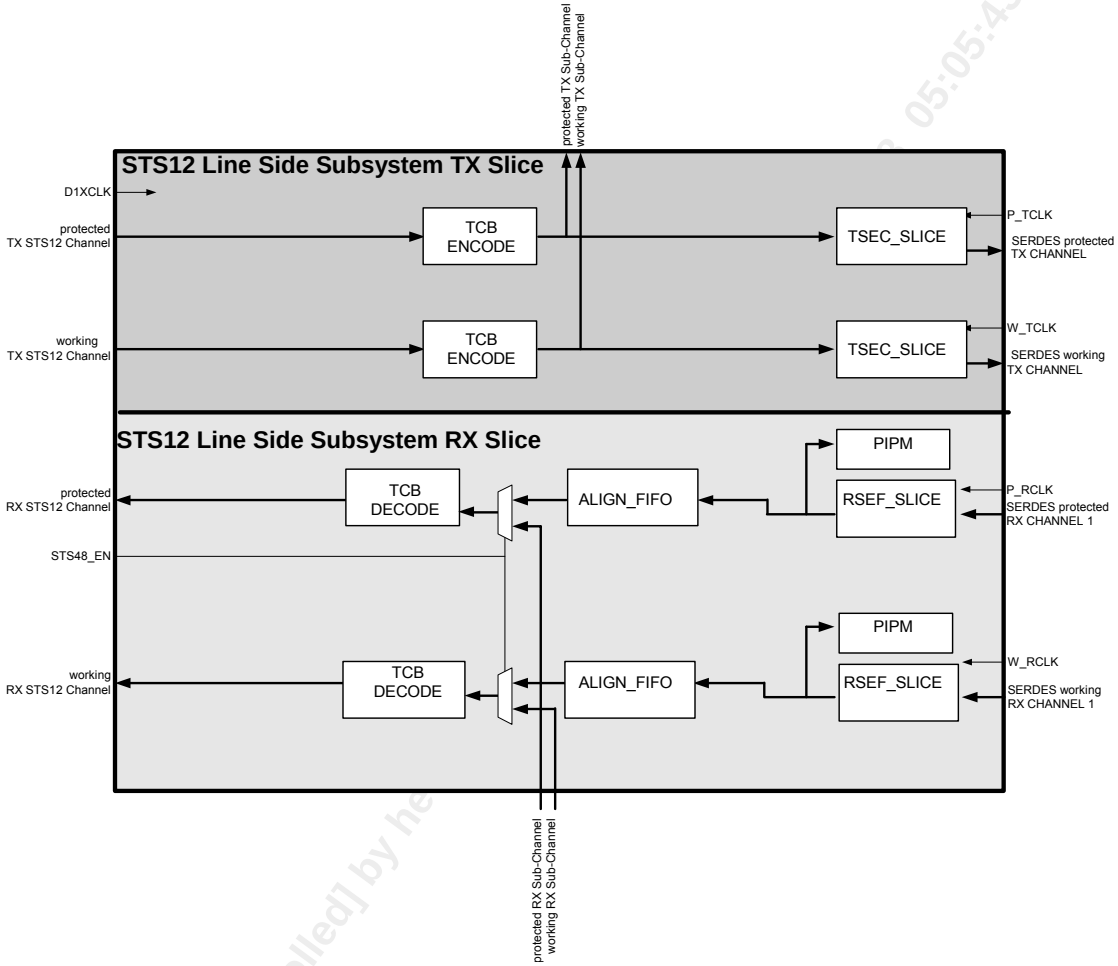
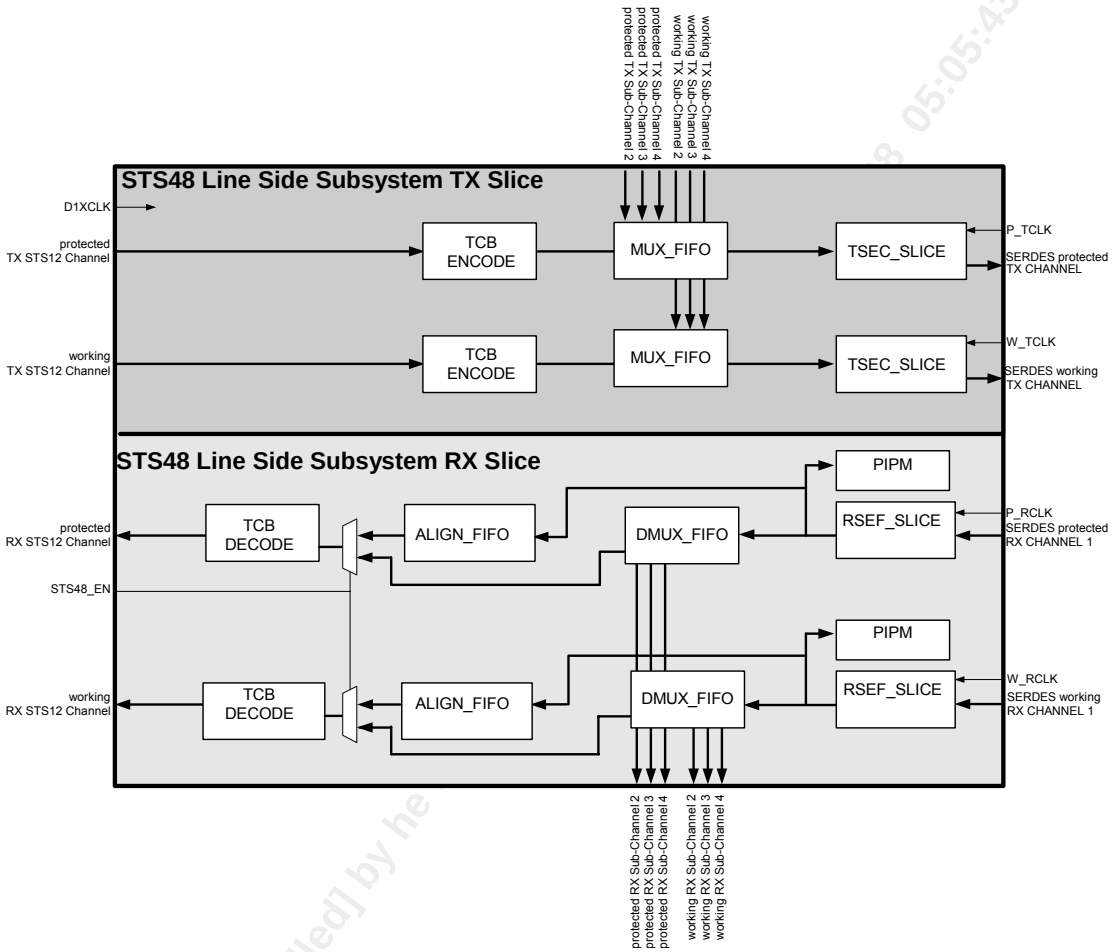


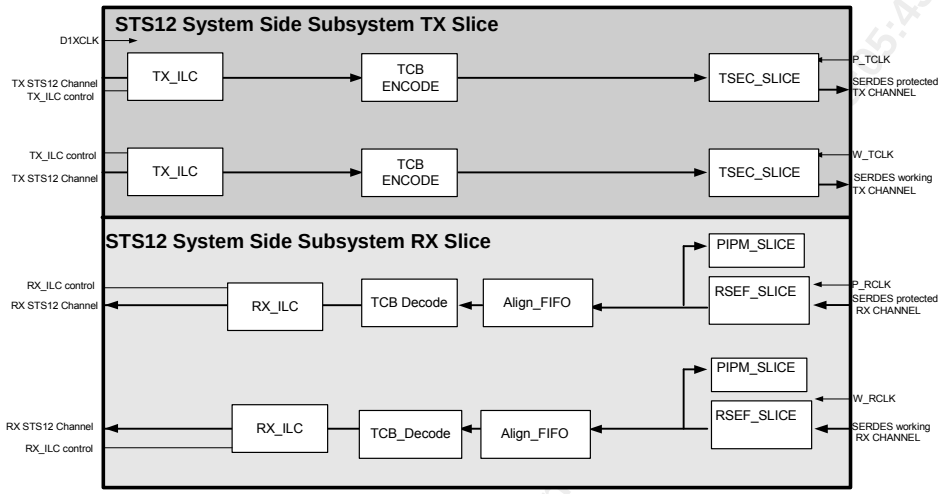
Figure 14 STS-48 CML Line Side Subsystem RX and TX Slices Block Diagram



10.1.4 System Side CML Digital Interface

The system side CML subsystem supports eight working and eight protect links which each support either 622 Mbit/sec scrambled SONET NRZ mode or 777 Mbit/sec 8B/10B encoded TelecomBus mode. The block diagram for the links within the system side CML digital interfaces is shown in Figure 15.

Figure 15 STS-12 CML System Side Subsystem RX and TX Slices Block Diagram



10.2 CML Receiver Interface Sub Blocks

The following sections describe the sub-blocks used in the CML receiver interface.

10.2.1 RSEF_SLICE Block

The RSEF_SLICE block contains the RSEF. The SERDES supplies a generated receive clock and data to the RSEF. Data from the SERDES is carried as 8-bit symbols for SONET/SDH scrambled mode or as 10-bit symbols for TelecomBus mode.

SONET/SDH Scrambled Data, 8B/10B Encoded Data Framer (RSEF)

A total of 24 RSEF blocks are instantiated in the TUPP 2488 device. There are eight RSEF blocks on the line side of TUPP 2488 for the four working and four protect Line Ingress Serial RASIO™ CML links. Likewise, there are 16 RSEF blocks on the system side of TUPP 2488 for the eight working and eight protect System Egress Serial RASIO™ CML links.

The RSEF block performs character alignment and frame alignment on a received unaligned SONET/SDH data stream. The RSEF block recovers character and frame alignment in two modes: Serial TelecomBus 8B/10B encoded data, and SONET/SDH scrambled data.

In Serial TelecomBus framing mode, the RSEF character alignment block uses the K28.5 control character (identifies the J0 byte) as a search pattern to determine correct byte alignment from the arbitrarily aligned input data. The character alignment block searches all possible input bit positions for the search pattern when in the out-of-character-alignment state. The internal byte alignment boundary is set and the character alignment block changes to the in-character-alignment state when the character alignment block finds a match to the search pattern. The character alignment block monitors line-code violations (LCV) reported by the 8B/10B decoder. The RSEF will enter the out-of-character-alignment state and begin searching for the K28.5 character if five or more line code violations are received within a 15-character window. Additionally, in this mode, the 8B/10B data stream is decoded into an internal 9-bit bus format of 8-bits data and 1-bit control (K).

In scrambled framing mode, the RSEF character alignment block transitions from the out-of-character-alignment state to the in-character-alignment state when three A1 characters followed by three A2 characters are found. The character alignment block will transition from the in-character-alignment state to the out-of-character-alignment state when the frame alignment block transitions to the out-of-frame state.

The frame alignment block synchronizes internal counters to the frame timing of the input data stream. The frame alignment block outputs an out of frame (OOF) signal that is initially asserted to indicate the RSEF is not aligned to a frame. The first character alignment will result in the frame alignment block changing to the hunt state. A single correctly aligned frame must be received before the frame alignment block de-asserts the OOF signal to indicate an in-frame condition. Similarly, receiving four improperly aligned frames when in the in-frame condition will result in the OOF signal being asserted and a return to the initial out-of-frame state. The frame alignment block processes the character alignment information whenever the frame alignment block is in the out-of-frame state. The framing block decodes the frame counters to generate the timing signals used by other blocks within the RSEF.

The 8B/10B decoder decodes according to the IEEE802.3 standard with the exception of special characters used to encode TelecomBus control signals (the line codes for positive and negative accumulated disparity of the control characters K28.5, K28.4, K28.6, K28.0, K27.7, K28.7, K29.7, K30.7, and K23.7). For these special control codes, the RSEF substitutes the decoded data with an arbitrarily defined value and sets the K control signal high. For all other characters, with the exception of characters that violate the 8B/10B line code, the RSEF outputs the decoded 8B/10B data value as defined by the IEEE802.3 specification and sets K low.

The 8B/10B decoder monitors and reports line code violations. A LCV occurs when the incoming data is not one of the valid 8B/10B characters or when the running disparity is incorrect. The TelecomBus special characters K28.0-, K28.0+, K28.4-, K28.4+, K27.7-, K27.7+, K28.7-, K28.7+, K29.7-, K29.7+, K30.7-, and K30.7+ are not considered LCVs but do affect current running disparity. A maskable interrupt is generated when a line code violation occurs. The 8B/10B decoder maintains an 8-bit count of the total number of line code violations when the 8B/10B decoder is enabled. To allow downstream blocks an opportunity to properly deal with LCVs, characters that generate a LCV are substituted with h0F and K is optionally asserted high.

The descrambler block descrambles data according to the SONET/SDH specifications with the exception of control characters output from 8B/10B decoder (K is high), which are not descrambled. The descrambler does not modify the K signal output from the 8B/10B decoder. The descrambler passes output data from the 8B/10B decoder without modification when DESCREN is asserted low.

The BIP8 block calculates the BIP8 parity on a block basis over a received frame of scrambled data and compares the result to the expected value in the B1 byte position of the next descrambled frame. The BIP8 block errors are counted when 8B/10B decoding is disabled. A maskable interrupt is generated when a BIP8 violation is detected. The BIP8 calculation is intended for monitoring SNRZ coded line data and is not valid when the 8B/10B decoder is enabled. The BIP8 interrupt should be masked and LCVs monitored for 8B/10B encoded data or for 8B/10B encoded SNRZ data.

10.2.2 Pointer Interpreter and PRBS Monitor (PIPM)

A total of 24 PIPM blocks are instantiated in the TUPP 2488 device. There are eight PIPM blocks on the line side of TUPP 2488 for the four working and four protect Line Ingress Serial RASIO™ CML links. There are 16 PIPM blocks on the system side of TUPP 2488 for the eight working and eight protect System Egress Serial RASIO™ CML links.

The PIPM provides line rate PRBS monitoring for SONET/SDH applications, and for raw bit-streams.

The PIPM receives 8-bit or 10-bit data words depending on the operating mode. In the SONET/SDH modes, 8-bit bytes are used, which can be data or control bytes. The control bytes correspond to Serial TelecomBus (STCB) control characters. A frame pulse is also required to identify the J0 byte. In the Raw mode, the PIPM can be configured for 8-bit or 10-bit data words as required.

For SONET/SDH, the PIPM supports PRBS monitoring of the STS-Nc payload capacity/C-4-Xc at the line rate: STS-12c/C-4-4c and STS-48c/C-4-16c. The STS-Nc SPE/VC-4-Xc payload is floating inside the transport frame, so the PIPM must identify the J1 position in order to locate the STS-Nc payload capacity/C-4-Xc. This can be done in two different ways depending on the type of input data: using a pointer interpreter, or using the control bytes in the data stream.

The PIPM contains a simplified pointer interpreter that identifies the J1 position in the concatenated payload and follows pointer justification events. The pointer interpreter does not implement the full specification for SONET/SDH pointer processing. Particularly, error conditions (AIS, LOP) are ignored, since it assumes that the frames containing PRBS will be correctly formatted. The fundamental operations (new pointer value during normal operation, new data flag, increment, and decrement) are fully implemented according to ANSI T1.105-1995.

When control bytes are present in the data stream, the pointer interpreter is bypassed, and the J1 position and pointer adjustments are determined from these control bytes. This mode can only be used when the data was Serial TelecomBus (STCB) encoded at the High-order Path Termination (HPT) level. If the data was scrambled, or was STCB encoded at the Multiplex Section Termination (MST) level, then the high-order path control bytes are not present.

In Raw mode, the incoming data is treated as a continuous bit sequence. Data is received in 8-bit or 10-bit words. The pointer interpreter is bypassed, and all received data is included in the PRBS monitoring. The supported data rates (8-bit/10-bit) are 622/777.6 Mbit/s and 2488 Mbit/s (8-bit).

The incoming PRBS data is tested against the $X^{23} + X^{18} + 1$ polynomial. The PRBS data is optionally inverted before being checked.

The PRBS monitoring process consists of first synchronizing the monitor with the incoming PRBS data, then generating subsequent expected PRBS words and comparing them with the incoming PRBS words. If the expected and received words are not equal, then an error has been detected in that word. This does not count bit errors since multiple bit errors in a word will be considered as a single word error. Four consecutive word errors will force the monitor out of synchronization.

Synchronization begins by loading the monitor with consecutive bits from the incoming PRBS pattern. This requires three words (23 of 24 bits, or 23 of 30 bits). If the following four expected PRBS words generated by the monitor match the incoming words, then the monitor is considered synchronized. If a mismatch occurs, then the monitor remains unsynchronized, and continues to attempt to synchronize by repeating this process with the next words in the data stream.

The PIPM will not synchronize to the input PRBS data if the data is a sequence of all 0 bits (or all 1 bits with inverted PRBS).

10.2.3 DMUX_FIFO Block

The DMUX_FIFO block is required to separate an STS-48 equivalent flow into four STS-12 equivalent flows as shown in Figure 14. It is used in the STS-48 slice only. The STS-12 slices of Figure 13 (three working and three protect) select the output of the associated working or protect DMUX_FIFO for further processing by blocks downstream of the CML slice when configured in STS-48 mode. The DMUX_FIFO decouples phase, jitter, and wander between the 77 MHz core clock and the 311 MHz recovered clock from the SERDES block.

The DEMUX_FIFO performs a simple byte de-interleave as shown in Figure 16(a). The OC-12 to OC-48 mode of the ingress STSI blocks reorders the byte de-interleaved streams to generate SDH compatible STS-12 streams as shown in Figure 16(b).

The DMUX FIFO block has four 36 word deep (4x36x9bit) FIFOs with write side logic ensuring J0 data from the RSEF is written to address 0. The read pointers will naturally wrap around to the J0 byte location as the FIF0 size divides evenly into the STS-12/STM-4 frame size.

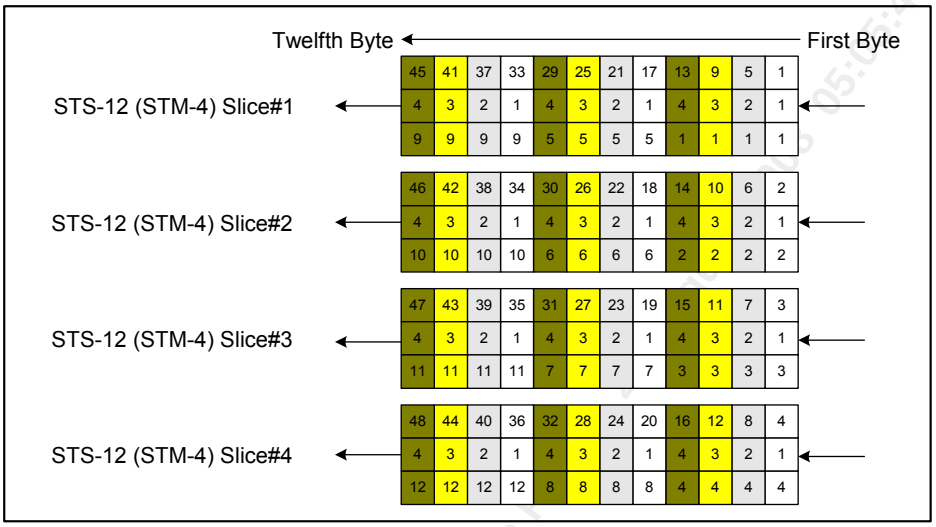
Each of the four STS-12 channel sets generated by the DMUX_FIFO are aligned to a programmable offset (LINE_INGRESS_REF_DLY) from the device frame start marker input IJ0. The offset frame start marker is referred to as RXJ0FP. The alignment distance between the receive frame pulse J0 marker generated by RSEF (indicates when the J0 character is written into address zero of the FIFO) and RXJ0FP is measured and can be read out with the DISTANCE bits in the CML Rx Slice Distance register. The offset is programmed such that the DISTANCE bits report a FIFO depth that is acceptable for accommodating receive clock jitter, and for systems containing multiple TUPP 2488 devices, skew between serial streams processed by different devices.

Loss of alignment is declared when the J0 character is not available in the DEMUX_FIFO at the expected time (coincident with RXJ0FP). The alignment failure is recorded in the CML Rx Slice INT_STATUS register. Optionally an interrupt is generated, enabled by the CML Rx Slice INT_ENABLE register.

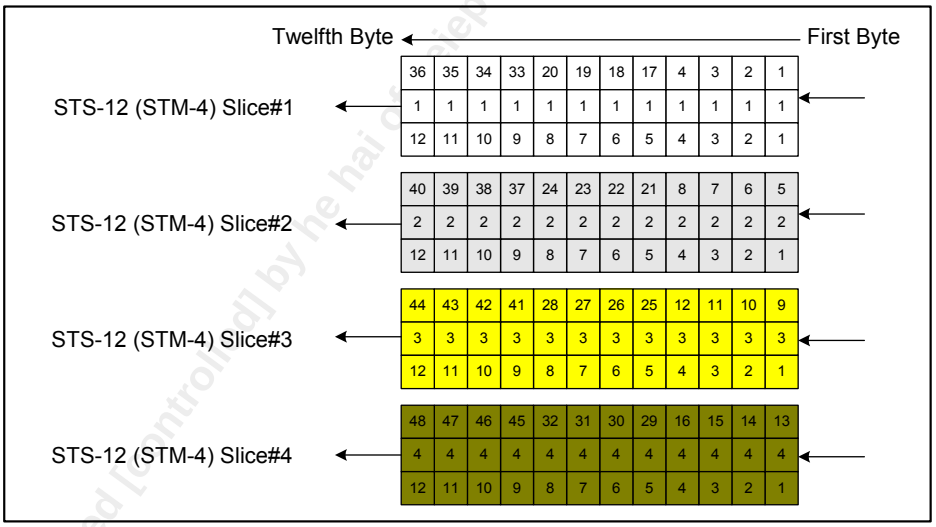
A DMUX_FIFO error is indicated and an interrupt is optionally generated whenever the read and write pointers are within 1 FIFO location of each other. The pointers continuously increment and are frequency locked so they are only compared when the write pointer wraps back to the first location in the FIFO.

Figure 16 DMUX_FIFO Operation

a) Four STS-12 (STM-4) Slices after DMUX FIFO (first 48 bytes shown)



c) Four STS-12 (STM-4) Slices after Ingress STSI



X: STS-48 (STM-16) Timeslot Number
Y: STS-12 (STM-4) Slice Number
Z: STS-12 (STM-4) Timeslot Number

10.2.4 ALIGN_FIFO Block

A STS-N equivalent flow received from a RSEF_SLICE is aligned to the external reference J0 by the ALIGN_FIFO block. A mux in the STS48 line side subsystem RX slice of Figure 14 selects either the output from the ALIGN_FIFO (STS12 mode) or the output of the DMUX_FIFO (STS48 mode).

The ALIGN_FIFO decouples phase, jitter, and wander between the 77 MHz core clock and the recovered clock from the SERDES block. The depth of the ALIGN_FIFO allows for interlink skew between the links of an interface, for example, the eight working and protect line side links.

The ALIGN_FIFO is 36 words deep (36x9bit) with write side logic ensuring J0 data appears at address 0. The read pointer will naturally wrap around to the J0 byte location as the FIF0 size divides evenly into the STS-12/STM-4 frame size. The ALIGN_FIFO processes only STS-12/STM-4 equivalent flows from the RSEF slice.

The STS-12 signal generated by the ALIGN_FIFO is aligned to a programmable offset (LINE_INGRESS_REF_DLY) from the device frame start marker input IJ0. The offset frame start marker is referred to as RXJ0FP. The alignment distance between the receive frame pulse J0 marker generated by RSEF (indicates when the J0 character is written into address zero of the FIFO) and RXJ0FP is measured and can be read out with the DISTANCE bits in the CML Rx Slice Distance register. The offset is programmed such that the DISTANCE bits report a FIFO depth that is acceptable for accommodating receive clock jitter and the skew between serial streams from the different links of an interface.

Loss of alignment is declared when the J0 pulse is not available in the ALIGN_FIFO at the expected time (coincident with RXJ0FP). The alignment failure is recorded in the CML Rx Slice INT_STATUS register. Optionally an interrupt is generated, enabled by the CML Rx Slice INT_ENABLE register.

An ALIGN_FIFO error is indicated and an interrupt is optionally generated whenever the read and write pointers are within 1 FIFO location of each other. The pointers continuously increment and are frequency locked so they are only compared when the write pointer wraps back to the first location in the FIFO.

10.2.5 TelecomBus Decoder (TCB Decoder)

A TCB Decoder block is required whenever the RSEF block is connected to the internal byte-wide 77.76 MHz TelecomBus. The TCB Decoder block decodes the 9-bit bus from RSEF (K + 8 bits data) into the byte-wide TelecomBus signals required by downstream blocks in the device.

10.2.6 Receive Inband Link Controllers (RILC)

The RILC block is used only on the system side of TUPP 2488 for the eight working and eight protect System Egress and System Ingress Serial RASIO™ CML links. The RILC block is used in the System Egress path.

The RILC block receives software messages across the system side RASIO™ CML links. The inband communication channels across system side RASIO™ CML links allow for centralized control and configuration when operating with a centralized fabric which is on a different board (e.g. external NSE family device), or when the internal crossbar is being used in a TUPP 2488 device with external SBS devices on a different board. The inband channel is full duplex. When an external NSE is used, the external NSE has active control of the link. When the internal crossbar is used, the TUPP 2488 has active control of the link.

Incoming messages are held in a FIFO in the RILC capable of holding eight messages each. Messages are read from the FIFO via the microprocessor interface. Message header bits are read through microprocessor-accessible registers. Interrupts may be generated based on status change of some received header bits. The status of message reception is reported via registers indicating the number of received messages. Interrupts can also be generated for message reception based on received message thresholds and also based upon timeout of received messages.

Interrupts can be generated by the RILC when the USER or LINK bits change state. There is no inherent flow control provided by the ILC blocks. The attached microprocessor is able to provide flow control via interrupts when the RILC inband message FIFO overflows and via the USER and Auxiliary bits in the header.

As each message arrives into the RILC, the CRC-16 and valid bit is checked; if the valid bit is not set the message is ignored and discarded, if it fails the CRC-16 check it is flagged as being in error. If the CRC-16 is OK, regardless of the valid bit, the Page, Link, User and Aux bits are passed on immediately. If the RILC FIFO erroneously overflows, an interrupt is generated.

Inband Channel

The inband channel is carried in the first 36 columns of four rows of the TelecomBus structure, rows 3, 6, 7, and 8. The overall inband channel capacity is thus 36*4*64 Kbit/s = 9.216 Mbit/s. Each 36 bytes per row allocated to the inband signaling channel is its own inband message between the end points. Four bytes of each 36-byte inband message are reserved for end-to-end control information and error protection, leaving 8.192 Mbit/s available for user data transfer between the end points.

The data transferred between the end points has no fixed format, effectively providing a clear channel for packet transfer between the attached microprocessors at each of the CML link terminating devices. Using the microprocessor interface, the user is able to send and receive any packet. Packets can be any size and any format packets are nominally up to 32 bytes in length. The first two bytes of each 36-byte message contain a header and the last two bytes of the message is a CRC-16 which detects errors in the message.

The inband channel may be used to carry out switching control changes in the internal MSU-Lite blocks in TUPP 2488 or the external SBS devices.

Inband Signaling Channel Format

The RILC block terminates two bytes of fixed header and a CRC-16 per every 32-byte inband message (total 36 bytes). The two-byte header provides control and status between devices at the ends of the CML link. The CRC-16 is calculated over the 32-byte (and two byte header) inband message and provides the terminating end the ability to detect errors in the inband message. The format of the inband header and message is shown in Table 3 and Table 4.

Table 3 Inband Signaling Channel Message Format

1 byte	1 byte	32 bytes	2 bytes
Header1	Header2	Free Format Information	CRC-16

Table 4 Inband Signaling Channel Header Format

Header1							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
VALID	LINK[1:0]		PAGE[1:0]		USER[2:0]		

Header2							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
AUX[7:0]							

Table 5 Inband Message Header Fields

Field Name	Master to Slave (External NSE/Internal CCB to Internal MSU-Lite/External SBS)	Slave to Master (Internal MSU-Lite/External SBS to External NSE/Internal CCB)
Valid	Message slot contains a message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)	Message slot contains a message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)
Link[1:0]#	These bits are optional, intended for devices which have multiple redundant links. Each bit either indicates which Link to use, Working(0) or Protect(1) when sourced from the master device, or which link is being used, when sourced from the slave device. Transmitted immediately.	These bits are optional, intended for devices which have multiple redundant links. Each bit either indicates which Link to use, Working(0) or Protect(1) when sourced from the master device, or which link is being used, when sourced from the slave device. Transmitted immediately.
Page[1:0]#	Each bit indicates which control page to use, page 1 or 0, two bits, bit 1 for the ingress MSU/MSU-Lite and bit 0 for the egress MSU/MSU-Lite. Only transmitted from the beginning of the first message of the frame	Each bit shows current control page in use, page 1 or 0, two bits, bit 1 for the ingress MSU/MSU-Lite and bit 0 for the egress MSU/MSU-Lite. Only transmitted from the beginning of the first message of the frame.
User[2:0]#	User defined register bits which may be read through the microprocessor interface. Transmitted immediately.	User defined bits. User[2:0] is sourced from top-level registers. Transmitted immediately.
Aux[7:0]#	User defined auxiliary register. Transmitted immediately.	User defined auxiliary register. Transmitted immediately.

Changes in these bits (received side) will not be processed if the received message CRC-16 indicates an error.

10.2.7 Working/Protect Selection

On the system egress side of TUPP 2488, selection between the working and protect serial RASIO™ CML links is done using the SEWSEL chip input or top-level registers. Changes in this chip input or top-level registers are synchronized to the next frame boundary.

On the line ingress side of TUPP 2488, selection between working and protect serial RASIO™ CML links is done at the output of the STSI blocks using the LIWSEL chip input or top-level registers.

10.2.8 ECBI_RX_SLICE Block

The ECBI_RX_SLICE block provides control and status for the CML receive slice.

10.3 CML Transmitter Interface Sub-blocks

The following sections describe the sub-blocks used in the CML transmitter interface.

10.3.1 Transmit Inband Link Controllers (TILC)

The TILC block is used only on the system side of TUPP 2488 for the eight working and eight protect System Egress and System Ingress Serial RASIO™ CML links. The TILC block is used in the System Ingress path.

The TILC block transmits software messages across the system side RASIO™ CML links. The inband communication channels across system side RASIO™ CML links allow for centralized control and configuration when operating with a centralized fabric which is on a different board (e.g. external NSE), or when the internal crossbar is being used in TUPP 2488 with external SBS devices on a different board. The inband channel is full duplex. When an external NSE is used, the external NSE has active control of the link. When the internal crossbar is used, the TUPP 2488 has active control of the link.

Outgoing messages are held in a FIFO in the TILC capable of holding eight messages each. Messages are written to the FIFO via the microprocessor interface. Message header bits are written through microprocessor-accessible registers. The status of message transmission is reported via registers indicating the number of messages queued for transmission.

Further details on the Inband Link messaging is given in Section 10.2.6.

10.3.2 TelecomBus Encoder (TCB Encoder)

A TCB Encoder block is required whenever the internal byte-wide 77.76 MHz TelecomBus is connected to a TSEC block. The TCB Encoder block encodes the byte-wide TelecomBus signals into the form of a control signal (K) and an 8-bit data bus which contains special control characters which are marked by K. Table 6 shows how the serial TelecomBus character encoding is done.

Table 6 Serial TelecomBus Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Level			
K28.5	001111 1010	110000 0101	J0 = ‘b1 PL= ‘b0 J0 frame and multiframe alignment
K28.4	001111 0010	—	High-order path AIS
High Order Path Termination (HPT) Mode			
K28.5	001111 1010	110000 0101	J0=’b1 PL=’b0 J0 frame and multiframe alignment
K28.4	001111 0010	—	High-order path AIS
K28.0-	001111 0100	—	PL=’b0 High-order path H3 byte position, no negative justification event.
K28.0+	—	110000 1011	PL=’b0 High-order path PSO byte position, positive justification event.
K28.6	001111 0110	110000 1001	J1=’b1, PL=’b1 High-order path frame alignment (J1).

10.3.3 MUX_FIFO Block

The MUX_FIFO block converts four STS-12 flows to a single STS-48 equivalent flow. Figure 16 shows the flow but in reverse order. It is used in the STS-48 slice only. The egress STSI block shall be set in OC-48 to OC-12 mode. It is not used when the STS-48 block is used in either of the STS-12 modes.

When transmitting in STS-48 mode the four STS-12 equivalent flows received synchronous to 77MHz REFCLK are interleaved from channel 1 to channel #4. This generates an output flow synchronous to the SERDES generated 311MHz clock (four times faster than 77MHz). The J0 marker received for the STS-12 equivalent input flow is retimed and marks the J0 position of channel 1 in the STS-48 equivalent output flow.

10.3.4 TSEC_SLICE Block

The TSEC_SLICE block contains the TSEC functional block followed by a timing FIFO. The FIFO decouples phase, jitter and wander between the core clock, which clocks data into the FIFO from the TSEC, and the SERDES generated transmit clock, which clocks data out of the FIFO into the SERDES.

Transmit Data Scrambler 8B/10B Encoder (TSEC)

The TSEC operates in either Serial TelecomBus mode or in SONET scrambled mode.

When operating in Serial TelecomBus mode, the TSEC converts the 8-bit data parallel input data and the associated control bit to the 8B/10B Serial TelecomBus 10-bit parallel data format.

If configured for emission of scrambled data, the TSEC applies SONET/SDH scrambling to the data stream.

The TSEC can be configured to overwrite the data stream with a pseudo random bit sequence (PRBS) either as a raw stream or with the PRBS within a SONET concatenated SPE, excluding the path overhead and fixed stuff bytes of the SPE. The TSEC supports PRBS generation of only concatenated SONET/SDH streams at the line rate: STS-12c, STS-48c. The PRBS polynomial used is $x^{23}+x^{18}+1$.

The STS48 Line Side Subsystem TX Slice contains two TSEC blocks, one that operates when the block is configured for STS12 operation and one that operates when the slice is configured for STS48 operation. The TSEC block addressed is dependent on the STS48_EN bit setting in the CML Control Register. Configure the STS48_EN bit prior to programming the TSEC block.

Timing FIFO Block (TIM_FIFO)

The TIM_FIFO block consists of an 8*10-bit FIFO. The transmit data from the TSEC is written to the FIFO synchronous to the 77 MHz core reference clock when in STS12 mode and a 311 MHz reference clock derived from the transmit PISO block when in STS48 mode. The FIFO is read synchronous to the transmit PISO clock.

The timing FIFO write address is initialized with four while the read address is initialized with zero. The CENTER bit of the CML TX Slice Config register resets the FIFO write and read addresses to there initial value. The CENTER register bits are self-clearing, so that a number of clock cycles after a bit has been set, the CENTER operation will complete, and the bit will be reset automatically.

A FIFO underrun or overrun is monitored and flagged via status bits in the CML TX Slice INT_STATUS register. An interrupt is optionally generated depending on the state of the interrupt enable bits of the CML TX Slice Control register.

10.3.5 ECBI_TX_SLICE Block

The ECBI_TX_SLICE block provides control and status for the RASIO™ CML transmit slice.

10.4 SONET/SDH Time Slot Interchange (STSI)

The line ingress interface of TUPP 2488 contains two STSI blocks – one for the Line Ingress Serial RASIO™ CML working links and one for the Line Ingress Serial RASIO™ CML protect links. The STSI for the working links is also shared with the Ingress Byte-Wide TelecomBus Interface.

Similarly, the line egress interface of TUPP 2488 contains two STSI blocks – one for the Line Egress Serial RASIO™ CML working links and one for the Line Egress Serial RASIO™ CML protect links. The STSI for the working links is also shared with the Egress Byte-Wide Telecom Bus Interface.

When the Line Ingress interface selected is Ingress Byte-Wide TelecomBus, only one of the STSI blocks in the Line Ingress path is used. When the Line Ingress format selected is Serial CML, both STSI blocks in the Line Ingress path are used. Similarly, only one of the STSI blocks in the Line Egress path is used when the Line Egress interface selected is Byte-Wide TelecomBus.

The STSI blocks can form the "Time" stage of a Time:Space:Time switch fabric in conjunction with external TSE and TBS devices. The STSI blocks effectively function as a TBS device.

The STSI is used to reorder the timeslots inside a SONET/SDH data stream. The timeslots can be reordered at an STS-1/STM-0 granularity. Any STS-1/STM-0 can be dropped, moved or copied to one or more STS-1/STM-0 data streams inside a SONET/SDH data stream.

The STSI reorders the timeslots of four STS-12/STM-4 parallel format data streams. The four data streams are required to be aligned on the same transport frame. This permits the STSI to reorder the timeslots both within and across the four SONET/SDH data streams.

The STSI uses two connection memory pages. Either of the two pages specifies the re-ordering operations to be performed on the data streams. In normal operation, one of the pages is active, containing the information used to reorder the current data stream. The other page can be updated by an external microprocessor in the background. When a connection memory change is indicated, the two pages are swapped and the most recently updated page becomes the active page. Page selection is done using the LICMP pin on the line ingress interface and the LECMP pin on the line egress interface or using top-level registers. The change of page selection is aligned to the second next transport frame boundary to provide hitless switchover.

The LICMP pin is sampled on the IJ0 reference pulse when using the Line serial bus. A programmable delay value in top-level registers specifies when the ingress STSI blocks expect to see a J0 in relation to the IJ0 reference pulse. Glue logic is used to wait for this programmable delay before updating the CMP input to the ingress STSI blocks. Similarly, the LECMP pin is sampled on the IJ0 reference pulse, and a programmable delay is used before updating the CMP input to the egress STSI blocks.

When using Parallel bus, CMPs are sampled on IJ0J1 and EJ0J1for the Ingress and Egress STSIs respectively.

The re-ordering of the input STS-1/STM-0 payload is based on the output STS-1/STM-0 payload. Each output STS-1/STM-0 time slot is associated with one input STS-1/STM-0 time slot.

The STSI can be set in a bypass mode by programming passthru switch settings. The STSI can also operate in an OC-48c to OC-12 translation mode, or OC-12 to OC-48c translation mode. In the translation modes, the connection memory pages are not used.

The LIWTSEN outputs on the working STSI block in the line ingress interface can be used to control multiplexers which select combinations of STS-1's from both working and protect Line Ingress Serial RASIO™ CML links. Changes to the selection of working and protect links are synchronized to the frame boundary to provide hitless switchover.

Selection between working and protect links on the Line Ingress Serial RASIO™ CML links can also be configured using the LIWSEL chip input pin. Changes in LIWSEL are also synchronized to the second next frame boundary to provide hitless switchover. A top-level register bit controls whether working/protect selection is done using the LIWTSEN outputs on the STSI block or using the LIWSEL chip input.

When the Ingress Byte-Wide TelecomBus is used instead of the Line Ingress Serial RASIO™ CML links, then no working/protect selection is performed. Traffic from the STSI block used by the Ingress Byte Wide TelecomBus is always selected.

10.5 High Order Path Overhead Subsystem

The High Order Path Overhead Subsystem is a complete communications subsystem that can be realized as part of a single high-performance integrated circuit. The High Order Path Overhead Subsystem terminates the path overhead of any legal mix of STS-1/3c/12c/48c (VC-3/4/4-4c/4-16c) payloads in a SONET/SDH STS-48/STM-16 stream. This subsystem is composed of four RTTP blocks, four RHPP_R blocks, one SARC-48 block, four THPP_R blocks, and four TTTP blocks.

In the receive direction, the High Order Path Overhead Subsystem detects path alarm conditions and detects and accumulates path BIPs (B3). It extracts Remote Error Indications (REIs) from path status (G1), and monitors and accumulates path Remote Error Indications (REIs) for performance monitoring. It accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result. It extracts the received path payload label (C2). All path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead if desired.

In the transmit direction, the High Order Path Overhead Subsystem creates and inserts the path BIPs (B3), optionally inserts a 16 or 64 byte path trace (J1) message, optionally inserts the path status byte (G1) and the path payload label (C2) byte into the transmit stream. In addition to its basic processing of the transmit SONET/SDH path overhead, the High Order Path Overhead Subsystem provides convenient access to all path overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of path overhead if desired. The High Order Path Overhead Subsystem also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, pointer errors and BIP errors, which are useful for system diagnostics and tester applications.

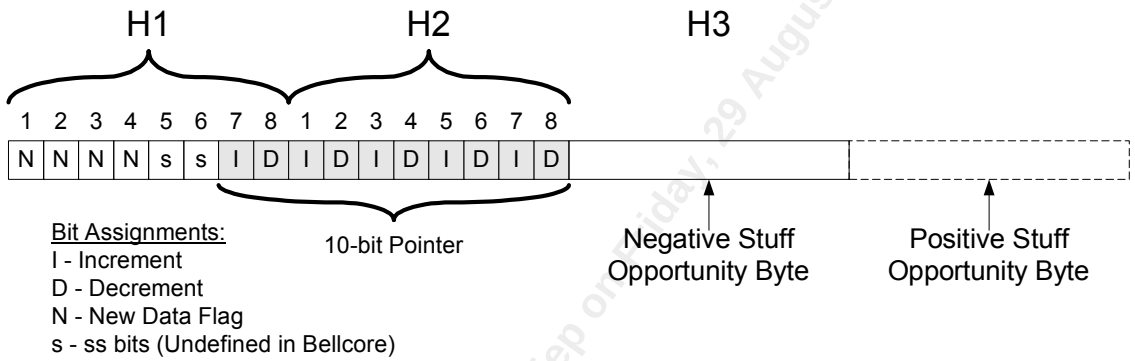
10.5.1 Receive High Order Path Processor (RHPP_R)

The Receive High Order Path Processor (RHPP_R) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

Pointer Interpreter

The function of the pointer interpreter is to extract and validate the pointer from the H1/H2 bytes in order to identify the location of the path trace byte (J1) and all the synchronous payload envelop (SPE) bytes of the constituent STS (VC) payloads. The pointer interpreter is a time-multiplexed finite state machine that can process any legal mix of STS-1/3c/12c (AU3/4/4-4c) pointers. The H1 and H2 bytes can be viewed as one word as shown in Figure 17.

Figure 17 Payload Pointers (H1, H2) Coding

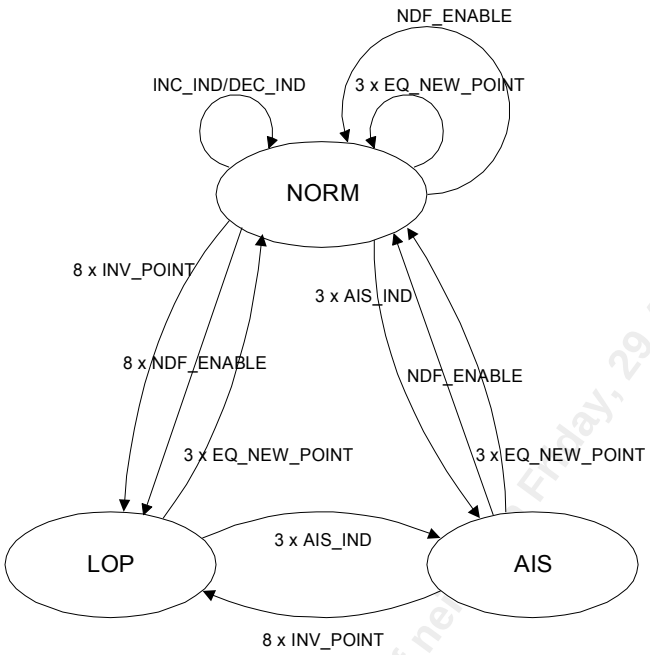


Within the pointer interpretation algorithm 3 states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

The transitions between the states will be consecutive events (indications), for example, 3 consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving an NDF enabled with a valid pointer value. It is implied that since the algorithm only contains transitions based on consecutive indications, non-consecutively received invalid indications do not activate the transitions to the LOP_state for example.

Figure 18 Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT: Disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: Enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: (H1 = FFh) + (H2 = FFh).

INC_IND: Disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + no previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

DEC_IND: Disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + no previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

INV_POINT: Not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: Disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
2. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100 and 0111.
4. The remaining 6 NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.
5. The ss bits are unspecified in SONET and have bit pattern 10 in SDH.
6. The use of ss bits in definition of indications may be optionally disabled with the SSEN register bit.
7. The requirement for previous NDF_ENABLE, INC_IND, or DEC_IND to be more than 3 frames ago may be optionally disabled with the JUST3DIS register bit.
8. NEW_POINT is also an INV_POINT.
9. The requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: Offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: 3 consecutive equal NEW_POINT indications

NDF_ENABLE: Single NDF_ENABLE indication

3 x AIS_IND: 3 consecutive AIS indications

8 x INV_POINT: Eight consecutive INV_POINT indications

8 x NDF_ENABLE: Eight consecutive NDF_ENABLE indications

Notes

1. The transition from NORM_state to NORM_state does not represent state changes but imply offset changes.
2. 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.
3. All 3 offset values received in 3 x EQ_NEW_POINT must be identical.
4. "Consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter). INV_POINT counter can be reset after 3 EQ_NEW_POINT optionally with the INVCNT register bit. INC_IND or DEC_IND may not reset the EQ_NEW_POINT counter.
5. The number of “consecutive AIS indications” required to transition to the AIS state is programmable with the RELAYAIS register bit. (1 or 3)

The pointer interpreter state machine detects path loss of pointer (LOP-P) defect and path alarm indication signal (AIS-P) defect. A LOP-P defect is declared when the pointer state machine enters the LOP_state and a LOP-P defect is removed when it exits the LOP_state. An AIS-P defect is declared when the pointer state machine enters the AIS_state and an AIS-P defect is removed when it exits the AIS_state.

Concatenation Pointer Interpreter State Machine

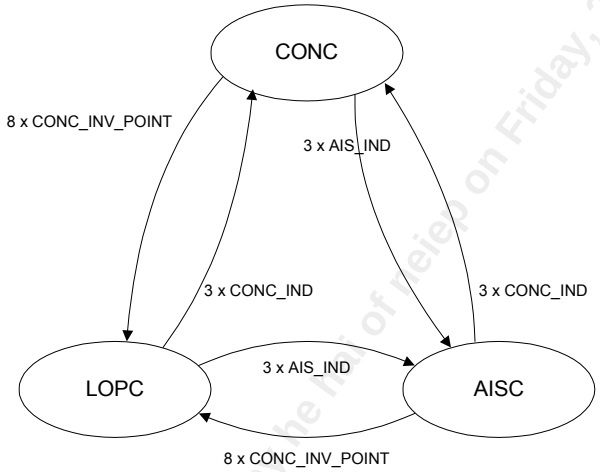
The function of the concatenation pointer interpreter is to extract and validate the concatenation pointer from the H1/H2 bytes. The concatenation pointer interpreter is a time-multiplexed finite state machine that can process any legal mix of STS-3c/12c (AU4/4-4c) concatenation pointers.

Within the concatenation pointer interpretation algorithm 3 states are defined as shown below:

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), for example, 3 consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER.

Figure 19 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

CONC_IND: Enabled NDF + dd + "1111111111"

AIS_IND: (H1 = FFh) + (H2 = FFh)

CONC_INV_POINT: Not any of the above (i.e.: not CONC_IND and not AIS_IND)

Notes

1. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, and 1000.
2. The remaining 11 NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, and 1111) result in an INV_POINT indication.
3. The dd bits are unspecified in SONET and SDH.

The transitions indicated in the state diagram are defined as follows:

3 X CONC_IND: 3 consecutive CONC indications

3 x AIS_IND: 3 consecutive AIS indications

8 x CONC_INV_POINT: 8 consecutive INV_POINT indications

Notes

1. "Consecutive event counters" are reset to zero on a change of state.
2. The number of “consecutive AIS indications” required to transition to the AIS state is programmable with the RELAYAIS register bit (1 or 3).

The concatenation pointer interpreter state machine detects path loss of pointer concatenation (LOPC-P) defects, path concatenation alarm indication signal (AISC-P) defects, and all path concatenation alarm indication signal (ALLAISC-P) defects. A LOPC-P defect is declared when any of the concatenation pointer interpreter state machine, processing the same concatenated payload, enters the LOPC_state. A LOPC-P defect is removed when all the concatenation pointer interpreter state machine, processing the same concatenated payload, exits the LOPC_state. An AISC-P defect is declared when any of the concatenation pointer interpreter state machine, processing the same concatenated payload, enters the AISC_state. An AISC-P defect is removed when all the concatenation pointer interpreter state machine, processing the same concatenated payload, exits the AISC_state. An ALLAISC-P defect is declared when all the concatenation pointer interpreter state machine, processing the same concatenated payload, enters the AISC_state. An ALLAISC-P defect is removed when any of the concatenation pointer interpreter state machine, processing the same concatenated payload, exits the AISC_state.

Error Monitoring

The RHPP_R calculates the path BIP-8 error detection codes on the STS-1/3c/12c/48c (VC-3/4/4-4c/4-16c) payloads. When processing a VC-3 payload, the two fixed stuff columns can be excluded of the BIP-8 calculation if the FSBIPDIS register bit is set. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of each constituent STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP_R accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP_R extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block block REI errors can be accumulated.

The RHPP_R monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP_R also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP_R also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 7. PLM-P is removed when the accepted PSL match the expected PSL according to Table 7. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP_R also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP_R also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. PPDI is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 8 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 7 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	=$_{exp}$PDI	Mismatch	Inactive	Active
				!=$_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	=$_{exp}$PDI	Match	Inactive	Active
				!=$_{exp}$PDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	= $_{exp}$PSL	Match	Inactive	Inactive
				!=$_{exp}$PSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	=$_{exp}$PDI	Match	Inactive	Active
				!=$_{exp}$PDI	Mismatch	Inactive	Inactive

Table 8 Expected PDI Defect Based On PDI and PDI Range Values

PDI Register Value	PDI Range Register Value	Exp PDI	PDI Register Value	PDI Range Register Value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6

PDI Register Value	PDI Range Register Value	Exp PDI	PDI Register Value	PDI Range Register Value	Exp PDI
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP_R monitors bits 5, 6 and 7 of the path status byte (G1) to detect to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

The RHPP_R extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4 and N1). RPOHCLK is the generated output clock used to provide timing for the RPOH port. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RPOHFP high with the rising edge of RPOHCLK identifies the MSB of the first J1 byte.

10.5.2 Receive Trail trace Processor (RTTP)

The RTTP can be configured to monitor the trail trace messages inside an STS-12/STM-4 8-bit serial stream at 77.76 MHz. The RTTP monitors up to 12 independent path trace messages.

Three trail trace algorithms are defined to detect trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Algorithm 1 is Telcordia compliant. This algorithm detects TIM on a 16 or 64 bytes trail trace message. Algorithm 2 is ITU compliant. This algorithm detects TIU and TIM on a 16 or 64 bytes trail trace message. Algorithm 3 is not Telcordia or ITU compliant. It detects TIU on a single continuous trail trace byte.

Trail trace Algorithm 1

This algorithm captures, synchronizes, and validates the trail trace message.

The current trail trace message is stored in the captured page. Each message can be configured to synchronize when receiving either a byte with its MSB high, or on the CR/LF (CR = 0Dh, LF = 0Ah) ASCII characters of the message. If the RTTP synchronizes on the MSB of the message, the byte with its MSB set high is placed in the first location (position 0) of the captured page. If the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message, the LF sync byte is placed at the last location of the message (position 15 or 63), and the following byte is placed in the first location (position 0) of the captured page.

A match trail trace message is declared when 16 of the last 20 messages match the expected message. A mismatch trail trace message is declared when none of the last 20 messages matches the expected message. The expected trail trace message is a static message written in the expected page by an external microprocessor.

Trail trace Algorithm 2

This algorithm captures, synchronizes, monitors persistency, monitors stability, and validates the trail trace message.

The current trail trace message is stored in the captured page. Each message can be configured to synchronize when receiving either a byte with its MSB high, or on the CR/LF (CR = 0Dh, LF = 0Ah) ASCII characters of the message. If the RTTP synchronizes on the MSB of the message, the byte with its MSB set high is placed in the first location (position 0) of the captured page. If the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message, the LF sync byte is placed at the last location of the message (position 15 or 63), and the following byte is placed in the first location (position 0) of the captured page.

A persistent trail trace message is declared when an identical message is received for 3 or 5 consecutive messages (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page.

A stable trail trace message is declared when a persistent message is received. An unstable trail trace message is declared when one or more erroneous bytes are detected between the current message and the previous message in a total of eight trail trace messages without any persistent message in between.

A match trail trace message is declared when the accepted message matches the expected message. A mismatch trail trace message is declared when the accepted message does not match the expected message. The expected message is a static message written in the expected page by an external microprocessor.

Trail trace Algorithm 3

This algorithm only monitors stability on the trail trace byte.

A stable trail trace byte is declared when an identical byte is received for 48 consecutive frames. An unstable trail trace byte is declared when one or more erroneous bytes are detected in three consecutive 16 byte windows. The first window starts on the first erroneous byte.

The RTTP provides an interrupt output to indicate any change in the status of section/path trace identifier unstable (TIU) and section/path trace identifier mismatch (TIM). An internal register can be read to identify the interrupt source. Each interrupt source is individually maskable.

Note: The RTTP algorithm for Trace Identifier Mismatch (TIM) detection is not compliant with the new R6-160 recommendation put forth in the 2000 issue of Telcordia's GR-253. R6-160 states 'A change in the phase of an incoming STS path trace string shall cause the STS PTE to consider, at most, one sample to be mismatched for the purposes of detecting and terminating TIM-P defects.'

The RTTP algorithm complies with this if the phase change happens to drop one or more bytes. However, the algorithm is non-compliant if the phase change happens to repeat one or more bytes. Instead, the RTTP will count a message longer than the expected length as two mismatched samples.

10.5.3 Transmit High Order Path Processor (THPP_R)

The THPP_R processes the SONET path or SDH high order path of an STS-12/STM-4 8-bit serial stream at 77.76 MHz. Four THPP_R's are used to process an STS-48/STM-16 32-bit parallel stream at 77.76 MHz. The THPP_R is used to optionally insert the POH bytes and fixed stuff bytes.

The THPP_R can insert the path overhead of any combinations of STS-1/3c/12c or VC-3/4/4-4c payloads of an STS-12/STM-4 stream. The path overhead bytes can be inserted serially in the THPP_R. They can also be extracted from the register set and inserted in the outgoing byte stream. Path overhead byte insertion may be optionally disabled for specific bytes by toggling the THPP_R PAIS input, to indicate that the overhead byte is already in the incoming byte stream. The THPP_R generates the HTPOHRDY portion of the EV5_HTPOHRDY pin output.

The THPP_R calculates and inserts the path BIP-8 (B3) byte for each constituent SPE/VC-n payload of the input stream. An externally generated BIP-8 code can be combined with the calculated BIP-8 code to support the processing of STS-48c/STM-16c frames, or possibly higher bandwidth concatenated frames. The values shifted in on the path overhead serial input stream during the B3 byte position may be used as an error mask. The H4 read from the serial POH input may also be used as an error mask. These values may be exclusive OR'ed with the calculated B3 value and the H4 byte in the incoming stream to selectively corrupt one or more bits in the resulting stream. It is also possible to invert all the B3 bits, or all the H4 bits via register bits.

There are several possible sources for the path status byte G1. The source of the P-REI and P-RDI bits inserted in the outgoing STS path status byte (G1) may be the inputs PREI[2:0] and PRDI[3:0] from the SARC-48, an internal register of the THPP_R or a valid G1 might already be encoded in the input byte stream. Refer to the description of the THPP_R Source and Pointer Control Register in the register document[**Error! Reference source not found.**] for a table that describes the overhead insertion priority given multiple sources for each path overhead byte.

10.5.4 Transmit Trail trace Processor (TTTP)

The TTTP can be configured to generate the trail trace messages inside an STS-12/STM-4 8-bit serial stream at 77.76 MHz. Each TTTP can generate up to 12 independent path trace messages. The THPP_R selects the TTTP as the source for the trail trace message if the PTBJ1 bit of the THPP_R Source and Pointer Control Register is a logic 1.

The TTTP can be configured to generate a 1-byte, 16-byte, or 64-byte trail trace message. The message is inserted in the path trace byte (J1) over multiple frames. The trail trace message is stored in an internal RAM and must be written by an external microprocessor. The trail trace message must include synchronization because the TTTP does not add synchronization to the message.

The TTTP can force a trail trace message to all zeros to avoid generating an unstable/mismatch message while the microprocessor updates the internal RAM.

10.5.5 SONET/SDH Alarm Reporting Controller 48 Streams (SARC-48)

The SARC-48 receives all the path defects detected by the receive overhead processor (RHPP_R) and, according to user specific configuration, generates consequent action indications. Configuration registers PAISPTRCFG[1:0] allow the user to select receive AIS-P defect coming from different combinations of PAIS, PAISC and ALLPAISC signals.

Configuration registers PLOPTRCFG[1:0] and PLOPTREND allow the user to select receive LOP-P defect coming from different combinations of PLOP, PLOPC, PAIS, and PAISC signals. Also others configuration registers allow terminating receive LOP-P defect when a receive AIS-P defect is present.

Receive path alarm (HRALM) indication is asserted when an AIS-P, LOP-P, PLU-P, PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P, or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to independently enable any defect from the previous enumeration.

Receive path alarm insertion (RPAISINS[4:1]) indication RPAISINS is asserted when an AIS-P, LOP-P, PLU-P, PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P, or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to independently enable any defect from the previous enumeration.

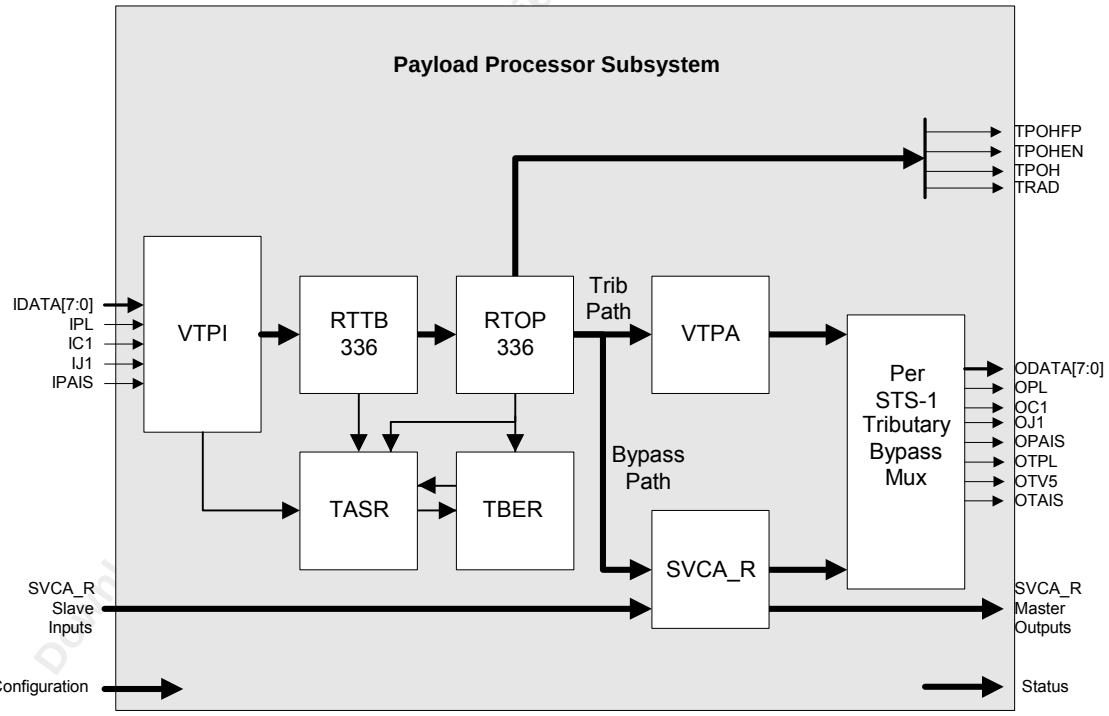
Remote path ERDI insertion indication TPERDIINS[2:0] is updated when an AIS-P, LOP-P, PLU-P, PLM-P, TIU-P, TIM-P, or UNEQ-P defect is detected in the receive data stream and output via the THPP_R.

10.6 Payload Processor Subsystem

There are four instances of the Payload Processor Subsystem in TUPP 2488 — one per STS-12/STM-4 slice. Each Payload Processor subsystem contains one VTPI, one RTTB336, one RTOP336, one VTPA, one SVCA_R, one TASR, one TBER and other control logic.

Figure 20 illustrates the tributary and bypass paths in the Payload Processor Subsystem (PP Subsystem). The Payload Processor Subsystem processes a SONET/SDH STS-12/STM-4 data stream. The STM-4/STS-12 frames may consist of SONET/SDH bypass traffic with no VT/TU's, contiguous concatenated payloads, SONET/SDH traffic with VT/TU's, or any legal mixture of all these types of traffic. Bypass traffic and contiguous concatenated payloads are processed in the Bypass path. VT/TU traffic is processed in the Tributary path. The Payload Processor can perform AU3 to AU4 conversion and AU4 to AU3 conversion.

Figure 20 Tributary and Bypass Paths



Both paths receive all types of traffic. However, only the bypass path will output valid bypass traffic and only the tributary path will output valid tributary data.

The VTPA can be disabled on an STM-0/STS-1 basis for bypass traffic and contiguous concatenated payloads to suppress extraneous interrupts. The Tributary-Bypass Mux is programmable to select the desired STM-0/STS-1 streams from either path. See the Operation Section (Section 13) for more details.

10.6.1 Tributary Path

The Tributary path runs through the VTPI, RTTB336, and RTOP336 before passing through the VTPA and terminates at the input to the Tributary-Bypass Mux. The Tributary path is configurable to handle the frame structures shown in Figure 21 and Figure 22.

Figure 21 Supported SDH Frame Structures in Tributary Path

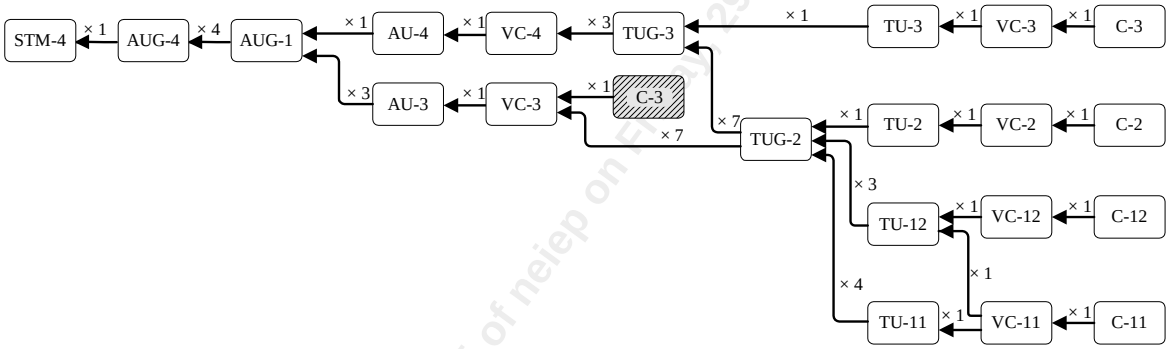
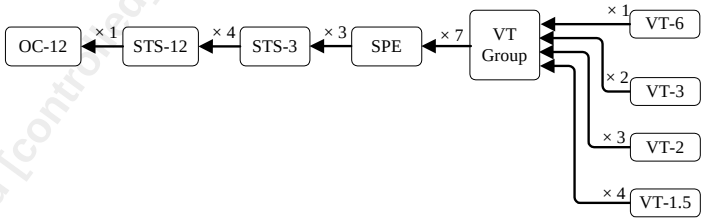


Figure 22 Supported SONET Frame Structures in Tributary Path



Notes

1. The Tributary path does not support contiguously concatenated payloads.
2. In SDH, an AU3/VC3/C3 payload may be input to the Tributary path, but the tributary path will convert this to an AU4/VC4/TUG3/TU3/VC3/C3 before outputting it.
3. Frames may consist of any legal mix of the above payloads.

The Tributary path interprets VT/TU pointers. It processes the tributary trace message within the path trace byte of the virtual tributaries, processes the tributary path overhead bytes of the tributaries and extracts the tributary path overhead bytes into a serial stream. It generates the tributary payload pointers for the outgoing STM-4/STS-12 data stream, and aligns the outgoing tributary multiframe to an equipment reference.

The Tributary path translates incoming pointer justifications in high order payloads (STS-1, AU4, AU3) to pointer justifications in low order payloads (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, or TU11), resulting in all VT/TUs being located in fixed columns of the transport frame.

It provides software configurable offset between the payload frame boundaries (J1) and the H3 byte of the transport overhead (High Order H1, H2 pointer value = 0 or 522). It aligns the synchronous payloads of a SONET/SDH STS-48/STM-16 or four STS-12/STM-4 byte serial streams to a new transport frame reference (J0). It inserts valid high order pointer bytes (H1, H2), framing bytes (A1, A2).

The VTPI, RTTB336, RTOP336, and VTPA interrupts can be disabled on an STM-0/STS-1 basis for bypass traffic to suppress extraneous interrupts.

The Tributary path can optionally perform the AU3 to AU4 and AU4 to AU3 conversions shown in Table 9.

Table 9 Tributary Path AU3/AU4 Conversions

Incoming Payload	Outgoing Payload	Outgoing VC4 Path Overhead	Outgoing VC3 Path Overhead
AU4/VC4/TUG3/TUG2	AU3/VC3/TUG2	N/A	All zero(*)
AU3/VC3/TUG2	AU4/VC4/TUG3/TUG2	All zeros(*)	N/A
AU3/VC3/C3	AU4/VC4/TUG3/TU3/VC3/C3	All zeros(*)	Same as Incoming VC3 Path Overhead

(*) Except H4, which will always be generated.

Notes

- The TUG2s each contain TU2, TU11 or TU12 tributaries units.

The outgoing tributary multiframe alignment (H4) from the VTPA is controlled by the OTMF input to the Payload Processor block. OTMF is generated from the EJ0 input to the TUPP 2488.

10.6.2 Bypass Path

The Bypass path runs through the VTPI, RTOP336, RTTB336, and SVCA_R and terminates at the input to the Tributary-Bypass Mux. The Bypass path processes any mix of non-VT/TU mapped payloads, including contiguous concatenation frame structures. The full range of frame structures supported by the Bypass Path is shown in Figure 23 and Figure 24.

Figure 23 Supported SDH Frame Structures in Bypass Path

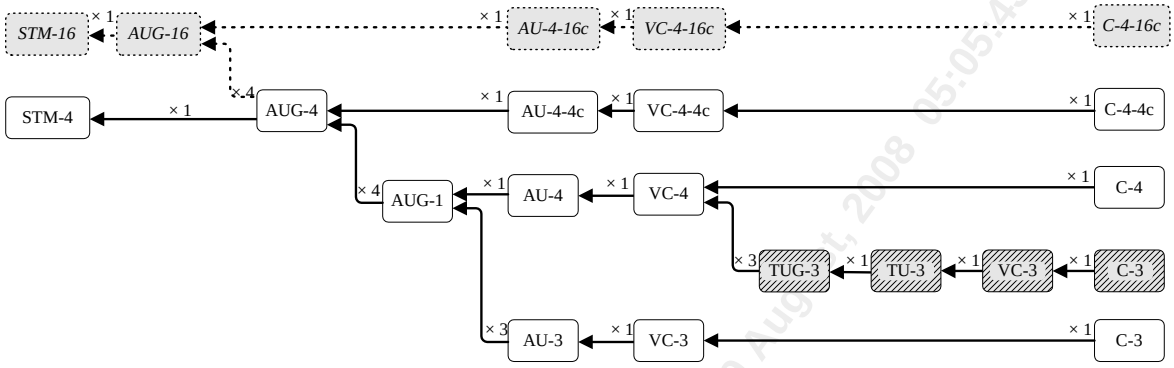
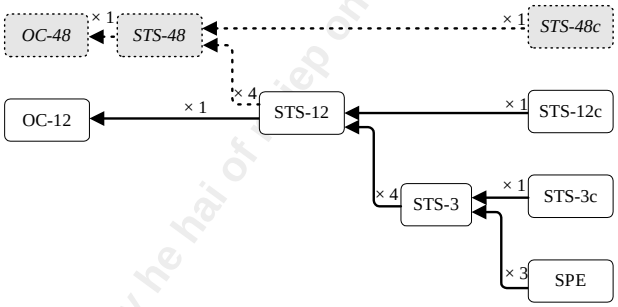


Figure 24 Supported SONET Frame Structures in Bypass Path



Notes

1. The Bypass Path does not support VT/TU mapped payloads.
2. In SDH, an AU4/VC4/TUG3/TU3/VC3/C3 payload may be input to the Bypass path, but the Bypass path will convert this to an AU3/VC3/C3 payload before outputting it.
3. AU4-16c/STS-48c is supported with four payload processors.
4. Frames may consist of any legal mix of the above payloads.

The Bypass path aligns the synchronous payloads of an STS-12/STM-4 byte serial stream to a new transport frame reference (J0). It inserts valid high order pointer bytes (H1, H2), framing bytes (A1, A2), and otherwise all-zero transport overhead bytes.

The SVCA_R interrupts can be disabled on an STM-0/STS-1 basis for the tributary traffic to suppress extraneous interrupts.

The Bypass path performs the AU4 to AU3 conversion shown in Table 10.

Table 10 Bypass Path AU4 to AU3 Conversion

Incoming Payload	Outgoing Payload	Outgoing VC4 Path Overhead	Outgoing VC3 Path Overhead
AU4/VC4/TUG3/TU3/VC3/C3	AU3/VC3/C3	N/A	Same as Incoming VC3 Path Overhead

10.6.3 Tributary-Bypass Mux

There are four distinct types of operation that the Payload Processor can perform, two for each of the two paths:

- Tributary Path: VT/TU mapped payload processing.
- Tributary Path: AU3/AU4 conversions.
- Bypass Path: non-VT/TU mapped payload processing including contiguously concatenated payloads.
- Bypass Path: AU4 to AU3 conversion.

All four operations occur at STS-1/STM-0, STS-3/STM-1, or STS-12/STM-4 granularities depending on the operation and payload configuration.

The Tributary-Bypass Mux selects the TelecomBus stream from either the Tributary Path or Bypass Path on an STM-0/STS-1 timeslot basis. The selection of the valid path (Tributary or Bypass) for each STM-0/STS-1 timeslot is user programmable.

10.6.4 VT/TU Pointer Interpreter (VTPI)

When used for SONET compatible operation, the VT/TU Pointer Interpreter (VTPI) processes the tributary payload pointers in the incoming STS-12 data stream. Each of the seven tributary groups (VT groups) per STS-1 may be independently configured to accept any of the four tributary types (VT1.5, VT2, VT3, or VT6). Based on the value of the tributary pointer (V1, V2 bytes), a reference signal is generated to mark the beginning of a VT SPE (V5 byte). The VTPI maintains the relative rates and justification events for further processing by downstream blocks. To assist downstream blocks in tributary processing, the VTPI provides control signals for tributary framing.

Similarly, when used for SDH compatible operation, the VTPI processes the tributary payload pointers in all AU3s or any of the three TUG3s in an AU4 of the incoming STM-4 data stream. Each of the seven TUG2s per TUG3 or AU3 may be independently configured to accept any of the three tributary types (TU11, TU12, or TU2). Alternately, the VTPI can process the payload pointer of a single TU3 mapped into a TUG3. A reference signal is generated to mark the beginning of a virtual container or VC (V5 byte). The VTPI maintains the relative rates and justification events for further processing by downstream blocks. To assist downstream blocks in tributary processing, the VTPI provides control signals for tributary framing.

The VTPI detects for loss of pointer and pointer re-acquisition for each tributary, and optionally generates interrupts. Tributary alarm indication signal (AIS) is also detected and interrupts are optionally generated upon detection of AIS and its removal. Externally provided high order AIS conditions are optionally translated to low order tributary AIS conditions on a per STS-1/STM-0 basis.

The VTPI optionally bypasses selected low order control signals in a transparent mode or generates them internally.

New incoming tributary pointer values may be filtered until confirmed by receipt of the same pointer values three times or the changes are corrected by receiving the new data flag in the corresponding incoming tributary payload pointer.

Per tributary performance monitoring is supported via positive and negative justification counts and a performance monitoring interface.

Incoming STS-1 path overhead bytes are transferred to the outgoing stream. There are no justification events performed. Therefore, the incoming and outgoing streams maintain identical frame rates and justification events.

10.6.5 Receive Tributary Trace Buffer (RTTB336)

The RTTB336 is a SONET/SDH STS-12/STM-4 Receive Tributary Trace Buffer. A tributary trace message (SONET) or a trail trace identifier (SDH) contains a repetitive path access point identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. Tributary trace messages or trail trace identifiers are contained in both J1 and J2 bytes. Formats for tributary trace messages and trail trace identifiers differ slightly from standard to standard, but are typically like the ones shown in Table 11.

Table 11 Typical Tributary Trace Message Format (SONET)

0XXX XXXX	Byte 1 - ASCII printable [i.e., 20H through 7EH]
0XXX XXXX	Byte 2 - ASCII printable [i.e., 20H through 7EH]
. .	
. .	
. .	
0XXX XXXX	Byte 62 - ASCII printable [i.e., 20H though 7EH]
0000 1101	Byte 63 - Carriage-Return
0000 1010	Byte 64 - Linefeed

Table 12 Typical Trail trace Identifier Format (SDH)

1XXX XXXX	Trace identifier Frame Alignment Signal (TFAS)
0XXX XXXX	Byte 2
. .	
. .	
. .	
0XXX XXXX	Byte 16

The entire tributary trace message or trail trace identifier (i.e., the collection of 64 or 16 bytes) is sometimes referred to as a multiframe.

The RTTB336 can be configured for either SONET or SDH compatible operation. When configured for SONET compatible operation, the RTTB336 processes the tributary trace message within the path trace (J2) byte of the virtual tributaries carried in an incoming STS-12 synchronous payload envelope. Each of the eighty-four tributary groups (VT groups) may be independently configured to accept any one of the four tributary types (VT1.5, VT2, VT3, and VT6).

When configured for SDH compatible operation, the RTTB336 processes for an incoming STM-4, the trail trace identifier within (a) the path trace (J2) byte of the tributaries carried in TUG2 tributary unit groups within VC3 virtual containers, (b) the path trace (J2) byte carried in TUG3 tributary unit groups in VC4 virtual containers, or (c) the path trace (J1) byte of TU3 tributary units carried in TUG3 tributary unit groups of VC4 virtual containers. Each of the four STM-1's within the STM-4 may be independently configured to accept one of (a), (b) or (c). Each TUG2 may be independently configured to accept any one of the three tributary types (TU-11, TU-12, and TU-2). Note that since the RTTB336 only processes the J1/J2 bytes of tributary units, it does not process the J1 byte of a VC4.

Two algorithms are defined for processing the tributary trace message and trail trace identifier. Algorithm 1 is TELCORDIA and ANSI compliant and is typically used in SONET. It detects Trace Identifier Mismatch (TIM) on a 16 or 64 byte tributary trace message. Algorithm 2 is ITU-T compliant and is typically used in SDH. It detects Trace Identifier Unstable (TIU) and TIM on a 16 or 64 byte trail trace identifier.

By way of clarification, please note that there are no TIM or TIU defect processing standards at the tributary level—they are just defined for the path or higher level. For example, GR-253-2000 states on pages 6-39, "At this time, TIM defects and failures have been defined in SONET only for STS paths; however, they could be defined for VT paths (or possibly at the Section layer) in the future." Consequently, the standards defined at the path and/or section level have been borrowed to define TIM and TIU processing at the tributary level.

Algorithm 1 – TELCORDIA and ANSI Compliant (Typically SONET)

This algorithm captures, synchronizes, and validates the tributary trace message. The current tributary trace message is stored in the captured page. The received message can be configured to synchronize when receiving either a byte with its Most Significant Bit (MSB) high, or on the Carriage-Return/Linefeed (CR=0DH, LF=0AH) ASCII characters of the message. If the RTTB336 synchronizes to the MSB of the message (i.e., the TFAS), the byte with its MSB set high is placed in the first location (position 0) of the captured page. If the RTTB336 synchronizes on the CR/LF characters of the message, the LF byte is placed at the last location of the message (position 15 or 63), and the following byte is placed at the first location (position 0) of the captured page.

A trace identifier mismatch (TIM) is declared when none of the last 20 messages match the expected message. A TIM is removed when 16 or more of the last 20 messages match the expected message. When the ZEROPGEN register bit is asserted, all zeros messages are given special consideration: TIM is declared when none of the last 20 messages either are all zeros or match the expected message; TIM is deasserted when 16 or more of the last 20 messages (a) are all zeros, (b) match the expected message, or are some mixture of (a) and (b). An interrupt is optionally generated upon a change in the TIM state. The expected tributary trace message is a static message written in the expected page by an external microprocessor.

The accepted page provides a debounced version of the captured message. A tributary trace message is placed in the accepted page when the identical message is received for 3 or 5 consecutive multiframes, as configured by the PER5 register bit. When the NOSYNC register bit is logic 0, a tributary trace message can only be declared persistent if it is appropriately synchronized via CR/LF characters or the TFAS. When the NOSYNC register bit is logic 1, tributary trace messages without synchronization can be declared persistent. In the special case where NOSYNC is logic 0 and ZEROPGEN is logic 1, all zeros messages can be declared persistent.

Algorithm 2 – ITU-T Compliant (Typically SDH)

This algorithm captures, synchronizes, monitors persistency, monitors stability and validates the trail trace identifier. The current received trail trace identifier is stored in the captured page. The received identifier can be configured to synchronize when receiving either a byte with its MSB high, or on the CR/LF ASCII characters of the identifier. If the RTTB336 synchronizes on the MSB of the identifier (i.e., the TFAS), the byte with its MSB high is placed in the first location (position 0) of the captured page. If the RTTB336 synchronizes on the CR/LF characters of the identifier, the LF byte is placed at the last location of the identifier (position 15 or 63), and the following byte is placed in the first location (position 0) of the captured page.

A persistent trail trace identifier is declared when an identical identifier is received for 3 or 5 consecutive multiframes, as configured by the PER5 register bit. When the NOSYNC register bit is logic 0, a trail trace identifier can only be declared persistent if it is appropriately synchronized via CR/LF characters or the TFAS. When the NOSYNC register bit is logic 1, trail trace identifiers without synchronization can be declared persistent. In the special case where NOSYNC is logic 0 and ZEROPGEN is logic 1, all zeros messages can be declared persistent. A persistent trail trace identifier becomes the accepted trail trace identifier. The accepted identifier is stored in the accepted page.

A trail trace identifier mismatch (TIM) is declared when the accepted identifier does not match the expected identifier. A TIM is removed when the accepted identifier matches the expected message. When the ZEROPGEN register bit is asserted, all zeros messages are given special consideration: TIM is declared when the accepted identifier is neither all zeros nor a match to the expected identifier; TIM is removed when the accepted identifier is either all zeros or a match to the expected identifier. An interrupt is optionally generated upon a change in the TIM state. The expected identifier is a static identifier written in the expected page by an external microprocessor.

An unstable trail trace identifier (TIU) is declared when one or more erroneous bytes are detected between the current received identifier and the previous received identifier in a total of 8 or 127 trail trace identifiers without an intervening persistent message. A TIU is removed when a persistent message is received. An interrupt is optionally generated upon a change in the TIU state.

The TIM algorithms contain other features as well. First, both algorithms are robust in the presence of bit errors. Second, in Algorithm 1, a change in the phase of the incoming J2 byte causes only one sample to be mismatched for the purposes of detecting TIM (a change of phase could be caused, for example, by upstream protection switches causing one or more J2 bytes to be dropped or repeated). Third, monitoring of TIM and TIU can be suspended via the SUSPEND function. SUSPEND is optionally enabled when the J2 byte becomes inaccessible (e.g., when a Loss Of Pointer or Alarm Indication Signal defect has been detected). SUSPEND is controlled via top-level registers to be a logical OR of any combination of the following alarms from the VTPI: LOM, Tributary LOP, Tributary AIS, Path AIS.

Note

- The terms “tributary trace message,” “trail trace identifier,” and “trail trace message,” are used interchangeably in this document.

10.6.6 Receive Tributary Overhead Processor (RTOP336)

When configured for SONET compatible operation, the RTOP336 SONET/SDH STS-12/STM-4 Receive Tributary Overhead Processor processes the path overhead bytes of tributaries in an STS-12 stream. Each tributary group (VT group) may be independently configured to accept any of the four tributary types (VT1.5, VT2, VT3, and VT6). The RTOP336 extracts the four tributary path overhead bytes (V5, J2, Z6, and Z7) from each tributary and outputs the bytes from all tributaries together bit serially. The RTOP336 may be configured for SDH compatible operation. The incoming stream may carry the AU3 of an STM-4 stream or a TUG3 of an AU4 in an STM-4 stream. Each tributary unit group (TUG2) may be independently configured to accept any of the three tributary types (TU-11, TU-12 and TU2). The RTOP336 extracts the four tributary path overhead bytes (V5, J2, N2, and K4) from each tributary and outputs the bytes from all tributaries together bit serially with an associated serial clock. The incoming stream can also carry a TU3 tributary. In that case, the RTOP336 extracts the nine path overhead bytes (J1, B3, C2, G1, F2, H4, F3, K3, N1) and outputs the bits serially.

The RTOP336 compares the BIP-2 code (BIP-8 code in TU3 mode) in the current tributary SPE multiframe with the calculated BIP-2 (BIP-8 code in TU3 mode) value from the previous tributary SPE multiframe. The results of the comparison of all the tributaries are combined into a bit-serial output timed by the serial tributary overhead output clock. BIP-2 (BIP-8 code in TU3 mode) errors of each tributary are also accumulated to one of a set of internal counters for performance monitoring purposes. The number of BIP errors is also output through a parallel alarm interface.

The tributary path signal label in the V5 byte (C2 byte in TU3 mode) and extended path signal label (bit 1 of K4 byte if configured) of each tributary is filtered and extracted into one of a set of internal registers. The tributary PSL is monitored for consistency over consecutive multiframes and can be compared with an expected value. Interrupts can be optionally generated upon PSL unstable and PSL mismatch events. The RTOP336 also monitors PSL for unequipped signal (UNEQ) and reports the UNEQ, PLSU, PLSM states through a parallel alarm interface.

The tributary far end block error bit in the V5 byte (G1 byte in TU3 mode) of each tributary is monitored. The FEBE bit of all the tributaries are combined into a bit-serial output. The FEBE indication of each tributary is also accumulated to one of a set of internal counters for performance monitoring purposes.

The tributary remote failure indication and remote defect indication bits in the V5 byte (G1 byte in TU3 mode) of each tributary is monitored. The RDI and RFI bits are filtered and may optionally generate interrupts upon change of state. The RTOP336 can also be configured to extract and filter the enhanced RDI from K4/Z7 byte (G1 byte in TU3 mode) and may optionally generate interrupts upon change of state. The outgoing tributary RDI, RFI, and PDI-V are output through the serial interface. The incoming tributary enhanced RDI and RDI/RFI states are also output through the serial interface.

The RTOP336 detects tributary payload defect indication (PDI-V) for each incoming tributary and output to the downstream functional block. The RTOP336 generates tributary path AIS indication for the outgoing tributaries as a consequential action upon a received AIS, LOP, LOM, PSLM, PSLU, UNEQ, TIU, or TIM alarm.

The RTOP336 can also be configured to generate the inband error report. This feature allows the insertion of remote alarm signals (RDI/RFI/ERDI[2:0]/REI) into the V5 byte (G1 byte for TU3 mode) in the outgoing tributaries. Table 13 summarizes the priority encoding for the G1 byte (TU3 mode) or V5/Z7(K4) bytes (non-TU3 mode) when inband error reporting is enabled by setting the RTOP336 IBER register bit to a logic 1. The table enumerates the values inserted into the G1 or V5/Z7(K4) bytes when enhanced remote defect indication is enabled (ERDIEN is set to a logic 1) and disabled (ERDIEN is set to a logic 0), respectively. Bits marked as “pass” are not modified.

Table 13 Priority of Triggers for RDI / ERDI Insertion and Insertion Values

Mode	Priority	Triggers	Interpretation	Positions			
				TU3 Mode (Insert into G1)			
				G1 Bit 5		G1 Bit 6	
				Non-TU3 Mode (insert into V5/Z7(K4))			
				V5 Bit 8	Z7(K4) Bit 5	Z7(K4) Bit 6	Z7(K4) Bit 7
ERDIEN=0	1	AIS, LOP, LOM, TIM, TIU, UNEQ, PLSU, PSLM	Remote server defect	1	pass	pass	pass
	2	No Defects	No remote defect	0	pass	pass	pass
ERDIEN=1	1	AIS, LOP	Remote server defect	1	1	0	1
	2	UNEQ, TIM	Remote connectivity defect	1	1	1	0
	3	PSLM	Remote payload defect	0	0	1	0
	4	No defects	No remote defect	0	0	0	1

Notes

1. In TU3 mode, G1 byte contains RDI/ERDI. In non-TU3 mode, V5/Z7(K4) byte contains RDI/ERDI.
2. Insertion requires the RTOP336 IBER register bit to be set to logic 1.

Payload Signal Label Processing

The RTOP336 processes the payload signal label (PSL) and detect payload label unstable (PSLU), payload mismatch (PSLM), payload defect indication (PDI), and payload unequipped defects. The PSL value is extracted from the C2 byte when the tributary is in TU3 mode, from V5 byte bit 5-7 when the tributary in non-TU3 mode, and from K4 bit 1 when the tributary is in extended PSL mode. Since the Telcordia and ITU-T standard have different requirements, both algorithms are defined and can be selected with the PSLMODE register bit.

The PSL3 configuration bit determines the PSL threshold value (n) of both the Telcordia and ITU-T algorithm. When PSL3 is set to logic 0, n = 5, and when PSL3 is set to logic 1, n = 3.

Telcordia Standard Algorithm:

The Telcordia algorithm detects payload mismatch (PSLM) defect, path unequipped (UNEQ) and tributary payload defect indications (PDIV) from the PSL pattern in tributary overhead bytes. The PSLM, UNEQ, and PDIV defects are reported via the tributary status registers.

The concept of persistent or accepted PSL is not defined in the Telcordia algorithm, so no PSLU defect will be declared. (PSLU is set to logic 0) The accepted payload signal label register bits (APSL[7:0]) are irrelevant when using this algorithm. The APSL will still be updated according to the ITU-T algorithm.

According to Table 14, the Telcordia algorithm declare a PSLMV alarm when the received PSL is defined as mismatch for n consecutive (multi-)frames. The algorithm removes the PSLMV alarm when the received PSL matches is defined as mismatch for n consecutive (multi-)frames. The expected PSL is a static 8-bit pattern written by an external microprocessor. In non-TU3 mode, the 3 bit EPSL is zero padded to form a 8 bit EPSL. The Telcordia standard does not specify extended PSL mode, therefore EXTDPSL must set to logic 0 when using this algorithm.

Table 14 also shows that the Telcordia algorithm declares an UNEQV alarm when the received PSL is defined as unequipped for n (multi-)frames. The algorithm removes the UNEQV alarm when the received PSL is defined as not unequipped for n consecutive (multi-)frames.

Finally, Table 14 illustrates that the Telcordia algorithm declares the PDIV alarm when PDIV defects are reported by the received PSL for n consecutive (multi-)frames. The algorithm removes the PDIV when PDIV defects are not reported by the received PSL for n consecutive (multi-)frames or the expected PDI code value is changed to “00000”. The expected PDI code consists of a static 5bit pattern written by the microprocessor.

In the Telcordia standard, PSL code FF in TU3 mode and 07 in non-Tu3 mode is marked as reserved value and requires special attention. Receiving the reserved PSL code will not cause any changes in the existing PSLMV, UNEQ and PDIV status.

ITU-T Standard Algorithm:

The ITU-T algorithm detects payload signal unstable (PSLU) defect, payload signal label mismatch (PSLM) defect, path unequipped (UNEQ) and tributary payload defect indication (PDVI) on the PSL. The PSLU, PSLM, UNEQ and PDIV defects are reported via the RTOP336 tributary status registers.

The ITU-T algorithm declares a persistent payload signal label (PSL) when an identical PSL is received for n consecutive (multi-)frames. When a persistent PSL is found, the persistent PSL becomes the accepted PSL. The accepted PSL is stored in a microprocessor readable register. (APSL[7:0]) The ITU-T algorithm declares a PSLU defect when n received PSL codes differ from the previously received PSL without any persistent PSL in between. The algorithm removes a PSLU defect when a persistent PSL is found.

According to Table 14, a PSLMV alarm is declared when the accepted (persistent) PSL does not match the expected PSL. The algorithm removes a PSLMV when the accepted (persistent) PSL matches the expected PSL. The expected PSL is a static 8-bit pattern written by an external microprocessor into a device register.

Table 14 also shows that the ITU-T algorithm declares an UNEQV alarm when the accepted (persistent) PSL is interpreted as unequipped. The algorithm removes an UNEQV when the accepted (persistent) PSL is interpreted as not unequipped.

Finally, Table 14 also illustrates the ITU-T algorithm declares a PDIV alarm when PDIV defects are reported by the accepted (persistent) PSL. The algorithm removes a PDIV alarm when no PDIV defects are reported by the accepted (persistent) PSL. The expected PDIV code consists of a static 5bit pattern written by an external microprocessor.

Both Telcordia and ITU-T algorithm use Table 14 to filter the alarm conditions. When PDI[4:0] is set to “00000”, there is no expected PDI and the PDI defect indication is disabled. In non-TU3 mode, the only valid expected PDI value is 06h. Therefore, only PDI[4:0] = “00110” is allowed in the configuration. In TU3 mode, the expPDI is E0h + PDI[4:0].

Table 14 PLMV, UNEQV, and PDIV Defects Declaration

Expected PSL		Accepted/Received PSL			PSLMV	UNEQV	PDIV
ITU-T algorithm, TU3 mode							
00	Unequipped	00	Unequipped		match	inactive	inactive
		01	Equipped non Specific		mismatch	inactive	inactive
		02-E0 FD-FF	Equipped specific		mismatch	inactive	inactive
		E1-FC	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI	mismatch	inactive	inactive
01	Equipped non specific	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-E0 FD-FF	Equipped specific		match	inactive	inactive
		E1-FC	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI	match	inactive	inactive
02-FF	Equipped specific PDI	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-E0 FD-FF	Equipped specific	= EPSL	match	inactive	inactive
				!= EPSL	mismatch	inactive	inactive
		E1-FC	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI, = EPSL	match	inactive	inactive
				no expPDI, != EPSL	mismatch	inactive	inactive
Telcordia algorithm, TU3 mode							
00	Unequipped	00	Unequipped		match	inactive	inactive
		01	Equipped non Specific		mismatch	inactive	inactive
		02-E0 FD-FE	Equipped specific		mismatch	inactive	inactive
		FF	Reserved		no change	no change	no change
		E1-FC	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI	mismatch	inactive	inactive
01	Equipped non specific	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive

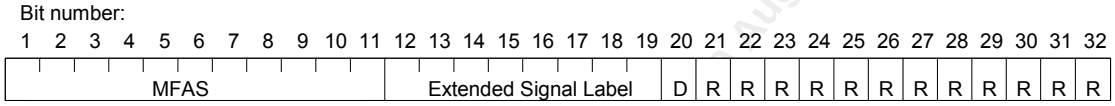
Expected PSL		Accepted/Received PSL			PSLMV	UNEQV	PDIV
		02-E0 FD-FE	Equipped specific		match	inactive	inactive
		FF	Reserved		no change	no change	no change
		E1-FC	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI	match	inactive	inactive
02-FF	Equipped specific PDI	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-E0 FD-FE	Equipped specific	= ESPL	match	inactive	inactive
				!= EPSL	mismatch	inactive	inactive
		FF	Reserved		no change	no change	no change
		E1-FC	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI, = EPSL	match	inactive	inactive
				no expPDI, != EPSL	mismatch	inactive	inactive
ITU-T Algorithm, non TU3 mode (including both extended and non-extended PSL mode)							
00	Unequipped	00	Unequipped		match	inactive	inactive
		01	Equipped non Specific		mismatch	inactive	inactive
		02-05 07-FF	Equipped specific	= EPSL	match	inactive	inactive
				!= EPSL	mismatch	inactive	inactive
		06	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI	mismatch	inactive	inactive
01	Equipped non specific	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-05 07-FF	Equipped specific		match	inactive	inactive
		06	PDI	= expPDI	match	inactive	defect
				!= expPDI	match	inactive	inactive
				no expPDI	match	inactive	inactive
02-FF	Equipped specific PDI	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-05 07-FF	Equipped specific	= ESPL	match	inactive	inactive
				!= EPSL	mismatch	inactive	inactive
		06	PDI	= expPDI	match	inactive	defect

Expected PSL		Accepted/Received PSL			PSLMV	UNEQV	PDIV
				!= expPDI, = EPSL	match	inactive	inactive
				!= expPDI, != EPSL	mismatch	inactive	inactive
				no expPDI, = EPSL	match	inactive	inactive
				no expPDI, != EPSL	mismatch	inactive	inactive
Telcordia Algorithm, non TU3 mode (only non-extended PSL mode)							
00	Unequipped	00	Unequipped		match	inactive	inactive
		01	Equipped non Specific		mismatch	inactive	inactive
		02-05	Equipped specific	= EPSL	match	inactive	inactive
				!= EPSL	mismatch	inactive	inactive
		06	PDI	= expPDI	match	inactive	defect
				!= expPDI	mismatch	inactive	inactive
				no expPDI	mismatch	inactive	inactive
		07	Reserved		no change	no change	no change
01	Equipped non specific	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-05	Equipped specific		match	inactive	inactive
		06	PDI	= expPDI	match	inactive	defect
				!= expPDI	match	inactive	inactive
				no expPDI	match	inactive	inactive
		07	Reserved		no change	no change	no change
02-07	Equipped specific PDI	00	Unequipped		mismatch	unequipped	inactive
		01	Equipped non Specific		match	inactive	inactive
		02-05	Equipped specific	= ESPL	match	inactive	inactive
				!= EPSL	mismatch	inactive	inactive
		06	PDI	= expPDI	match	inactive	defect
				!= expPDI, = EPSL	match	inactive	inactive
				!= expPDI, != EPSL	mismatch	inactive	inactive
				no expPDI, = EPSL	match	inactive	inactive
				no expPDI, != EPSL	mismatch	inactive	inactive
		07	Reserved		no change	no change	no change

Extended PSL

When extended PSL mode is configured (EXTDPSL is set to logic 1, only allowed when PSLMODE is set to logic 1) in the RTOP336, the extended PSL is located in bit 1 of K4 byte over 32 multi-frames. Figure 25 shows the extended PSL bit sequence. The multi-frame alignment signal (MFAS) consists of "0111 1111 110". The extended signal label (extPSL) is contained in bits 12 to 19. Bit 20 is ignored in the MFAS alignment, and the remaining 12 bits are reserved for future standardization and normal set to zero.

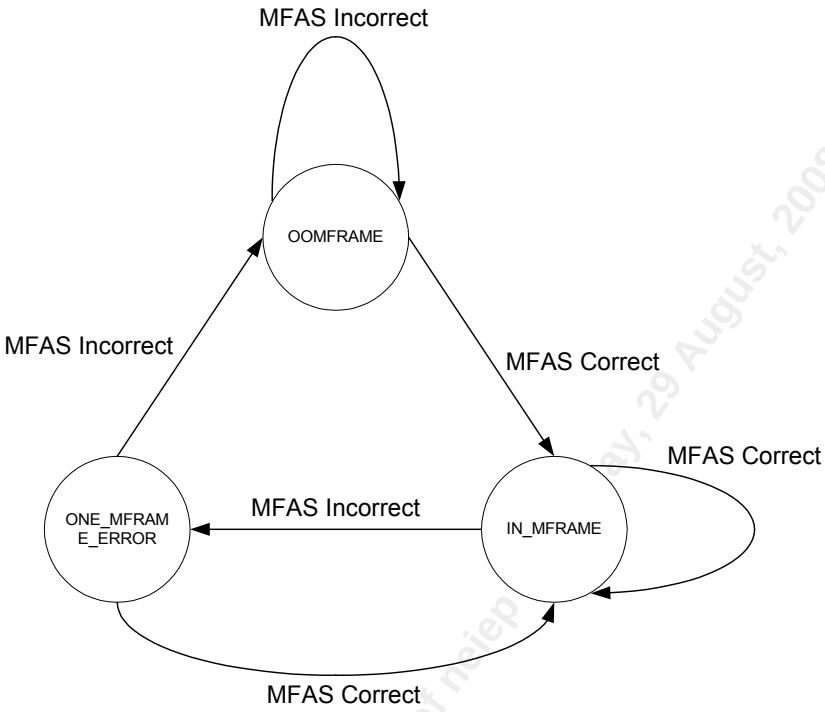
Figure 25 VC-1/2 Extended Signal Label (Extracted from ITU-T G.707)



MFAS Multiframe alignment bits
D Don't care
R Reserved bit

The MFAS is detected by a multi-frame alignment state machine which is within the PSL processor block. The MFAS state machine only search for the MFAS pattern in Out Of Multi-Frame (OOM) state. Once the pattern is found, the MFAS state machine changes to In Multi-Frame state (IM), and will continuously checked the presumed multi-frame state position for the alignment. Only the first 11 bits of the 32 bit sequence is checked against the MFAS pattern for frame alignment, the remaining bits will be ignored. The Frame alignment is lost (entering OOM state) when two consecutive MFAS mismatch the MFAS alignment pattern "0111 1111 110". The Frame alignment is deemed to have been recovered (entering the IM sate) when one correct MFAS is found. When the MFAS is in OOM state and the tributary is configure to extended PSL mode, the PSLM is set to high. Figure 26 shows the state diagram for the multiframe alignment state machine.

Figure 26 Extended PSL Multiframe Alignment State Diagram



When the MFAS state machine is not in OOM state, bit 12 to bit 19 in the 32 bit sequence are extracted as the extended PSL which is then stored in the State RAM. Similar to the 3-bit PSL, the 8-bit extended PSL is processed by the ITU-T algorithm to determine the PSLM, PSLU and PDIV alarm status. In G.707 specification, extended PSL value “00” to “07” is reserved to give a unique name to the non-extended PSL signal label. The ITU-T algorithm will process the value “00” to “07” from extended PSL as they are non-extended PSL.

In both Telcordia and ITU-T mode, when PSLMPERSIST is set to high, the assertion of UNEQ status will clear the PSLMV status.

In summary, the Telcordia algorithm has three separate state machines that keep tracks of the PSLM, UNEQ and PDIV states. The algorithm filters the received PSL to generate mismatch, unequipped and pdi defect first, then updates the corresponding state machines.

The ITU-T algorithm has two state machines that keep tracks of accepted PSL and PSLU. The ITU-T algorithm debounce the received PSL and store the value in accepted PSL first, then the algorithm filters the accepted PSL to generate the PSLM, UNEQ and PDIV status. The PSLU state machine is updated by comparing the current and previous received PSL.

10.6.7 VT/TU Payload Aligner (VTPA)

When configured for SONET compatible operation, the VT/TU Payload Aligner (VTPA) generates the tributary payload pointers for the outgoing STS-12 data stream. Each of the seven tributary groups (VT groups) per STS-1 stream may be independently configured to accept any of the four tributary types (VT1.5, VT2, VT3, and VT6).

Similarly, when configured for SDH compatible operation, the VTPA generates the tributary payload pointers in the VC3s or the TUG3s in a VC4 of the outgoing STM-4 data stream. Each of the seven tributary unit group twos (TUG2s) in a TUG3 or VC3 may be independently configured to accept any of the three tributary types (TU11, TU12, and TU2). Alternately, the VTPA can accept an incoming VC3 mapped into an AU3 or a TU3 mapped into a TUG3 while processing the payload pointer of a single outgoing TU3 mapped into a TUG3.

The VTPA aligns the outgoing tributary multiframe to an equipment reference. The alignment is accomplished by calculating the tributary payload pointer values based on the status of the elastic store buffer. The VTPA translates incoming STS/AU pointer justifications to tributary pointer resulting in all VT/TUs being located in fixed columns of the transport frame. It provides software configurable offset between the payload frame boundaries (J1) and the H3 byte of the transport overhead (High Order H1, H2 pointer value = 0 or 522). It aligns the synchronous payloads of an STS-12/STM-4 byte serial stream to a new transport frame reference (J0). It inserts valid high order pointer bytes (H1, H2), framing bytes (A1, A2).

Incoming tributary pointer justifications may be attenuated or optionally translated immediately into outgoing tributary pointer justification events on a per-tributary basis. Outgoing pointer justifications may be strictly limited to once per three multiframes. The VTPA will optionally generate interrupts on generating an outgoing pointer justification. Per tributary performance monitoring is also supported via positive and negative justification counts and a performance monitoring interface. Incoming STS/AU pointer justifications have the same effect as a tributary pointer justification on one of the tributaries in the incoming data stream. Of the tributaries carried in the incoming data stream, the one tributary affected depends on the relative phase of the incoming STS-1 frame and the incoming SPE. The STS/AU pointer justification is attenuated depending on whether the affected tributary is configured to attenuate incoming pointer events.

The VTPA uses an elastic store to accommodate the differing data rates on the incoming and outgoing streams. Interrupts are optionally generated when the tributary elastic store overflows or underflows. The VTPA provides optional insertion of tributary path AIS or tributary idle (unequipped; the idle pattern is configurable) and will insert tributary path AIS on any tributaries with an AIS condition. The VTPA can be configured to insert a new BIP2 value into the V5 byte (non-TU3 mode; BIP8 into the B3 byte for TU3 mode). The VTPA can also insert inverted new data flag fields, which can be used to diagnose downstream pointer processing elements.

Incoming STS-1 (VC3/VC4) path overhead bytes may be optionally transferred to the outgoing stream on a best effort basis. Error-free transfer cannot be guaranteed as the incoming and outgoing payload frame rates may differ resulting in an excess or deficit of incoming POH bytes on the incoming stream relative to the outgoing stream. Path overhead pass-through is disabled for any STS-1 configured to process a C3 mapped into a VC3.

The VTPA provides optional squelch control on a tributary multiframe (H4). The multiframe alignment sequence can be reset to all ones. Normal sequencing resumes when the squelch control is removed.

The VTPA regenerates transport overhead bytes (except A1/A2/H1/H2 bytes), fixed stuff bytes and tributary V4 byte with all-zero pattern.

10.6.8 SONET/SDH Virtual Container Aligner (SVCA_R)

The SVCA_R aligns the transport overhead of an STS-12/STM-4 stream to a new reference signal. When used in the SONET/SDH receive path, it aligns the transport overhead to an transport frame reference (J0). The alignment is accomplished by recalculating the STS payload pointer value based on the offset between the transport overhead of the incoming and outgoing streams. It inserts valid high order pointer bytes (H1, H2), framing bytes (A1, A2), and otherwise all-zero transport overhead bytes.

Multiple SVCAs can be used to process higher concatenated payloads (STS-48c/VC4-16c). An STS-48c/VC-4-16c is processed by four SVCA. The first SVCA is master and the three others are slaves.

Outgoing pointer justification events are indicated on two separate outputs. A slave SVCA uses one of these outputs to perform the required justification when a concatenated STS-48c/STM-16c is processed. The other set of outputs can be used for performance monitoring. Excessive pointer justification events may indicate network synchronization failure. Finally, the SVCA provides pointer justification performance counters for each path.

The SVCA aligns the synchronous payload of any legal mix of STS-1/3c/12c (VC-3/4/4c). The STS (VC) payloads are independently floating inside the STS-12 (STM-4) transport frame. The SVCA must align each one independently.

The SVCA provides support for a VC4 virtual container carrying TUG-3 tributary data. The SVCA removes TUG-3 fixed stuff columns (#1, #2, #3, #4, #5, and #6) and adds VC-3 fixed stuff columns (#30 and #59) on the system side-outgoing stream.

External PAIS insertion is provided to insert path alarm indication signal (AIS) in the outgoing SONET/SDH stream on a per path basis. Also, internal events (FIFO overflow or underflow) optionally cause path AIS insertion.

The SVCA supports a transparent bypass mode. In this case, the SVCA does not buffer the input stream nor realign it. The SVCA simply clocks out the input data on the next output clock rising edge.

The SVCA provides an interrupt output to indicate any changes in the status of output pointer justification (NJE, PJE) and FIFO overflows or underflows. Each interrupt source is independently maskable.

The SVCA may generate double NDFs for a given path when coming out of AIS. In the first of the two NDFs it may give an invalid pointer value. It recovers from the second NDF onwards. The SVCA may also remove the J1 pulse of a path in AIS. If the J1 pulse is it returns on the second NDF. This behavior will change depending on the incoming pointer values.

10.6.9 Low-Order (VT/TU) Path Signal Degrade and Excessive Error Defect Monitoring (TBER)

The Low-Order (VT/TU) Path Signal Detect and Excessive Error Defect Monitoring (TBER) block provides 2 independent bit error rate (BER) monitoring circuits (BERM block). They are used to monitor the VT/TU path bit error rate indicator (BIP-2). One BERM block monitors the VT/TU Signal Degrade (SD) alarm and the other BERM block monitors the VT/TU excessive error defect (DEXC) alarm.

10.6.10 Tributary Alarm Summary Reporting (TASR)

The tributary alarm summary reporting block (TASR) detects the signal fail (SF) condition based on tributary defects. The TASR receives defect indication signals (LOP, AIS, AIS_AGGR, UNEQ, TIM, TIU, PSLM, PSLU, LOM, PDI, DEXC and SD) from upstream tributary processors. A tributary SF alarm is generated when any one of the enabled upstream alarms for the tributary is asserted. Table 15 summarizes the source of alarms that contribute to the SF condition. The bits to enable the contribution of an upstream alarm to the SF condition are located in the TASR Indirect Data Register #1. An interrupt is optionally generated when a SF condition is reported.

The TASR receives per STS-1/STM-0 LOM state information from the VTPI block. A per STS-1/STM-0 interrupt is optionally generated upon a change of LOM state. The TASR provides per STS-1/STM-0 LOM status and interrupt indication bits to trace the source of a LOM alarm.

Table 15 Source of TASR SF Alarm Contributors

ALARM	ALARM_EN Bit	Alarm Source
LOM	LOM_EN	VTPI
LOP	LOP_EN	VTPI
AIS	AIS_EN	VTPI
DEXC	DEXC_EN	TBER
SD	SD_EN	TBER
TIM	TIM_EN	RTTB336
TIU	TIU_EN	RTTB336
PSLM	PSLM_EN	RTOP336
PSLU	PSLU_EN	RTOP336
UNEQ	UNEQ_EN	RTOP336
PDI	PDI_EN	RTOP336
AIS_AGGR	AIS_AGGR_EN	RTOP336

Note

- AIS_AGGR is composed of the enabled AIS contributors reported by the RTOP: UNEQAIS, PSLMAIS, PSLUAIS, TIUAIS, TIMAIS, LOPAIS, and LOMAIS

10.7 Switch Fabric Subsystem

The sixteen MSU-Lite blocks and one CCB block in TUPP 2488 form the switch fabric subsystem. These can be used as:

- An internal Time:Space:Time switch fabric for use in Hairpinning applications and for use in ADM applications where tributaries are continued.
- The Time:Space stages of a Time:Space:Time fabric in the ingress (Drop) direction. The terminating Time stage must be implemented outside the TUPP 2488 in an SBS device.
- The Space:Time stages of a Time:Space:Time fabric in the egress (Add) direction. The initial Time stage must be implemented outside the TUPP 2488 in an SBS device.
- The MSU-Lites may be used with an external NSE to implement a Time:Space:Time fabric for ADM applications.

The Switch Fabric supports eight STS-12/STM-4 input streams. Any SONET/SDH VT/TU up to STS-1/STM-0 can be switched. Each of the ingress STS-12/STM-4 streams is bi-cast into the fabric. There are eight MSU-Lite blocks in the ingress path of TUPP 2488 (two per STS-12/STM-4 slice) and eight MSU-Lite blocks in the egress path (two per STS-12/STM-4 slice) of TUPP 2488. The MSU-Lite block is a time switch.

There is one CCB block in TUPP 2488. The CCB is a space switch.

The CCB block can be bypassed and an external crossbar (e.g. NSE device) can be used instead. The MSU-Lite blocks can form the “Time” stage of a Time:Space:Time switch fabric in conjunction with external NSE and SBS devices.

For T:S:T switching all sixteen input streams to the CCB must align with each other for meaningful switching to occur. Subsystem logic is used to generate alignment control for the ingress streams based on the PP Frame Alignment Delay Register and the egress stream alignment (EJ0 and System Egress Reference Delay values).

Subsystem logic chooses the correct CMP value for each of the functional blocks and will ensure that the CMP values are delayed so they arrive at each block at the correct time.

The user has the option of outputting the J0 character once every four frames to denote multiframe alignment on the system egress output. The first frame of the four-frame multiframe is specified by EJ0.

10.7.1 Memory Switch Unit (MSU-Lite)

The MSU-Lite is an STS-12 77.76 MHz TelecomBus column switch. Any input column can be switched to any output column. Control information is switched along with the data byte.

Data entering the MSU-Lite is stored in two alternating pages of memory. Each page contains one row (1080 bytes) of information. One of these alternating pages is currently filling while the other page is currently full. Data exiting the MSU-Lite is extracted from the currently full page. As a consequence the MSU-Lite imposes a nominal switching latency of 1 row (~13.94 µs). The switching connection memory for the output port contains 13-bit control for each of the 1080 columns in the frame. Dual banks of this control memory are provided to enable hitless frame boundary switchover.

Any changes to the Switch Control RAM data are written into the off-line page through the MPIF. When there is a change in the Switch Control RAM pages, the MSU-Lite can copy the on-line page onto the off-line one. This can also be done by writing to the Interrupt Status and Memory Page Update Register. While this page copy is happening, data is prevented from being written into the off-line page, and an interrupt is generated when the off-line page update is completed. In addition, a change in the connection memory page input, signifying that a change of the RAM pages is to occur at the next frame boundary, is flagged by an interrupt.

The MSU-Lite supports a bypass mode in which no switching is done. In this mode, each STS-12 slice bypasses the corresponding MSU-Lite. Bypass of individual MSU-Lite blocks is not allowed i.e. all eight ingress MSU-Lites must be bypassed together or all eight egress MSU-Lites must be bypassed together.

The MSU-Lites (#9, #10, #11, and #12) contain the per column EMSU_SEL configuration bit used to select which of the bi-casted streams is transmitted to the egress data path.

The MSU-Lite also supports an overwrite mode where columns can be configured with specific overwrite modes. When enabled these modes generate the output stream based on the per column configuration stored in the Switch Control RAM. The overwrite modes are active when the switch control RAM value is out of range (i.e. IN_BYTE(13:12) = 11b). The overwrite modes allow output streams (VT/TU or STS-1/STM-0 level) to be configured to generate outputs such as Unequipped tributaries, generate tributary or path level indicators such as V5 and J1 on the output stream. For further details see Table 38. V5 and TPL overwrite have no effect in the egress path.

10.7.2 Column Cross Bar Switch (CCB)

The CCB block is central to TUPP 2488 in performing column granularity space switching on 16 STS-12 77.76 MHz TelecomBuses. The CCB functions as an STS-192/STM-64 cross bar and allows for hair-pinning and OC-48 ADM functionality (with 1-2 multicasting).

At every clock cycle of the 77.76 MHz clock the CCB switches a byte of data and its associated controls from one of the input ports to an output port. This mapping is software configured in the connection memory page. The switched information may be one byte of a column comprising a VT1.5, VT2, VT3, VT6, or STS-1.

The 16 input buses to CCB must be synchronized (i.e. J0 frame aligned) in order for switching to take place.

Configuration settings for the outputs are stored in two pages of connection memory that are software accessible. Each page of RAM maps all 16 outputs from an input in a 1080 byte row. The dual page configuration architecture allows configuration changes to the offline page to take place while the device is reading from the active page to support hitless switching. When configuration updates are complete, pages are swapped on the next frame boundary.

The CCB supports a bypass mode in which no switching is done. This is configured so that when the CCB is placed in bypass mode, the eight STS-12 streams from the line ingress path are passed through the CCB to the eight system ingress STS-12 streams, and the eight system egress STS-12 streams are passed through the CCB to the line egress path.

10.7.3 Switch Fabric Subsystem Logic

The subsystem logic implements the following functions:

- J0 control
- CMP control
- Bi-Cast multiplexing
- Loopback logic
- Reset control logic

J0 Control

The J0 glue generates an every frame and every four-frame version of the EJ0 reference input signal. These flywheeled signals are offset from the EJ0 position by a programmable offset PP_FRM_ALIGN_DLY.

The J0 glue also generates the J0 reference pulse used by the system CML interface Alignment FIFO. This is generated at a configurable delay from the EJ0 reference input signal. This delay is specified by SYSTEM_EGRESS_REF_DLY

Finally the J0 glue can output the system ingress side OJ0 every frame or every four frames, depending on the SYSTEM_FRAME_MODE configuration bit. This allows the system ingress CML to transmit J0 characters every frame or every four frames.

CMP Control

The CMP glue logic generates the following CMP (Connection Memory Page select) signals for the CCB, Ingress MSU-Lites and Egress MSU-Lites timed appropriately. The logic also selects source of the CMPs dependant on configuration registers, CCB_CMP_SRC, IMSU_CMP_SRC, and EMSU_CMP_SRC.

Bi-Cast Multiplexing

This multiplexes the outputs of the Egress MSU-Lite[12:9] with the outputs of Egress MSU-Lites[16:13]. The control for this multiplexing is from the EMSU_SEL register bit of the eight Egress MSU-Lites[16:9] allowing per column selection between the MSU-Lite pairs.

10.8 Egress Data path

The egress data path blocks sit between the Switch Fabric output and the High Order Path Overhead subsystem transmit section. These blocks perform the following functions:

- High Order Pointer interpretation for traffic received from the system egress RASIO™ CML links.
- Align the synchronous payloads of an STS-12/STM-4 egress byte serial stream to a new transport frame reference (J0). This allows alignment to a line side STS-1 fabric.
- Egress AU3/AU4 conversions.
- Reframing of the realigned egress stream including H1, H2 generation and A1, A2 framing.

10.8.1 SONET/SDH High Order Pointer Interpreter (SHPI)

A total of four SHPI blocks are instantiated in the TUPP 2488 device. The four SHPI blocks are in the egress path between the switch fabric and the egress SVCA_R.

The SHPI can interpret the STS/AU pointers of an STS-12/STM-4 SONET/SDH transport frame. The input is an eight bit serial stream at 77.76 MHz. Four SHPIs can be used to locate the STS SPE (VC) payloads in a STS-48 (STM-16) SONET/SDH transport frame.

The STS SPE (VC) payloads are independently floating inside the transport frame and the SHPI must interpret each of the STS-1/3c/12c (AU3/4/4-4c) pointers in order to locate the boundaries of the payloads; i.e. the path trace bytes (J1). Once the STS SPE (VC) payloads are located, the SHPI indicates the location of each path trace byte. The SHPI also indicates the location of the STS-SPE (VC) payloads and of the path overhead bytes.

The SHPI provides an interrupt output to indicate a pointer justification event, a path loss of pointer, a path alarm indication signal or a BIP error in the STS SPE (VC) payloads. An internal register can be read to identify the interrupt source. Each interrupt source is individually mask-able.

The SHPI blocks in the egress path of TUPP 2488 are needed to indicate the J1 position to the egress byte-wide TelecomBus.

Pointer Interpreter

See 10.5.1 for Pointer Interpreter description.

Concatenation Pointer Interpreter State Machine

See 10.5.1 for Concatenation Pointer Interpreter State Machine description.

10.8.2 Egress SONET/SDH Virtual Container Aligner (Egress SVCA_R)

The SVCA aligns the transport overhead of an STS-12 stream to a new reference signal. The alignment is accomplished by recalculating the STS payload pointer value based on the offset between the transport overhead of the incoming and outgoing streams. It inserts valid high order pointer bytes (H1, H2), framing bytes (A1, A2), and otherwise all-zero transport overhead bytes.

Multiple SVCA can be used to process higher concatenated payloads (STS-48c/VC4-16c). An STS-48c/VC-4-16c is processed by four SVCA. The first SVCA is master and the three others are slaves.

Outgoing pointer justification events are indicated on two separate outputs. A slave SVCA uses one of these outputs to perform the required justification when a concatenated STS-48c/STM-16c is processed. The other set of outputs can be used for performance monitoring. Excessive pointer justification events may indicate network synchronization failure. Finally, the SVCA provides pointer justification performance counters for each path.

The SVCA aligns the synchronous payload of any legal mix of STS-1/3c/12c (VC-3/4/4c). The STS (VC) payloads are independently floating inside the STS-12 (STM-4) transport frame. The J1PIN is multiplexed among the independent payloads. The SVCA must align each one independently. The output pointer justification events are multiplexed among all the output streams.

The SVCA provides support for a VC4 virtual container carrying TUG-3 tributary data. On the transmit side, when TUG-3 configuration bits are enabled, the SVCA removes VC-3 fixed stuff columns (#30 and #59) and inserts VC-4 fixed stuff columns (#1, #2, #3, #4, #5, and #6). It also indicates both the TU-3 and AU-4 trace (J1) bytes. The TU-3 pointer is generated by the SVCA and the AU-4 pointer is a user provided fixed pointer.

External PAIS insertion port is provided to insert path alarm indication signal (AIS) in the outgoing SONET/SDH stream on a per path basis. Also, internal events (FIFO overflow or underflow) optionally cause path AIS insertion.

The SVCA provides an interrupt output to indicate any changes in the status of output pointer justification and FIFO overflows or underflows. Each interrupt source is independently maskable.

10.9 Data Paths in TUPP 2488

The TUPP 2488 can use one of four data paths to cater to different applications.

Hair-Pinning

- Traffic from the line ingress is groomed through the internal Time:Space:Time fabric, (ingress MSU-Lite->CCB->egress MSU-Lite) and is sent back out the line egress.

ADM with Internal Crossbar

- Traffic from the line ingress is routed to the ingress time switches (ingress MSU-Lites), and then exits through either the system ingress via the internal crossbar (CCB), or through the line egress via the internal crossbar and egress time stage (egress MSU-Lites). External time stages (SBS type devices) on the system ingress interface are needed to complete the last time stage of the Time:Space:Time fabric for system ingress traffic.
- Traffic from the system egress is routed to the line egress via the internal crossbar and the egress time stage switches. External time stages devices on the system egress interface complete the first time stage of the Time:Space:Time fabric. Traffic from the system egress can also be routed through the internal crossbar to the system ingress. External time stages on the system egress interface complete the first time stage of the Time:Space:Time fabric.

ADM with External Crossbar

- Traffic from the line ingress is sent to the system ingress. The ingress time stage switches are used but the internal crossbar is not used. An external crossbar and time stage switches on the system ingress are needed to complete the Time:Space:Time fabric.

- Traffic from the system egress is sent to the line egress. The ingress time stage switches are used but the internal crossbar is not used. An external crossbar and time stage switches on the system egress are needed to complete the Time:Space:Time fabric.

Payload Processing Loopback

- Traffic from the line ingress passes through the payload processor blocks, bypasses the internal Time:Space:Time fabric completely and is sent out the line egress parallel bus.

10.10 Latency Through TUPP 2488

Table 16 outlines the latency through the various blocks in TUPP 2488. All blocks (except some parts of the CML subsystems) operate off a 77.76 MHz clock. Therefore, the clock period is 12.86 ns. Table 16 gives the latency in 12.86 ns clocks for each block.

Table 16 Latency through TUPP 2488

	Mode	Min No. of Clocks	Nom No. of Clocks	Max No. of Clocks	Notes
Ingress STSI Subsystem					
STSI	Switching	4	15	27	Time Switch
Glue		2	2	2	
Egress STSI Subsystem					
STSI	Switching	4	15	27	Time Switch
Glue	all modes	2	2	2	
Subsystem in PP_LBEN	PP_LBEN	1	1	1	
Ingress HPOH Subsystem					
Glue and RHPP	all modes	5	5	5	
Egress HPOH Subsystem					
SVCA	all modes	91	175	257	Depends on alignment FIFO
SHPI, THPP and glue	all modes	11	11	11	
Ingress Switch Fabric					
IMSUs	Switching	746	1085	1420	Time Switch
IMSUs	Bypass	2	2	2	
CCB	all modes	2	2	2	
Glue to system ingress CML		2	2	2	
Egress Switch Fabric					
EMSUs	Switching	746	1085	1420	Time Switch
EMSUs	Bypass	2	2	2	
CCB	all modes	2	2	2	
Glue to Egress HPOH	all modes	1	1	1	
PP Subsystem					
RTOP, VTPI, RTTB, glue	all modes	28	28	28	
VTPA	VT1.5	373	1495	1869	Depends on alignment FIFO
	VT2	278	1110	1389	Depends on alignment FIFO
	VT3	182	733	917	Depends on alignment FIFO
	VT6	90	363	454	Depends on alignment FIFO
	TU3	13	90	90	Depends on alignment FIFO

	Mode	Min No. of Clocks	Nom No. of Clocks	Max No. of Clocks	Notes
SVCA	all modes	91	175	257	Depends on alignment FIFO
System Egress Receive CML					
glue, RILC, RSEF	all modes	15	15	15	
align FIFO	all modes	1	8	16	
tim_fifo	all modes	1	4	8	
SERDES	all modes	1	2	2	
System Ingress Transmit CML					
glue, TILC, TSEC	all modes	12	12	12	
tim_fifo	all modes	1	4	8	
SERDES	all modes	1	2	2	
Line Ingress Receive CML					
glue	all modes	1	1	1	
SERDES	all modes	1	2	2	
RSEF	777/622	11	11	11	
align_fifo	777/622	5	21	37	Depth user configurable
RSEF	2488	11	11	11	311MHz clock
dmux FIFO	2488	5	121	37	Depth user configurable
Line Egress Transmit CML					
glue		2	2	2	
SERDES	all modes	1	2	2	
tim_fifo	777/622	1	4	8	
TSEC	777/622	8	8	8	
Mux FIFO	777/622	0	0	0	
tim_fifo	2488	1	4	8	311MHz clock
TSEC	2488	8	8	8	311MHz clock
Mux FIFO	2488	1	4	8	311MHz clock

10.10.1 Latency for the Different Modes of Operation

Device latency estimates assume the following:

- RASIO™ CML (777/622) is being used on the line side. If line ingress uses parallel bus in, latency figures are reduced by 0.488 µs in the ingress path. If line egress uses parallel out, latency figures are reduced by 0.257 µs in the egress path.
- STSI blocks are switching giving STSI subsystems 206 ns latency.
- Figures quoted for VT-level traffic are for VT1.5 as this is the worst case.

- Two sets of figures are shown in applications where MSU-Lites are used – when the MSU-Lites are in 1:1 configuration; i.e. data goes out the same order it came in, and when they are doing extreme switching; i.e. the first tributary in is the last tributary out.

Notes on VTPA

1. VTPA latency of 19.23 µs for VT1.5 is the steady state delay through VTPA. This will increase momentarily to a delay of 24.03 µs during negative justification events until the corresponding negative pointer movement can be performed. Once an incoming negative pointer movement is detected, VTPA can't begin an outgoing one until the beginning of the next multiframe (V1 byte) and the effect of the schedule movement does not take place until the V3 byte.
2. The above assumes that the aggregate incoming high order and low order justification rate per tributary is no more than one every four multiframes.
3. For out of tolerance justification rates (i.e. more than one justification every four multiframes), latency through VTPA will be more than 24.03 µs.
4. In the following calculations, the steady state delay of 19.23 µs through the VTPA was used.

Notes on MSU-Lite

1. Max switching delay of 18.26 µs through MSU-Lite assumes that VT-level switching is being performed. 18.26 µs corresponds to 1.33 rows of the STS-12 frame. If full column switching is performed i.e. the order of the columns inside a VT is allowed to change, then max delay through MSU-Lite would be 26.9 µs i.e. approx 2 rows of the STS-12 frame.
2. In the following calculations, max delay of 18.26 µs was used through MSU-Lite for MSU switching configurations.
3. In the hairpinning case, max delay through one MSU-Lite (1.33 rows) and nominal delay through the other MSU-Lite (1 row) was used.

Table 17 Latency for Different Modes of Operation

Data path	MSU-Lite Not Switching (in µs)	MSU-Lite Switching (in µs)	Application
VT1.5 traffic from line ingress to system ingress	34.607	38.915	ADM
STS-1 bypass traffic from line ingress to system ingress	18.686	22.991	ADM
VT1.5 and STS-1 traffic from system egress to line egress	18.421	22.741	ADM
VT1.5 traffic from line ingress to line egress in payload processing loopback (no MSU-Lites used). Parallel I/Os	19.869	N/A	Pure Payload Processing
STS-1 bypass traffic from line ingress to line egress in payload processing Loopback (no MSU-Lites used). Parallel I/Os	5.318	N/A	Pure Payload Processing
VT1.5 traffic from line ingress to line egress in hairpinning - ingress and egress msu-lites used	52.761	57.1	Hair-pinning
STS-1 traffic from line ingress to line egress in hairpinning - ingress and egress msu-lites used	36.523	40.843	Hair-pinning

10.11 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The TUPP 2488 identification code is 0x153640CD hexadecimal.

10.12 DLL

The DLL in TUPP 2488 ensures that the REFCLK pin and clocks to internal logic are aligned correctly.

10.13 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the TUPP 2488 to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the TUPP 2488 while the test mode registers are used to enhance the testability of the TUPP 2488. The register set is accessed as shown in Table 18.

Memory addresses that are not shown are not used and must be treated as Reserved.

Table 18 TUPP 2488 Memory Map

0000-00FF								Master Registers
STSI Subsystem								
0100-0107								Ingress STSI (Working)
0108-010F								Ingress STSI (Protect)
0110-0113								Egress STSI (Working)
0118-011B								Egress STSI (Protect)
0115-0117								SOH Overwrite (working)
011C-011F								SOH Overwrite (protect)
0120-0123								DLL
SF Subsystem								
MSU #1	**MSU #2**	**MSU #3**	**MSU #4**	**MSU #5**	**MSU #6**	**MSU #7**	**MSU #8**	
0200-020F	0210-021F	0220-022F	0230-023F	0240-024F	0250-025F	0260-026F	0270-027F	Ingress MSULite
0280-029F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	CCB
MSU #9	**MSU #10**	**MSU #11**	**MSU #12**	**MSU #13**	**MSU #14**	**MSU #15**	**MSU #16**	
0300-030F	0310-031F	0320-032F	0330-033F	0340-034F	0350-035F	0360-036F	0370-037F	Egress MSULite
LSCML Subsystem								
Link #1	**Link #2**	**Link #3**	**Link #4**	**Link #5**	**Link #6**	**Link #7**	**Link #8**	
0800-0807	0A00-0A07	0C00-0C07	0E00-0E07	N/A	N/A	N/A	N/A	Line Side RSEF (Working)
0808-080F	0A08-0A0F	0C08-0C0F	0E08-0E0F	N/A	N/A	N/A	N/A	Line Side RSEF (Protect)
0810-0813	0A10-0A13	0C10-0C13	0E10-0E13	N/A	N/A	N/A	N/A	Line Side PIPM (Working)
0818-081B	0A18-0A1B	0C18-0C1B	0E18-0E1B	N/A	N/A	N/A	N/A	Line Side PIPM (Protect)
0820-083F	0A20-0A3F	0C20-0C3F	0E20-0E3F	N/A	N/A	N/A	N/A	Line Side Receive Slice
0860-086F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Line Side CSU Interface (CSUI)
0900-0903	0B00-0B03	0D00-0D03	0F00-0F03	N/A	N/A	N/A	N/A	Line Side TSEC (Working)
0908-090B	0B08-0B0B	0D08-0D0B	0F08-0F0B	N/A	N/A	N/A	N/A	Line Side TSEC (Protect)
0910-091F	0B10-0B1F	0D10-0D1F	0F10-0F1F	N/A	N/A	N/A	N/A	Line Side Transmit Slice
SSCML Subsystem								
Links #1,2 working	**Link #3,4 working**	**Link #5,6 working**	**Link #7,8 working**	**Link #1,2 protect**	**Link #3,4 protect**	**Link #5,6 protect**	**Link #7,8 protect**	

1000-1007	1200-1207	1400-1407	1600-1607	1800-1807	1A00-1A07	1C00-1C07	1E00-1E07	System Side RSEF
1008-100F	1208-120F	1408-140F	1608-160F	1808-180F	1A08-1A0F	1C08-1C0F	1E08-1E0F	System Side RSEF
1010-1013	1210-1213	1410-1413	1610-1613	1810-1813	1A10-1A13	1C10-1C13	1E10-1E13	System Side PIPM
1018-101B	1218-121B	1418-141B	1618-161B	1818-181B	1A18-1A1B	1C18-1C1B	1E18-1E1B	System Side PIPM
1020-103F	1220-123F	1420-143F	1620-163F	1820-183F	1A20-1A3F	1C20-1C3F	1E20-1E3F	System Side Receive Slice
1040-104F	1240-124F	1440-144F	1640-164F	1840-184F	1A40-1A4F	1C40-1C4F	1E40-1E4F	System Side RILC
1050-105F	1250-125F	1450-145F	1650-165F	1850-185F	1A50-1A5F	1C50-1C5F	1E50-1E5F	System Side RILC
1060-106F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	System Side CSU Interface (CSUI)
1100-1103	1300-1303	1500-1503	1700-1703	1900-1903	1B00-1B03	1D00-1D03	1F00-1F03	System Side TSEC
1108-110B	1308-130B	1508-150B	1708-170B	1908-190B	1B08-1B0B	1D08-1D0B	1F08-1F0B	System Side TSEC
1110-111F	1310-131F	1510-151F	1710-171F	1910-191F	1B10-1B1F	1D10-1D1F	1F10-1F1F	System Side Transmit Slice
1120-112F	1320-132F	1520-152F	1720-172F	1920-192F	1B20-1B2F	1D20-1D2F	1F20-1F2F	System Side TILC
1130-113F	1330-133F	1530-153F	1730-173F	1930-193F	1B30-1B3F	1D30-1D3F	1F30-1F3F	System Side TILC
Egress Data path								
STS-12 #1	**STS-12 #2**	**STS-12 #3**	**STS-12 #4**					
2000-207F	2200-227F	2400-247F	2600-267F	N/A	N/A	N/A	N/A	SHPI
2080-208F	2280-228F	2480-248F	2680-268F	N/A	N/A	N/A	N/A	Egress SVCA
HPOH Subsystem								
HPOH #1	**HPOH #2**	**HPOH #3**	**HPOH #4**					
2100-217F	2300-237F	2500-257F	2700-277F	N/A	N/A	N/A	N/A	HPOH RHPP_R
2180-2187	2380-2387	2580-2587	2780-2787	N/A	N/A	N/A	N/A	HPOH RTTP
2190-219F	2390-239F	2590-259F	2790-279F	N/A	N/A	N/A	N/A	HPOH THPP_R
21A0-21A3	23A0-23A3	25A0-25A3	27A0-27A3	N/A	N/A	N/A	N/A	HPOH TTTP
21C0-21DF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	HPOH SARC-48
PP Subsystem								
PP #1	**PP #2**	**PP #3**	**PP #4**					
3000-307F	3200-327F	3400-347F	3600-367F	N/A	N/A	N/A	N/A	Payload Processor RTOP336
3080-30FF	3280-32FF	3480-34FF	3680-36FF	N/A	N/A	N/A	N/A	Payload Processor VTPI
3100-313F	3300-333F	3500-353F	3700-373F	N/A	N/A	N/A	N/A	Payload

								Processor RTTB336
3140-317F	3340-337F	3540-357F	3740-377F	N/A	N/A	N/A	N/A	Payload Processor VTPA
3180-31BF	3380-33BF	3580-35BF	3780-37BF	N/A	N/A	N/A	N/A	Payload Processor TASR
31C0-31EF	33C0-33EF	35C0-35EF	37C0-37EF	N/A	N/A	N/A	N/A	Payload Processor TBER
31F0-31FF	33F0-33FF	35F0-35FF	37F0-37FF	N/A	N/A	N/A	N/A	Ingress SVCA

Notes on Register Memory Map

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the TUPP. Normal mode registers (as opposed to test mode registers) are selected when A[14] is set low.

Notes on Normal Mode Registers

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the functional block to determine the programming state of the block.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect TUPP operation unless otherwise noted.

11.1 Device-Level Registers

Table 19 Device-Level Registers

Address	Mnemonic	Register
0000	MSTR_RST1	TUPP Master Reset #1
0001	MSTR_RST2	TUPP Master Reset #2
0002	MSTR_RST3	TUPP Master Reset #3
0003	JTAG_ID1	JTAG ID #1
0004	JTAG_ID2	JTAG ID #2
0005	MSTR_INTSRC1	TUPP Master Interrupt Source #1
0006	MSTR_INTSRC2	TUPP Master Interrupt Source #2
0007	MSTR_INTSRC3	TUPP Master Interrupt Source #3
0008	MSTR_INTSRC4	TUPP Master Interrupt Source #4
0009	MSTR_INTSRC5	TUPP Master Interrupt Source #5
000A	MSTR_INTSRC6	TUPP Master Interrupt Source #6
000B	MSTR_INTSRC7	TUPP Master Interrupt Source #7
000C	MSTR_INTSRC8	TUPP Master Interrupt Source #8
000D	MINTE	Master Device Interrupt Enable
000E	MSTR_INTEN1	TUPP Master Interrupt Enable #1
000F	MSTR_INTEN2	TUPP Master Interrupt Enable #2
0010	MSTR_INTEN3	TUPP Master Interrupt Enable #3
0011	MSTR_INTEN4	TUPP Master Interrupt Enable #4
0012	MSTR_INTEN5	TUPP Master Interrupt Enable #5
0013	MSTR_INTEN6	TUPP Master Interrupt Enable #6
0014	MSTR_INTEN7	TUPP Master Interrupt Enable #7
0015	MSTR_INTEN8	TUPP Master Interrupt Enable #8
0016	MSTRDPCTRL	Master Data path Control Register
0017	CML_CTRL	CML Control Register
0018	LTPARCTRL	Line Side Telecom Bus Parity control
0019	LISDLY	Line Ingress System Reference Delay
001A	STSIMDCTRL	STSI Mode Control
001B	ESVCA_DLY	Egress SVCA Frame Alignment Delay Register
001C	IMON	Input Monitor Register
001D	PMON	Performance Monitor Control and Status Register
001E	WCIMODE_CFG	WCIMODE Configuration Register
001F	TUPP_IO_CFG	TUPP I/O Configuration Register
0020	HPOH_RCFG	HPOH Receive Configuration
0021	HPOH_TCFG	HPOH Transmit Configuration

Address	Mnemonic	Register
0022, 0023, 0024, 0025	HPOH_TAPC	HPOH Transmit Alarm Preprocessing Configuration #1-#4
0026	HPOH_T3C	HPOH Transmit STS3c Configuration
0030	SF_CTRL1	Switch Fabric Control Register #1
0031	SF_CTRL2	Switch Fabric Control Register #2
0032	SF_CTRL3	Switch Fabric Control Register #3
0033	SF_CTRL4	Switch Fabric Control Register #4
0034	SESDLY	System Egress System Reference Delay
0040, 0060, 0080, 00A0	VTPICFGn	VTPI Configuration and Status
0041, 0061, 0081, 00A1	VTPIFRMCFGn	VTPI Frame Configuration
0042, 0062, 0082, 00A2	RIGCFGn	RIG Configuration
0044, 0064, 0084, 00A4	TRIBFRMCFGn	Tributary Frame Configuration
0046, 0066, 0086, 00A6	VTPACFGn	VTPA Configuration and Status
0047, 0067, 0087, 00A7	VTPAIFRMCFGn	VTPA Incoming Frame Configuration
0048, 0068, 0088, 00A8	VTPAOFRMCFGn	VTPA Outgoing Frame Configuration
004A, 006A, 008A, 00AA	VIGCFGn	VIG Configuration
004B, 006B, 008B, 00AB	SIGCFGn	SIG Configuration
004D, 006D, 008D, 00AD	TRIBBYMUXCFGn	Tributary-Bypass Mux Configuration and Status
004F, 006F, 008F, 00AF	PPLOMSTS	PP Loss of Multiframe Status
00C0	PTILCP	Protect Transmit ILC Page
00C1	WTILCP	Working Transmit ILC Page
00C2	TILCUB0	Transmit ILC User Bit 0
00C3	TILCUB1	Transmit ILC User Bit 1
00C4	TILCUB2	Transmit ILC User Bit 2
00C5	PRILCP	Protect Receive ILC Page
00C6	WRILCP	Working Receive ILC Page
00C7	RILCRUB0	Receive ILC User Bit 0

Address	Mnemonic	Register
00C8	RILCRUB1	Receive ILC User Bit 1
00C9	RILCRUB2	Receive ILC User Bit 2
00F0	Reserved	
00F1	Reserved	
00F2	Reserved	
00F3	Reserved	
00F4	Reserved	
00F5	Reserved1	
00FF	Reserved2	

The entire normal mode register description is available in PMC-2020188, “TUPP 2488 Register Description Document.”

12 Test Features Description

Asserting (low) RSTB causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TUPP 2488. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[14]) is high.

The TUPP 2488 supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 20 Test Mode Register Memory Map

Address	Register
0000H-3FFFH	Normal Mode Registers
4000H-7FFFH	Master Test

12.1 Master Test and Test Configuration Registers

Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 4000H: TUPP Master Test

Bit	Type	Function	Default
Bit 15:5	R	Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	Reserved	X
Bit 2	W	DBCTRL	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable TUPP 2488 test features. PMCTST is reset when CSB is high. PMCTST can also be reset by writing a logic 0 to the corresponding register bit.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the TUPP. While the HIZIO bit is a logic one, all output pins of the TUPP except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and PMCTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the TUPP to drive the data bus and holding the CSB pin high tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

Reserved

This bit must remain at ‘0’ for normal operation.

PMCTST

The PMCTST bit is used to configure the TUPP for PMC's manufacturing tests. When PMCTST is set to logic one, the TUPP microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. As well, the analog blocks are placed in IDDQ mode = the digital circuitry within the analog blocks is held static The PMCTST bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Register 4001H: TUPP Master Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15:14	R	Unused	X
Bit 13	R/W	TM_A_EN[13]	X
Bit 12	R/W	TM_A_EN[12]	X
Bit 11	R/W	TM_A_EN[11]	X
Bit 10	R/W	TM_A_EN[10]	X
Bit 9	R/W	TM_A_EN[9]	X
Bit 8	R/W	TM_A_EN[8]	X
Bit 7	R/W	TM_A_EN[7]	X
Bit 6	R/W	TM_A_EN[6]	X
Bit 5	R/W	TM_A_EN[5]	X
Bit 4	R/W	TM_A_EN[4]	X
Bit 3	R/W	TM_A_EN[3]	X
Bit 1	R/W	TM_A_EN[2]	X
Bit 1	R/W	TM_A_EN[1]	X
Bit 0	R/W	TM_A_EN[0]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST is set to logic 1 and provided A[14:8] is not “0000000” (within the TUPP master register address range). The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

TM_A_EN[13:0]

When TM_A_EN[X] is logic 1 and PMCTST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST, TM_A_EN[13:0] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 4002H: TUPP Master Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15:14	R	Unused	X
Bit 13	R/W	TM_A[13]	X
Bit 12	R/W	TM_A[12]	X
Bit 11	R/W	TM_A[11]	X
Bit 10	R/W	TM_A[10]	X
Bit 9	R/W	TM_A[9]	X
Bit 8	R/W	TM_A[8]	X
Bit 7	R/W	TM_A[7]	X
Bit 6	R/W	TM_A[6]	X
Bit 5	R/W	TM_A[5]	X
Bit 4	R/W	TM_A[4]	X
Bit 3	R/W	TM_A[3]	X
Bit 2	R/W	TM_A[2]	X
Bit 1	R/W	TM_A[1]	X
Bit 0	R/W	TM_A[0]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

TM_A[13:0]

When TM_A_EN[X] is logic 1 and PMCTST is logic 1, the TM_A[X] bit replaces the input pin A[X]. The TM_A[X] bits are not cleared on reset. TM_A[13:0] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 400AH: TUPP Misc Test Write Register

Bit	Type	Function	Default
Bit 15:1	R	Unused	X
Bit 0	W	STS48_EN_TST	0

This register is used to enable miscellaneous TUPP 2488 test features.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

STS48_EN_TST

The STS48_EN_TST bit controls the line side CML configuration of the TUPP 2488 while in test mode. When STS48_EN_TST is a ‘1’ in test mode the line side CML subsystem is configured for the STS-48 (2.488 G/Sec) operation

Register 4010H: TUPP Misc Test Read Register

Bit	Type	Function	Default
Bit 15:1	R	Unused	X
Bit 0	R	STS48_EN_TST	0

This register is used to enable miscellaneous TUPP 2488 test features.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

STS48_EN_TST

The STS48_EN_TST bit controls the line side CML configuration of the TUPP 2488 while in test mode. When STS48_EN_TST is a ‘1’ in test mode the line side CML subsystem is configured for the STS-48 (2.488 G/Sec) operation

12.2 JTAG Test Port

The TUPP JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, refer to the Operation Section (Section 13).

Table 21 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 22 Identification Register

Length	32 bits
Version Number	1H
Part Number – TUPP 2488	5364H
Manufacturer's Identification Code	0CDH
Device Identification – TUPP 2488	053640CDH

Table 23 Boundary Scan Register

Name	Register Bit	Cell Type
A[11]	352	IN_CELL
A[10]	351	IN_CELL
A[9]	350	IN_CELL
A[8]	349	IN_CELL
A[7]	348	IN_CELL
A[6]	347	IN_CELL
A[5]	346	IN_CELL
A[4]	345	IN_CELL
A[3]	344	IN_CELL
A[2]	343	IN_CELL
A[1]	342	IN_CELL
A[0]	341	IN_CELL
OEB_D[15]	340	OUT_CELL
D[15]	339	IO_CELL
OEB_D[14]	338	OUT_CELL
D[14]	337	IO_CELL
OEB_D[13]	336	OUT_CELL
D[13]	335	IO_CELL
OEB_D[12]	334	OUT_CELL
D[12]	333	IO_CELL

Name	Register Bit	Cell Type
OEB_D[11]	332	OUT_CELL
D[11]	331	IO_CELL
OEB_D[10]	330	OUT_CELL
D[10]	329	IO_CELL
OEB_D[9]	328	OUT_CELL
D[9]	327	IO_CELL
OEB_D[8]	326	OUT_CELL
D[8]	325	IO_CELL
OEB_D[7]	324	OUT_CELL
D[7]	323	IO_CELL
OEB_D[6]	322	OUT_CELL
D[6]	321	IO_CELL
OEB_D[5]	320	OUT_CELL
D[5]	319	IO_CELL
OEB_D[4]	318	OUT_CELL
D[4]	317	IO_CELL
OEB_D[3]	316	OUT_CELL
D[3]	315	IO_CELL
OEB_D[2]	314	OUT_CELL
D[2]	313	IO_CELL
OEB_D[1]	312	OUT_CELL
D[1]	311	IO_CELL
OEB_D[0]	310	OUT_CELL
D[0]	309	IO_CELL
OEB_INTB	308	OUT_CELL
INTB	307	OUT_CELL
OEB_TPOH[4]	306	OUT_CELL
TPOH[4]	305	OUT_CELL
OEB_TPOHEN[4]	304	OUT_CELL
TPOHEN[4]	303	OUT_CELL
OEB_TPOHFP[4]	302	OUT_CELL
TPOHFP[4]	301	OUT_CELL
OEB_TRAD[4]	300	OUT_CELL
TRAD[4]	299	OUT_CELL
OEB_TPOH[3]	298	OUT_CELL
TPOH[3]	297	OUT_CELL
OEB_TPOHEN[3]	296	OUT_CELL
TPOHEN[3]	295	OUT_CELL
OEB_TPOHFP[3]	294	OUT_CELL

Name	Register Bit	Cell Type
TPOHFP[3]	293	OUT_CELL
OEB_TRAD[3]	292	OUT_CELL
TRAD[3]	291	OUT_CELL
OEB_TPOH[2]	290	OUT_CELL
TPOH[2]	289	OUT_CELL
OEB_TPOHEN[2]	288	OUT_CELL
TPOHEN[2]	287	OUT_CELL
OEB_TPOHFP[2]	286	OUT_CELL
TPOHFP[2]	285	OUT_CELL
OEB_TRAD[2]	284	OUT_CELL
TRAD[2]	283	OUT_CELL
OEB_TPOH[1]	282	OUT_CELL
TPOH[1]	281	OUT_CELL
OEB_TPOHEN[1]	280	OUT_CELL
TPOHEN[1]	279	OUT_CELL
OEB_TPOHFP[1]	278	OUT_CELL
TPOHFP[1]	277	OUT_CELL
OEB_TRAD[1]	276	OUT_CELL
TRAD[1]	275	OUT_CELL
OEB_HPOHCLK	274	OUT_CELL
HPOHCLK	273	OUT_CELL
OEB_HPOHFP	272	OUT_CELL
HPOHFP	271	OUT_CELL
OEB_HRPOH[4]	270	OUT_CELL
HRPOH[4]	269	OUT_CELL
OEB_HRPOHEN[4]	268	OUT_CELL
HRPOHEN[4]	267	OUT_CELL
OEB_HB3E[4]	266	OUT_CELL
HB3E[4]	265	OUT_CELL
OEB_HRPOH[3]	264	OUT_CELL
HRPOH[3]	263	OUT_CELL
OEB_HRPOHEN[3]	262	OUT_CELL
HRPOHEN[3]	261	OUT_CELL
OEB_HB3E[3]	260	OUT_CELL
HB3E[3]	259	OUT_CELL
OEB_HRPOH[2]	258	OUT_CELL
HRPOH[2]	257	OUT_CELL
OEB_HRPOHEN[2]	256	OUT_CELL
HRPOHEN[2]	255	OUT_CELL

Name	Register Bit	Cell Type
OEB_HB3E[2]	254	OUT_CELL
HB3E[2]	253	OUT_CELL
OEB_HRPOH[1]	252	OUT_CELL
HRPOH[1]	251	OUT_CELL
OEB_HRPOHEN[1]	250	OUT_CELL
HRPOHEN[1]	249	OUT_CELL
OEB_HB3E[1]	248	OUT_CELL
HB3E[1]	247	OUT_CELL
IDATA_4[7]	246	IN_CELL
IDATA_4[6]	245	IN_CELL
IDATA_4[5]	244	IN_CELL
IDATA_4[4]	243	IN_CELL
IDATA_4[3]	242	IN_CELL
IDATA_4[2]	241	IN_CELL
IDATA_4[1]	240	IN_CELL
IDATA_4[0]	239	IN_CELL
IDP[4]	238	IN_CELL
IPL[4]	237	IN_CELL
IJ0J1[4]	236	IN_CELL
IPAIS[4]	235	IN_CELL
IDATA_3[7]	234	IN_CELL
IDATA_3[6]	233	IN_CELL
IDATA_3[5]	232	IN_CELL
IDATA_3[4]	231	IN_CELL
IDATA_3[3]	230	IN_CELL
IDATA_3[2]	229	IN_CELL
IDATA_3[1]	228	IN_CELL
IDATA_3[0]	227	IN_CELL
IDP[3]	226	IN_CELL
IPL[3]	225	IN_CELL
IJ0J1[3]	224	IN_CELL
IPAIS[3]	223	IN_CELL
IDATA_2[7]	222	IN_CELL
IDATA_2[6]	221	IN_CELL
IDATA_2[5]	220	IN_CELL
IDATA_2[4]	219	IN_CELL
IDATA_2[3]	218	IN_CELL
IDATA_2[2]	217	IN_CELL
IDATA_2[1]	216	IN_CELL

Name	Register Bit	Cell Type
IDATA_2[0]	215	IN_CELL
IDP[2]	214	IN_CELL
IPL[2]	213	IN_CELL
IJ0J1[2]	212	IN_CELL
IPAIS[2]	211	IN_CELL
IDATA_1[7]	210	IN_CELL
IDATA_1[6]	209	IN_CELL
IDATA_1[5]	208	IN_CELL
IDATA_1[4]	207	IN_CELL
IDATA_1[3]	206	IN_CELL
IDATA_1[2]	205	IN_CELL
IDATA_1[1]	204	IN_CELL
IDATA_1[0]	203	IN_CELL
IDP[1]	202	IN_CELL
IPL[1]	201	IN_CELL
IJ0J1[1]	200	IN_CELL
IPAIS[1]	199	IN_CELL
IJ0	198	IN_CELL
LIWSEL	197	IN_CELL
LICMP	196	IN_CELL
LECMP	195	IN_CELL
LIPROT[4]	194	IN_CELL
LIWORK[4]	193	IN_CELL
LIPROT[3]	192	IN_CELL
LIWORK[3]	191	IN_CELL
LIPROT[2]	190	IN_CELL
LIWORK[2]	189	IN_CELL
LIPROT[1]	188	IN_CELL
LIWORK[1]	187	IN_CELL
LEPROT[1]	186	OUT_CELL
LEWORK[1]	185	OUT_CELL
LEPROT[2]	184	OUT_CELL
LEWORK[2]	183	OUT_CELL
LEPROT[3]	182	OUT_CELL
LEWORK[3]	181	OUT_CELL
LEPROT[4]	180	OUT_CELL
LEWORK[4]	179	OUT_CELL
LOSC	178	OUT_CELL
LREFCLK	177	IN_CELL

Name	Register Bit	Cell Type
OEB_EDATA_4[7]	176	OUT_CELL
EDATA_4[7]	175	OUT_CELL
OEB_EDATA_4[6]	174	OUT_CELL
EDATA_4[6]	173	OUT_CELL
OEB_EDATA_4[5]	172	OUT_CELL
EDATA_4[5]	171	OUT_CELL
OEB_EDATA_4[4]	170	OUT_CELL
EDATA_4[4]	169	OUT_CELL
OEB_EDATA_4[3]	168	OUT_CELL
EDATA_4[3]	167	OUT_CELL
OEB_EDATA_4[2]	166	OUT_CELL
EDATA_4[2]	165	OUT_CELL
OEB_EDATA_4[1]	164	OUT_CELL
EDATA_4[1]	163	OUT_CELL
OEB_EDATA_4[0]	162	OUT_CELL
EDATA_4[0]	161	OUT_CELL
OEB_EDP[4]	160	OUT_CELL
EDP[4]	159	OUT_CELL
OEB_EPL[4]	158	OUT_CELL
EPL[4]	157	OUT_CELL
OEB_EJ0J1[4]	156	OUT_CELL
EJ0J1[4]	155	OUT_CELL
OEB_EAIS[4]	154	OUT_CELL
EAIS[4]	153	OUT_CELL
OEB_ETPL_HTPOH[4]	152	OUT_CELL
ETPL_HTPOH[4]	151	IO_CELL
OEB_EV5_HTPOHRDY[4]	150	OUT_CELL
EV5_HTPOHRDY[4]	149	OUT_CELL
OEB_EIDLE_HTPOHEN[4]	148	OUT_CELL
EIDLE_HTPOHEN[4]	147	IO_CELL
OEB_EDATA_3[7]	146	OUT_CELL
EDATA_3[7]	145	OUT_CELL
OEB_EDATA_3[6]	144	OUT_CELL
EDATA_3[6]	143	OUT_CELL
OEB_EDATA_3[5]	142	OUT_CELL
EDATA_3[5]	141	OUT_CELL
OEB_EDATA_3[4]	140	OUT_CELL
EDATA_3[4]	139	OUT_CELL
OEB_EDATA_3[3]	138	OUT_CELL

Name	Register Bit	Cell Type
EDATA_3[3]	137	OUT_CELL
OEB_EDATA_3[2]	136	OUT_CELL
EDATA_3[2]	135	OUT_CELL
OEB_EDATA_3[1]	134	OUT_CELL
EDATA_3[1]	133	OUT_CELL
OEB_EDATA_3[0]	132	OUT_CELL
EDATA_3[0]	131	OUT_CELL
OEB_EDP[3]	130	OUT_CELL
EDP[3]	129	OUT_CELL
OEB_EPL[3]	128	OUT_CELL
EPL[3]	127	OUT_CELL
OEB_EJ0J1[3]	126	OUT_CELL
EJ0J1[3]	125	OUT_CELL
OEB_EAIS[3]	124	OUT_CELL
EAIS[3]	123	OUT_CELL
OEB_ETPL_HTPOH[3]	122	OUT_CELL
ETPL_HTPOH[3]	121	IO_CELL
OEB_EV5_HTPOHRDY[3]	120	OUT_CELL
EV5_HTPOHRDY[3]	119	OUT_CELL
OEB_EIDLE_HTPOHEN[3]	118	OUT_CELL
EIDLE_HTPOHEN[3]	117	IO_CELL
OEB_EDATA_2[7]	116	OUT_CELL
EDATA_2[7]	115	OUT_CELL
REFCLK	114	IN_CELL
OEB_EDATA_2[6]	113	OUT_CELL
EDATA_2[6]	112	OUT_CELL
OEB_EDATA_2[5]	111	OUT_CELL
EDATA_2[5]	110	OUT_CELL
OEB_EDATA_2[4]	109	OUT_CELL
EDATA_2[4]	108	OUT_CELL
OEB_EDATA_2[3]	107	OUT_CELL
EDATA_2[3]	106	OUT_CELL
OEB_EDATA_2[2]	105	OUT_CELL
EDATA_2[2]	104	OUT_CELL
OEB_EDATA_2[1]	103	OUT_CELL
EDATA_2[1]	102	OUT_CELL
OEB_EDATA_2[0]	101	OUT_CELL
EDATA_2[0]	100	OUT_CELL
OEB_EDP[2]	99	OUT_CELL

Name	Register Bit	Cell Type
EDP[2]	98	OUT_CELL
OEB_EPL[2]	97	OUT_CELL
EPL[2]	96	OUT_CELL
OEB_EJ0J1[2]	95	OUT_CELL
EJ0J1[2]	94	OUT_CELL
OEB_EAIS[2]	93	OUT_CELL
EAIS[2]	92	OUT_CELL
OEB_ETPL_HTPOH[2]	91	OUT_CELL
ETPL_HTPOH[2]	90	IO_CELL
OEB_EV5_HTPOHRDY[2]	89	OUT_CELL
EV5_HTPOHRDY[2]	88	OUT_CELL
OEB_EIDLE_HTPOHEN[2]	87	OUT_CELL
EIDLE_HTPOHEN[2]	86	IO_CELL
OEB_EDATA_1[7]	85	OUT_CELL
EDATA_1[7]	84	OUT_CELL
OEB_EDATA_1[6]	83	OUT_CELL
EDATA_1[6]	82	OUT_CELL
OEB_EDATA_1[5]	81	OUT_CELL
EDATA_1[5]	80	OUT_CELL
OEB_EDATA_1[4]	79	OUT_CELL
EDATA_1[4]	78	OUT_CELL
OEB_EDATA_1[3]	77	OUT_CELL
EDATA_1[3]	76	OUT_CELL
OEB_EDATA_1[2]	75	OUT_CELL
EDATA_1[2]	74	OUT_CELL
OEB_EDATA_1[1]	73	OUT_CELL
EDATA_1[1]	72	OUT_CELL
OEB_EDATA_1[0]	71	OUT_CELL
EDATA_1[0]	70	OUT_CELL
OEB_EDP[1]	69	OUT_CELL
EDP[1]	68	OUT_CELL
OEB_EPL[1]	67	OUT_CELL
EPL[1]	66	OUT_CELL
OEB_EJ0J1[1]	65	OUT_CELL
EJ0J1[1]	64	OUT_CELL
OEB_EAIS[1]	63	OUT_CELL
EAIS[1]	62	OUT_CELL
OEB_ETPL_HTPOH[1]	61	OUT_CELL
ETPL_HTPOH[1]	60	IO_CELL

Name	Register Bit	Cell Type
OEB_EV5_HTPOHRDY[1]	59	OUT_CELL
EV5_HTPOHRDY[1]	58	OUT_CELL
OEB_EIDLE_HTPOHEN[1]	57	OUT_CELL
EIDLE_HTPOHEN[1]	56	IO_CELL
OEB_HRALMCLK	55	OUT_CELL
HRALMCLK	54	OUT_CELL
OEB_HRALMFP	53	OUT_CELL
HRALMFP	52	OUT_CELL
OEB_HRALM	51	OUT_CELL
HRALM	50	OUT_CELL
LCLK	49	IN_CELL
SECMP	48	IN_CELL
SEWSEL	47	IN_CELL
RSTB	46	IN_CELL
SCANB	45	IN_CELL
BRNDSEL[0]	44	IN_CELL
BRNDSEL[1]	43	IN_CELL
SEWORK[1]	42	IN_CELL
SEWORK[2]	41	IN_CELL
SEWORK[3]	40	IN_CELL
SEWORK[4]	39	IN_CELL
SIWORK[1]	38	OUT_CELL
SIWORK[2]	37	OUT_CELL
SIWORK[3]	36	OUT_CELL
SIWORK[4]	35	OUT_CELL
SEWORK[5]	34	IN_CELL
SEWORK[6]	33	IN_CELL
SEWORK[7]	32	IN_CELL
SEWORK[8]	31	IN_CELL
SIWORK[5]	30	OUT_CELL
SIWORK[6]	29	OUT_CELL
SIWORK[7]	28	OUT_CELL
SIWORK[8]	27	OUT_CELL
SEPROT[1]	26	IN_CELL
SEPROT[2]	25	IN_CELL
SEPROT[3]	24	IN_CELL
SEPROT[4]	23	IN_CELL
SIPROT[1]	22	OUT_CELL
SIPROT[2]	21	OUT_CELL

Name	Register Bit	Cell Type
SIPROT[3]	20	OUT_CELL
SIPROT[4]	19	OUT_CELL
SEPROT[5]	18	IN_CELL
SEPROT[6]	17	IN_CELL
SEPROT[7]	16	IN_CELL
SEPROT[8]	15	IN_CELL
SIPROT[5]	14	OUT_CELL
SIPROT[6]	13	OUT_CELL
SIPROT[7]	12	OUT_CELL
SIPROT[8]	11	OUT_CELL
SOSC	10	OUT_CELL
SREFCLK	9	IN_CELL
EJ0	8	IN_CELL
SICMP	7	IN_CELL
CSB	6	IN_CELL
RDB	5	IN_CELL
WRB	4	IN_CELL
ALE	3	IN_CELL
A[14]	2	IN_CELL
A[13]	1	IN_CELL
A[12]	0	IN_CELL

Notes

1. When set high, INTB will be set to high impedance.
2. Enable cell OEB_pinname, tristates pin pinname when set high.
3. Cells ‘Logic 1’ are Input Observation cells whose input pad is bonded to VDD internally.
4. Register bit 352 is the boundary scan cell closest to TDI (bit 0 is closest to TDO).

12.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 27 Input Observation Cell (IN_CELL)

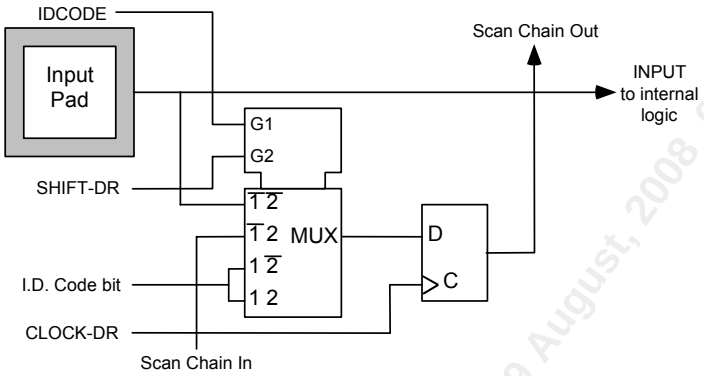


Figure 28 Output Cell (OUT_CELL)

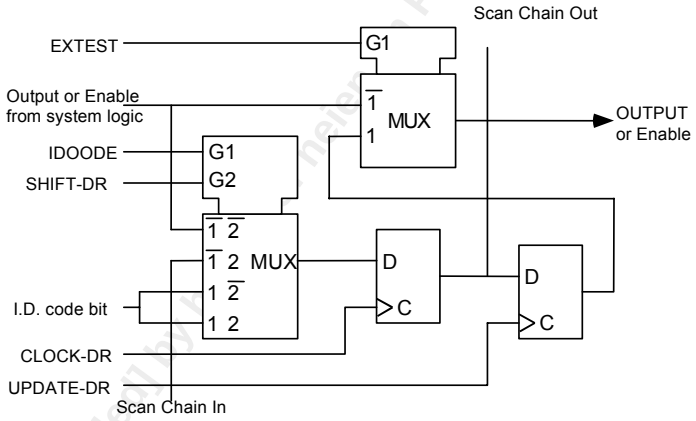


Figure 29 Bidirectional Cell (IO_CELL)

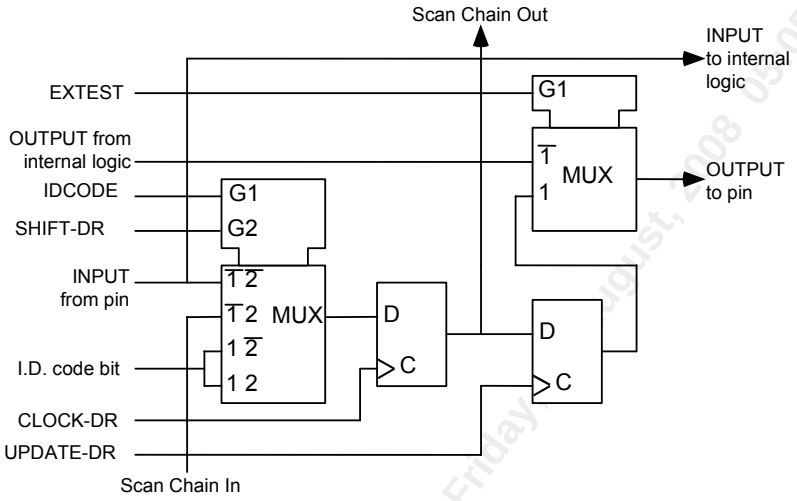
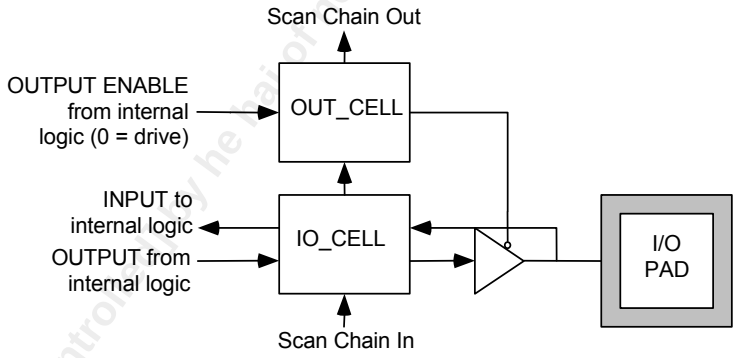


Figure 30 Layout of Output Enable and Bidirectional Cells



13 Operation

There are several important aspects regarding the operation of the TUPP 2488. These are described in detail in the following sections. Example configuration scripts are available in the TUPP 2488 Configuration Guide.

13.1 Configuration Options

The TUPP 2488 carries SDH tributary units (TUs) in an STS-48/STM-16 or four STS-12/STM-4 byte serial data streams. The four streams are each carried in four slices each containing payload processing blocks. Each slice consists of seven blocks: tributary pointer interpreter (VTPI), tributary path overhead processor (RTOP), tributary trace buffer (RTTB), tributary payload aligner (VTPA), SONET/SDH virtual container aligner (SVCA), tributary bit error rate monitor (TBER), and the tributary alarm summary report block (TASR).

Along with the payload processing mentioned above, TUPP 2488 provides STS-1 level switching at its line ingress input and line egress output. On the system side, TUPP 2488 contains eight OC-12 column granularity time switches in each direction. Next to these is an OC-192 column space switch which takes information from both line and system side and also sends information in both directions.

The TUPP 2488 processes High Order Pointer information on its Line Ingress and Transmits High Order Pointer information on its Line Egress.

The TUPP 2488 device passes information on both the line and system side through serial CML blocks. The line side can also work in parallel TelecomBus mode.

The applications of the TUPP 2488 device are facilitated by configuring it for the following:

- Payload Processing Configuration
- ADM using internal crossbar
- ADM using external crossbar
- Hairpinning – internal tributary level Time: Space: Time switching

There are a number of loopbacks and bypasses that may be used within TUPP 2488 for normal operation and also to aid in debug.

OC-12#1 represents the Master OC-12 for TUPP 2488's internal subsystems barring the System CML. In the System CML where there are two sets of OC-48 buses, both OC12-#1 and OC-12#5 are Master Streams.

13.2 Device Reset Procedure & Initialization

Refer to Section 13.13 RASIO™ CML Reset Sequence.

13.3 Reference J0 Pulses

TUPP 2488 passes information in both the ingress and egress directions. Reference J0 pulses are to be supplied for both the Line and System side inputs. IJ0 has a programmable offset from the Line Ingress and EJ0 has a programmable offset for the System Egress. IJ0 is expected every frame and EJ0 is expected every four frames (where a frame is 9720 bytes or one STS-12 SONET frame).

The various programmable delays in TUPP 2488 are summarized in Table 24.

Table 24 Delay Definitions

Delay name	Relative to…	Maximum Value	Comment
LINE_INGRESS_REF_DLY[13:0]	IJ0 (frame-flywheeled version)	1 frame	Delay from IJ0 to J0 arriving out of line ingress RASIO™ CML or arriving at the parallel telecombus input as marked by the IJ0J1 device input.
ESVCA_FRM_ALIGN_DLY [13:0]	IJ0 (frame-flywheeled version)	1 frame	Delay from IJ0 to the output of the egress SVCAs.
PP_ FRM_ALIGN_DLY [15:0]	EJ0 (frame-flywheeled version)	4 frame	Delay from EJ0 to the output of the PP subsystem. Bits 15 and 14 allow up to 3 entire frames of delay to added. Bits 13 to 0 specify the number of refclk cycles for partial frames. Note: that bits 15 and 14 effectively allow a negative delay by advancing nearly 4 frames. For most applications bits 15 and 14 will be 0.
SYSTEM_EGRESS_REF_DLY[15:0]	EJ0 (frame-flywheeled version)	4 frame	Delay from EJ0 to J0 character at input to the egress side of the CCB. (Arriving out of system egress RASIO™ CML). This delay must always be configured as it provides J0 input to the Egress MSU-Lites (two clocks later than SYSTEM_EGRESS_REF_DLY).

13.4 Rate of J0s at Chip I/Os

The line side of TUPP 2488 expects and outputs J0 characters/signals every frame or multiples thereof.

The system side, when configured for 777 MHz TelecomBus mode, can be configured to transmit J0 characters every frame or every four frames. The characters are output every frame when SYSTEM_FRAME_MODE is ‘1’ and every four frames when SYSTEM_FRAME_MODE is ‘0’. EJ0 is always expected every four frames or multiple thereof.

13.5 Controlling the STSI Blocks

These blocks perform full STS-1 level switching (time stage) across a full OC-48 (STS-12/STM-4 serial stream at 77.76 MHz) and lie in both the egress and ingress paths. The desired rearrangement of STS-1s is selected by setting the control pages entries (one per output data stream and timeslot) to the desired input data stream and timeslot.

The timeslot interchange function is implemented with two control pages so that one can be updated while the other is actively used for switching data. The transition of control from one page to the next is synchronized with the beginning of a SONET frame on the data stream to prevent any data loss.

Along with timeslot interchange, the Ingress Working STSIs have a programmable per timeslot output which is used to control working/protect muxes on the line ingress path.

13.5.1 Different Modes

The STSI can operate in any one of four different modes. The mode is set by the SW_MODE register (001Ah) for each STSI. The options are as follows:

SW_MODE = “00”: Normal Mode (Dynamic Switching Mode)

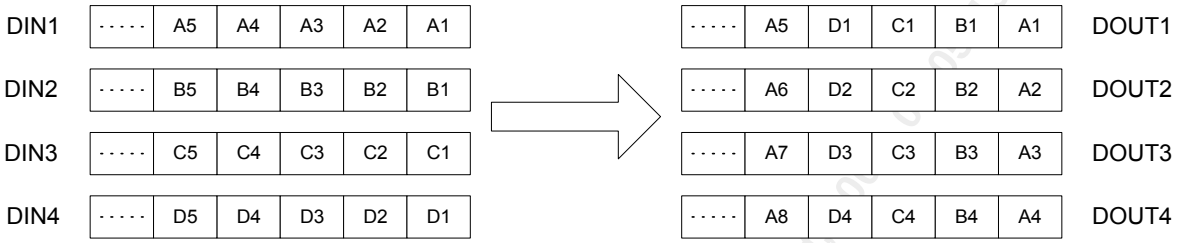
This is normal switching mode where the configuration pages determine where each STS1 is switched.

SW_MODE = “01”: Reserved

SW_MODE = “10”: OC12 - OC48

This mode, illustrated in Figure 31, defines a straight-through timeslot connection, mapping four OC-12 data streams into a single OC-48 data stream. There is no timeslot interchange on the component OC-12 data streams.

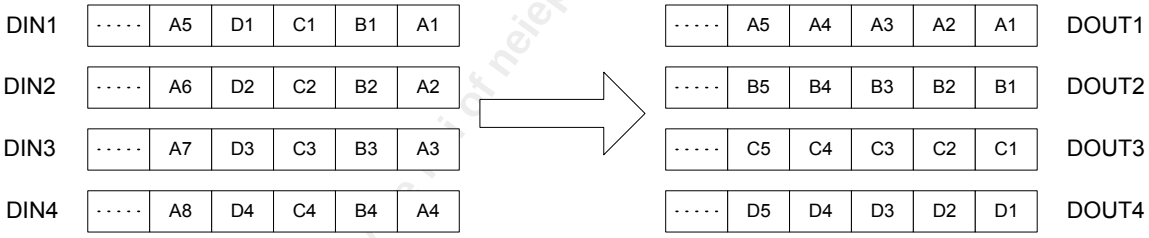
Figure 31 OC-12 to OC-48 Mode



SW_MODE = "11": OC48 - OC12

This mode, illustrated in Figure 32, is the converse of the OC12-OC48 mode. This mode defines a straight-through timeslot connection mapping an OC-48 data stream into its component OC-12 data streams. There is no timeslot interchange on the component OC-12 data streams.

Figure 32 OC-48 to OC-12 Mode



13.5.2 Control Page Accesses

The control page access procedure allows the microprocessor to update or examine the control pages. These control pages determine the output data function, along with programmable outputs (referred to as TSEN in Table 25) controlling the working/protect muxes in the ingress path. This programmable output is not needed in the egress path. This section includes a description of the indirect control page access procedure. The formats of the control page access registers are included as a reference. The data written to the control page access registers determines the switching function and is detailed in the subsequent three sub-sections.

The STSI Indirect Address register format used to access individual control page entries is common to the programmable outputs. These functions are associated with a specific control page entry and that entry is accessed through the STSI Indirect Address register. The fields in this register are interpreted as follows: the PAGE field (one bit) specifies the control page accessed (page 0 or page 1), the TSOUT field (four bits) specifies the timeslot (between 1 and 12) and the DOUTSEL field (two bits) specifies the data stream (data stream 0 to 3). **It is not recommended to set the control page entries for the currently active page; data corruption will result.**

The procedure to examine the control pages is as follows. Note that the following registers are internal to the STSIs.

1. Wait for BUSY = 0
2. Write the desired indirect address with RWB set to logic 1 into register 00H
3. Wait for BUSY = 0
4. Read the control page entry from register 01H (STSI Indirect Data)

The procedure to update the control page is:

1. Wait for BUSY = 0
2. Read register offset 02H in the STSI, bit 3 (STSI Configuration register, ACTIVE bit) to determine the current active page
3. Write the desired indirect data to register offset 01H (STSI Indirect Data register)
4. Write the desired indirect address with RWB set to logic 0 into register offset 00H (STSI Indirect Address register).

Table 25 STSI Control Page Entry

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Unused		RSVD	RSVD	TSEN	RSVD			TSIN				RSVD		DINSEL	

The bits in Table 25 are described as follows:

- Unused bits. These should all be set to ‘0’
- RSVD: RESERVED – should always be set to ‘0’
- TSEN: Used to for working/protect selection from the STSIs
- TSIN[3:0]: The input timeslot select bits select the input timeslot which is mapped to the current output timeslot. These bits drive the control for the timeslot interchange multiplexer in the muxing block.

Table 26 Timeslot Selection

TSIN[3:0]	DOUT
0000	XXXXXXXX
0001 – 1100	Holding registers (timeslots 1 – 12)
1101 – 1111	XXXXXXXX

DINSEL[1:0]: The input data stream select bits select the input data stream mapped to the current output timeslot. These bits drive the control for the data stream select multiplexer in the muxing block.

Table 27 Data Stream Selection

DINSEL[1:0]	DOUT
00	Holding registers (data stream 1)
01	Holding registers (data stream 2)
10	Holding registers (data stream 3)
11	Holding registers (data stream 4)

Table 28 STSI Indirect Address Register Format

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BUSY	RWB	Unused			PAGE	Unused		TSOUT[3:0]				Unused		DOUTSEL	

Table 28 provides the data stream number, the time-slot number, and the control page select used to access the control pages. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is in progress. The bits are as follows:

- DOUTSEL[1:0]: The Data Output Select bits select the output data stream accessed by the current indirect transfer.

DOUTSEL[1:0]	DOUT
00	DOUT #1
01	DOUT #2
10	DOUT #3
11	DOUT #4

- TSOUT[3:0]: The indirect STS-1/STM-0 output time slot bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access. Time slots #1 to #3 are valid in STS-3/STM-1 mode. Time slots #1 to #12 are valid in STS-12/STM-4 mode.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

- PAGE: The page bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

- RWB: The indirect access control bit selects between a configure (write) or interrogate (read) access to the control pages.
- BUSY: The indirect access status bit reports the progress of an indirect access.

13.5.3 Timeslot Interchange

The normal mode of operation for the STSI blocks is timeslot interchange. The blocks can be configured to perform timeslot interchange on either four independent data streams or one data stream striped across all four inputs. The difference lies in the value programmed into the DINSEL field of the STSI Indirect Data register and subsequently written into a selected control page entry.

The STSIs can be configured to perform timeslot interchange on any one of the following data formats: 1 x OC-48 (striped across 4 links) or 4 x OC-12. The timeslot interchange mechanism can be programmed to perform an arbitrary rearrangement of the data in either of these formats.

13.5.4 Control Page Selection

The current active page determines the timeslot interchange function. The change of page is synchronized with the start of a SONET frame on the ingress data streams. This prevents data corruption when switching pages. The active control page is selected by a combination of hardware and software control. The Ingress STSIs are controlled by LICMP and the Egress STSIs are controlled by LECMP. The following procedure is used to select the active page when using software control for active page selection in the STSI:

1. Read STSI Configuration register, ACTIVE bit (register offset 02H in the STSI, bit 3) to determine the current active page

2. Select the new active page by writing to top level Configuration register, PSEL bit (this assumes that the CMP pin for the STSI is ‘0’ as this is XORed with the register to form the STSI CMP).

3. Wait for the COAPI interrupt in the STSI to determine if the page change has occurred.

13.5.5 Page Change Interrupt

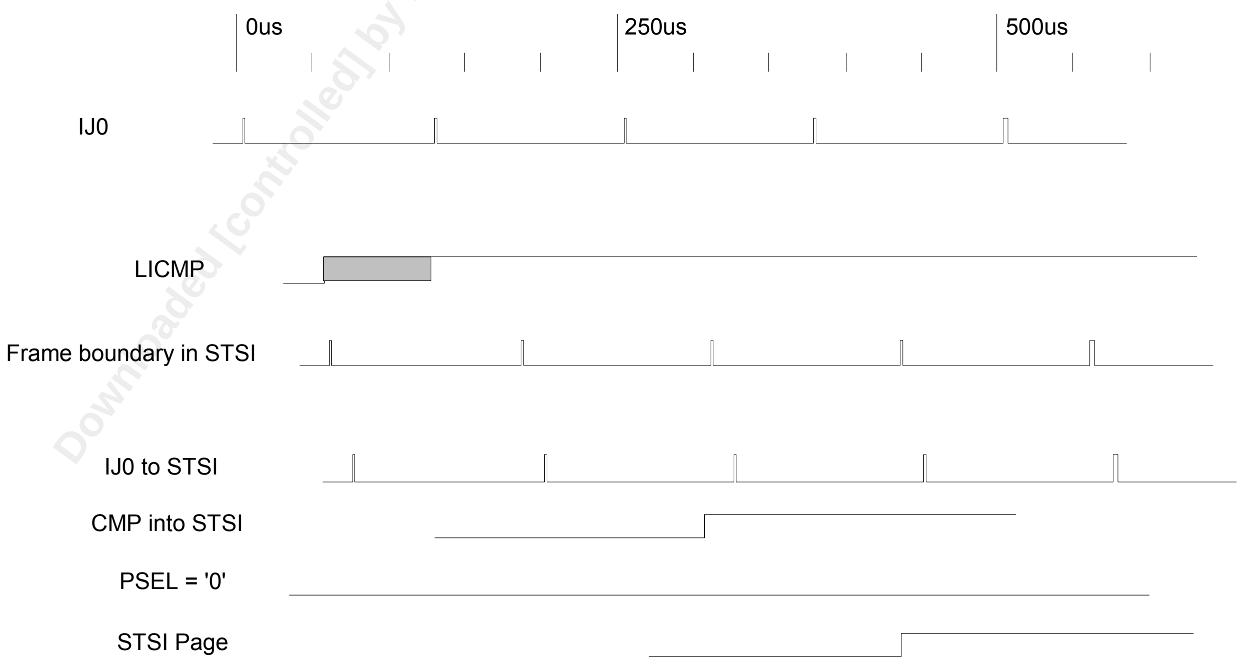
The STSI functional block indicates that the current active page has changed by setting bit 0, register offset 03H (STSI Interrupt Status, COAPI bit). Optionally the value of this bit can also be used to create a hardware interrupt via the top level STSI interrupts. This behavior is controlled by bit 0, register 02H (STSI Configuration register, COAPE bit). When this bit is set to logic zero (the default hardware reset value) the value of the COAPI bit is suppressed and no hardware interrupt can occur. When this bit is set to logic one, the value of the COAPI bit is propagated to the external hardware interrupt logic.

13.5.6 STSI CMP Timing

In serial mode, LICMP is sampled for ingress STSI at IJ0, and delays for the LINE_INGRESS_REF_DLY to allow J0s to align at the input to the STSIs. The sampled CMP takes effect on the second next frame boundary. In the egress path, CMP is sampled on IJ0, delayed for the egress SVCA delay and takes effect on the second next frame boundary. STS-1 switching will occur according to Figure 33. When in parallel mode, LICMP is sampled when the J0 byte location is present at the input of the working ingress STSI and the active page changes on the second next frame boundary. On the egress path in parallel mode, LECMP is sampled on EJ0J1[1] (with EPL[1] = ‘0’) and takes effect on the second next frame boundary.

CMP can also be configured with the top level PSEL registers. This value is XORed with the external CMPs. PSEL changes are sampled on the STSIs J0 and the page change takes effect on the next frame boundary.

Figure 33 STSI Page Change Timing (LINE_PARALLEL = ‘0’)



13.5.7 J0 Synchronization of the STSI in a CHESS System

Any TSE/TBS fabric can be viewed as a collection of different stages. For example, a Time-Space-Time switch could be constructed with five data path stages:

- Ingress load devices (e.g. SPECTRA 2488)
- Ingress time switch (e.g. TBS or STSI)
- Crossbar switch (e.g. TSE)
- Egress time switch (e.g. TBS or STSI)
- Egress load devices (e.g. SPECTRA 2488)

The STSIs on the line side of the TUPP 2488 are the equivalent of a TBS switching section.

Note that in some cases, one physical device may serve in two stages, such as SPECTRA 2488 in stages 1 and 5 or TBS in stages 2 and 4. STS-12 frames are pipelined through this fabric in a regular fashion, under control of a single clock frequency (77.76 MHz). In order to maintain valid framing for the group of STS-12 streams, the data path devices must be coordinated with one another. The first step in this coordination is the use of a global frame synchronization pulse to mark the position of frame boundaries as they enter the fabric. However, since each device in the system data path sees the STS-12 frames at a different latency than other devices, there must be a mechanism to account for the individual latencies at different points along the data path.

The most significant source of delay is the cumulative latency of the devices that lie along the system data path. To accommodate different system arrangements, a synchronization frame pulse and a programmable frame delay register are used to re-frame the STS-12 streams for each system data path device. In the TBS, this FIFO is 24-words deep and is controlled by the RJ0FP pin along with the RJ0DLY register (TUPP 2488 has IJ0 and similar registers to RJ0DLY). This frame delay register is used to inform the TBS or TUPP 2488 of the latency between a frame pulse on the RJ0FP/IJ0 pin and the presence of J0 characters in the FIFOs so that a re-framing mechanism can be triggered at the appropriate time. Because the J0 characters may lie at different FIFO depths, due to skew between links, this re-framing can be achieved by realigning the FIFO read pointers to match the J0 positions.

The purpose of the TUPP 2488s CML ALIGN and DMUX FIFOs is similar to the TBS FIFOs. The depth of the FIFOs is intended to accommodate skew between the arrival time of the J0 character between links of a single TUPP2488 device and between links of different TUPP 2488 devices. The LINE_INGRESS_REF_DLY value and SYSTEM_EGRESS_REF_DLY value specify an offset from the IJ0 and EJ0 frame pulse inputs to the device, respectively. This offset, inturn, specifies when the J0 character is read from the CML FIFOs. The reference delay values must be programmed such that the J0 character is present in the FIFOs at the time marked by the input frame pulse (referred to as the RXJ0FP marker in the register document) and associated REF_DLY offset. The TUPP 2488 simplifies the task of determining the correct REF_DLY values by reporting the difference between when the J0 character is written to the FIFO and when the RXJ0FP marker initiates a read of the J0 character. The distance value is reported in the CML Rx Slice Distance Register.

In addition to device latencies, there are other sources of delay. Furthermore, these delays may vary from link to link. For example, clock skew or differential trace lengths impose uneven delays on individual links. The 36-word depth of the FIFOs allows these delays to be equalized as part of the re-framing process. When the RJ0FP-RJ0DLY trigger signals the occurrence of a frame boundary, the Line Serial/CML will read the J0 character from address 0 of the FIFO, the position into which the J0 character is always written. As long as the J0 characters from all the STS-12 streams are indeed simultaneously present in their respective FIFOs when this occurs, the Serial/CML will effectively re-align the streams as part of the re-framing process. The large FIFO depth allows the Serial/CML to compensate for such differential delays as trace lengths that vary by several meters. Smaller delay variances, such as those due to clock jitter, need to be included in the FIFO depth budget. The effective FIFO depth is 31 bytes as the FIFO will report an error if the read and write pointers are too close. Therefore, the FIFOs can accommodate a total delay variance of 398ns between the arrival time of J0 characters on different links.

The number of clock cycles can be determined by simply adding the relevant device and cable length latencies or by reading the distance values reported by the FIFOs and adjusting the REF_DLY values appropriately. This synchronization mechanism is flexible enough to accommodate system paths with different cumulative device latencies.

13.6 Payload Processing Subsystem Operation

The Payload Processor Subsystem contains two paths: Tributary Path and Bypass Path. Each path supports a selection of modes of operation. When a mix of traffic is present both Tributary and Bypass Paths may be used. Both paths will receive all types of traffic, but only the correct path for that type of traffic will produce valid output data. The valid output data from the two paths is multiplexed together at the output of the Payload Processor in the Tributary-Bypass Mux.

13.6.1 Tributary Path

The Tributary path is used to process tributary traffic. The Tributary Path can process any legal mix of tributaries. The frame configuration must be predetermined and the Payload Processor top level registers and constituent functional blocks configured to be consistent with this frame configuration. The Tributary path performs tributary extraction, trail trace processing, tributary overhead processing serial alarm extraction and arbitrary C1/J0 alignment. High order justifications are translated to low order justifications, which ensures that outgoing tributaries are always in the same outgoing frame column as they came in.

For normal operation the incoming and outgoing frame configurations are the same. Legal frame configurations can be summarized as:

- AU3/VC3/TUG2
- AU4/VC4/TUG3/TUG2
- AU4/VC4/TUG3/TU3/VC3

The Tributary path can perform any legal AU3 to AU4 conversion, and AU4 to AU3 conversion with tributary traffic. This means that the incoming and outgoing frame configurations are different. The legal conversions for the Tributary path are:

- **3x** AU3/VC3/TUG2 to AU4/VC4/TUG3/TUG2
- **3x** AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3
- AU4/VC4/TUG3/TUG2 to **3x** AU3/VC3/TUG2

Note: Mixing AU3/VC3/C3 and AU3/VC3/TUG2 payloads in an AU4 during AU3 to AU4 or AU4 to AU3 conversion is not supported.

In both normal and conversion cases a TUG2 can contain a TU11, TU12, or TU2. Further details on SONET and SDH data types are given in the next section.

13.6.2 Tributary Path Functional Block Operation

The VTPI, RTTB336, RTOP336, and VTPA share a common internal architecture in the way they are configured, what payloads they support and how they process the incoming STM-4/STS-12 frames.

They process the portion of a SONET frame that corresponds to an STS-1 SPE. Equivalently, they process the portion of an SDH frame that corresponds to a VC3 with the 2 columns of fixed stuff that are added when mapping a VC3 into an AU3. By time-slicing the operation, they can process a SONET STS-12 or SDH STM-4 frame (the associated data bytes for four STM-1 frames whose bytes are labeled A, B, C, and D are interleaved in an STM-4 frame in the order A, B, C, D, A, B, C, D…) by independently processing 12 STS-1 SPEs or 12 VC3s carried within AU3s.

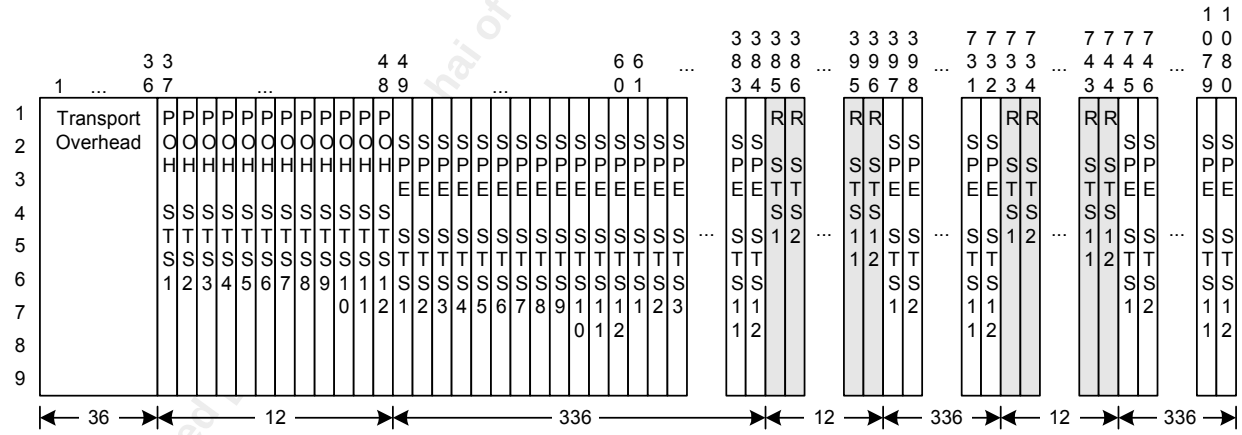
The payloads supported are summarized as follows:

- STS-1: This is default. Each STS-1 is assumed to carry seven VT groups, each of which can be independently configured to carry VT1.5s, VT2s, VT3s, or VT6s. There are up to 12 interleaved STS-1s, each processed independently, in the received STS-12 frame.
- AU3: This is also the default, as it corresponds exactly to STS-1, except for nomenclature. Each AU3 is assumed to carry seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of an AU3 is allowed but there is no SDH nomenclature to describe this). There are up to 12 interleaved AU3s, each processed independently, in the received STM-4 frame.
- TUG3: This is enabled for a particular STS-1 when the associated TU3 bit in the Frame Configuration Register is set low and ITUG3 bit of the same register is set high for the corresponding STS-1 (AU3) time slots. Four frame configuration registers are provided for each payload processing slice, one register for the VTPI, one for the RTOP336 and RTTB blocks, one for the VTPA ingress frames, and one for the VTPA egress frames. The TUG3 is multiplexed with two others into an AU4. Each TUG3 in the AU4 may be independently configured for TU3 or TUG2. The TUG3 processed carries seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. There are up to four interleaved AU4s, each processed independently, in the received STM-4 frame.

- TU3: This is enabled when the TU3 bit of a frame configuration register is set high. A single TU3 is placed in a TUG3 which forms one-third of the VC4. Each TUG3 in the VC4 may be independently configured for TU3 or TUG3.
- Transparent: This is used to conduct AU3/VC3/C3 frame configurations. Tributary level interrupts and alarms can be disabled because they have no relevance in a payload with no tributaries. The tributary path may accept frames in this format, but can only produce valid data from this format by converting it to a an AU4/VC4/TUG3/TU3/VC3 frame configuration. Other wise the Bypass path is used to process this type of traffic.

Transport overhead and path overhead bytes are shown for notational convenience only. In the incoming direction, except for the H4 byte, input data does not need to contain valid transport and STS/AU path overhead byte values Figure 34 shows an STS-12 (STM-4) frame carrying 12 STS-1 frames. The entire frame increments across the 12 STS-1 frames in a round-robin fashion. Therefore, every 12th byte (column) belongs to the same STS-1 frame. For simplicity, each of the 12 frames is shown to have a zero offset such that the SPE begins in the column immediately following the POH for the given STS-1. However, the offset may cause the SPE to begin anywhere within the frame. Additionally, each of the 12 STS-1 frames may have an independent offset.

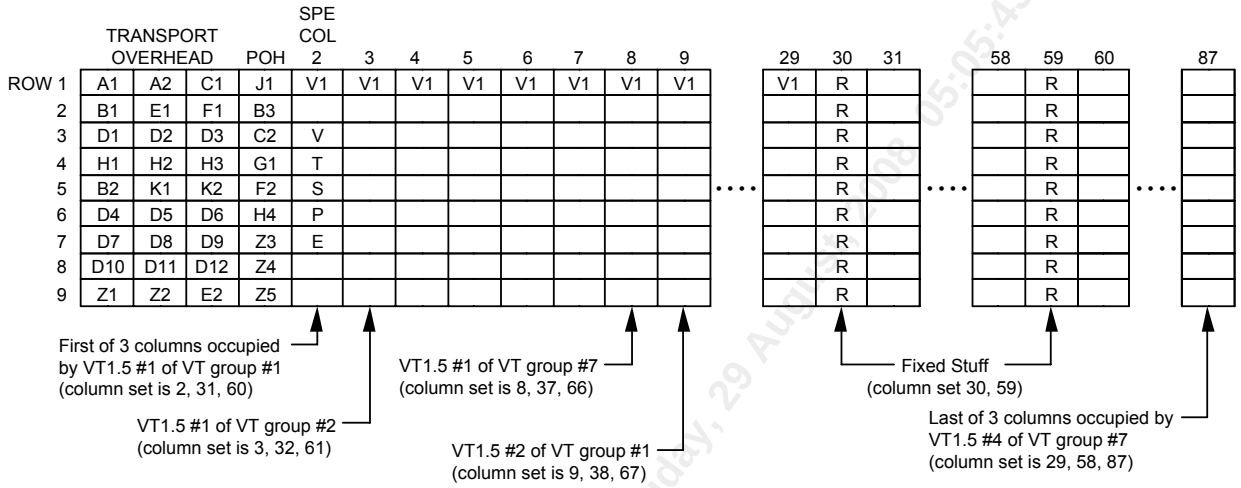
Figure 34 STS-12 Frame with 12 Interleaved STS-1s



STS-1

A sample placement of tributaries in STS-1 is illustrated in Figure 35. The figure shows a single STS-1 frame which is interleaved in the received STS-12 frame. For simplicity, this figure shows the synchronous payload envelope starting immediately after the J0 byte. Other alignments of the SPE with respect to the STS-1 frame are possible. This snapshot shows the first frame of the tributary multiframe when the V1 bytes are present. In subsequent frames, the byte position labeled V1 would sequentially carry the V2, V3, and V4 bytes. For improved readability, only the VT SPE bytes in the first column are labeled; those in the remaining columns are left blank. All tributary groups in Figure 35 are configured for VT1.5 streams.

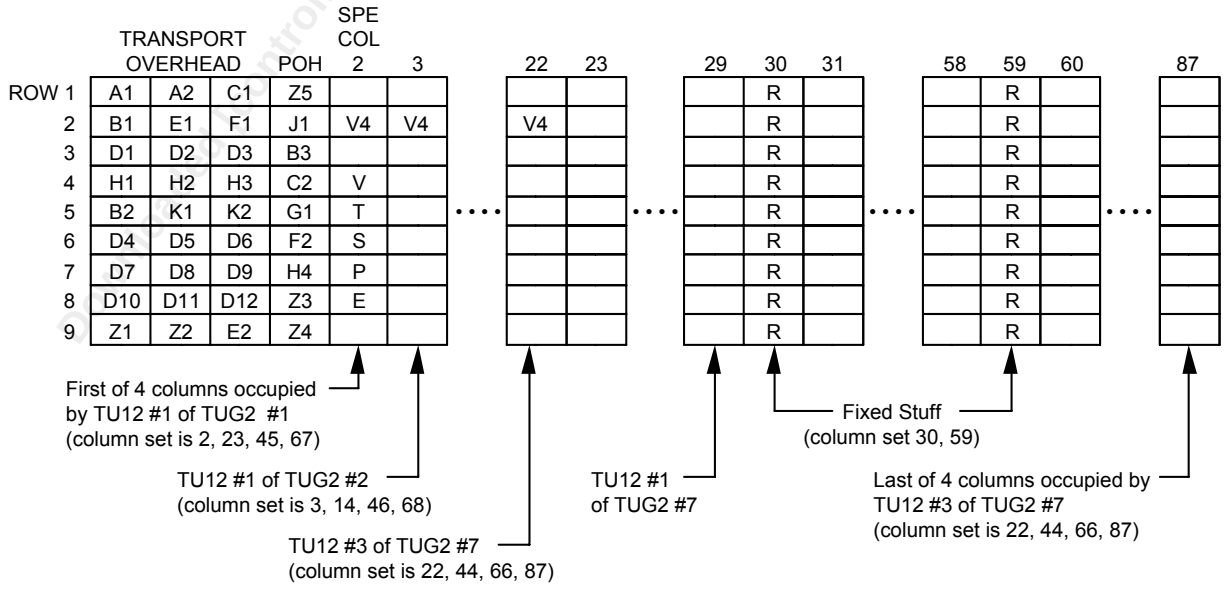
Figure 35 SONET STS-1 Carrying VT1.5



AU3

A possible placement of tributaries in AU3 is illustrated in Figure 36. This figure shows a single AU3 which is interleaved in the received STM-4 frame. This figure shows the virtual container starting immediately after the F1 byte. Other alignments of the VC with respect to the AU3 frame are possible. This snapshot shows of the last frame of the tributary multiframe when the V4 bytes are present. In subsequent frames, the byte position labeled V4 would sequentially carry the V1, V2, and V3 bytes. The H4 byte position shown is the one marked by the DTMF output. All tributary groups are configured for TU12 streams.

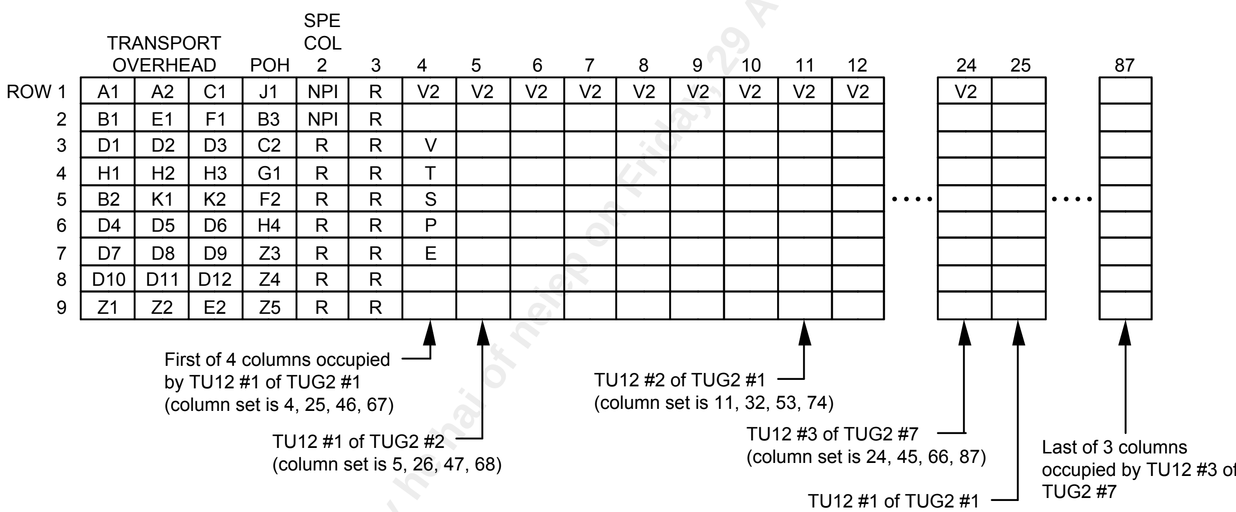
Figure 36 SDH AU3 Carrying TU12



TUG

Figure 37 illustrates a placement of tributaries in TUG3. This figure shows a single TUG3 which is interleaved in the received STM-4 frame. This figure shows the first TUG3 containing TUG2s that are multiplexed into the VC4. For the remaining two TUG3s, the path overhead column (POH) contains fixed stuff bytes. For simplicity, the VC4 is shown to begin immediately after the J0 byte. This example shows a snapshot of the second frame of the tributary multiframe when the V2 bytes are present. All seven TUG2s in the TUG3 are configured to carry TU12s.

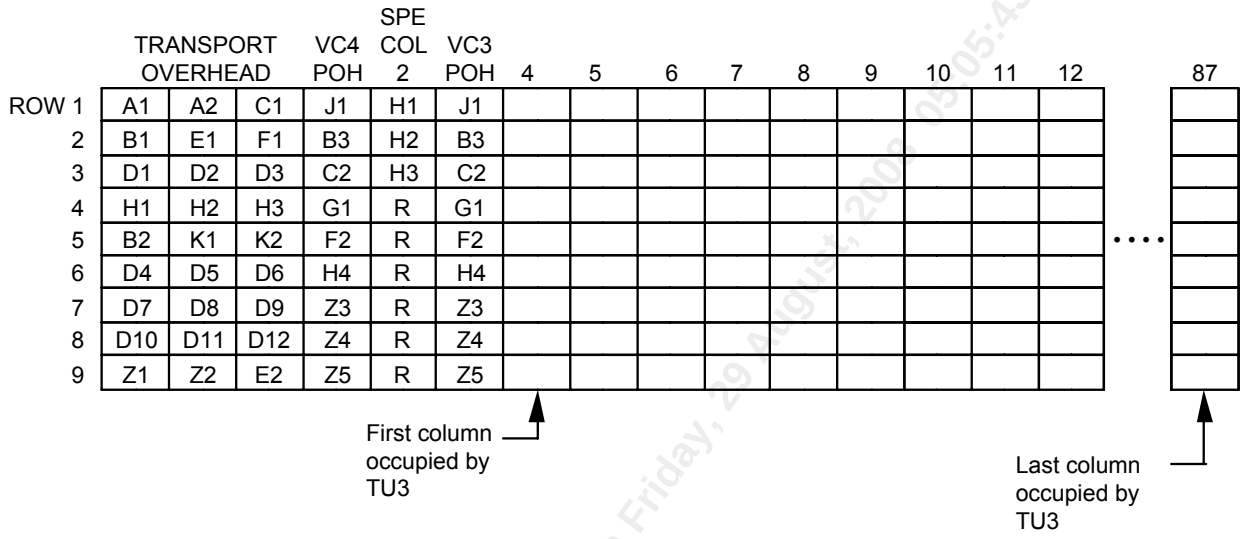
Figure 37 SDH TUG3 Containing TUG2s Configured for TU12



TU3

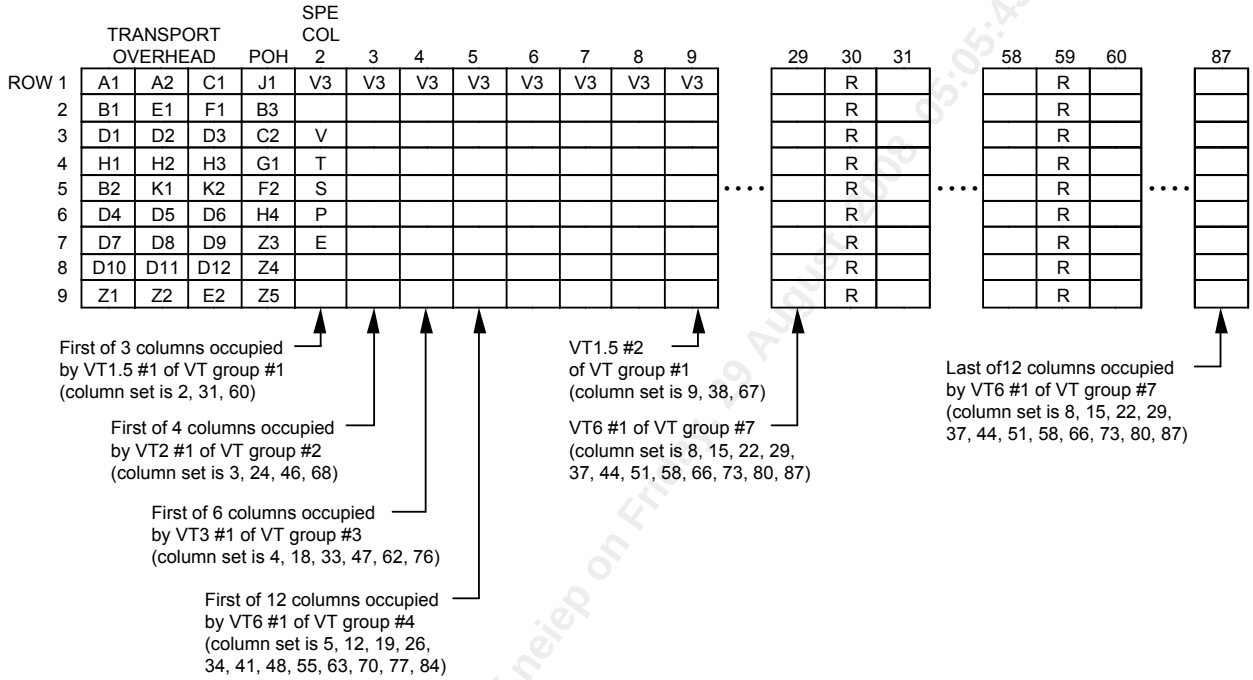
The placement of tributaries in TU3 is illustrated in Figure 38. This figure shows a single TUG3 which is interleaved in the received STM-4 frame. The first TUG3 that is multiplexed into the VC4 virtual container is shown. For simplicity, the VC4 is shown to immediately follow the C1 byte, and the VC3 is shown to immediately follow the TU3 H1 byte. The H1, H2, and H3 bytes in SPE column 2 form the TU3 offset pointer, while those in row 4 form the AU4 offset pointer.

Figure 38 SDH TUG3 Containing TU3



In the sample tributary placements shown so far, all virtual tributaries groups are configured to be of one type. Figure 39 illustrates a placement within an STS-1 frame, where the VT groups are configured for a mixture of tributary types. This snapshot shows the third frame in the tributary multiframe. VT group #1 is configured for VT1.5, VT group #2 for VT2, VT group #3 for VT3, and VT groups #4 to #7 for VT6.

Figure 39 SONET STS-1 Carrying Mix of VT1.5, VT2, VT3, and VT6



Thus far, the tributary placement figures have shown a simple STS-1 frame. However, the Payload Processor subsystem receives STS-12 (STM-4) frames. Therefore, all of the previous examples can co-exist within a given STS-12 frame. The only difference is that the number of columns for the frame increases by a factor of 12 to 1,044. The actual column within the STS-12 frame is determined by multiplying any illustrated column number minus 1 by 12 and adding an offset value within the range 0 – 11. For example, the first column shown would take on the values 1 through 12 ([1-1]x12 + N) corresponding to the Nth STS-1 frame within the STS-12 frame structure. Similarly, the last column would take on column values of 1,033 through 1,044 ([87-1)*12 + N) of the STS-12 frame.

Transparent

This is generally used to conduct AU3/VC3/C3 frame configurations. Transparent payload is not really a payload at all, but is a way of describing how to ‘keep the tributary path quiet’ by disabling interrupts etc. It is used when the Bypass path is active or when the Tributary path is converting an AU3/VC3/C3 to an AU4/VC4/TUG3/TU3/VC3/C3 frame.

When configured like this the tributary level interrupts and alarms can be disabled because they have no relevance in a payload with no tributaries. The tributary path may accept frames in this format, but can only produce valid data from this format by converting it to a an AU4/VC4/TUG3/TU3/VC3 frame configuration. Otherwise the Bypass path is used to process this type of traffic.

The tributary level interrupts and alarms from the VTPI, RTTB336, RTOP336, and VTPA functional blocks can be disabled using indirect accesses to the tributary configurations that would exist in the C3 space if the VC3 was carrying a TUG2 instead.

13.6.3 Tributary Path Functional Block Configuration and Status

The VTPI, RTTB336, RTOP336, and VTPA are configured through an indirect access mechanism. The RAM containing the configuration and status is memory mapped according to the memory maps set out in the register document. For a write operation, the data is first written to the indirect data register. The address along with the write command bit is written to the indirect address register thus initiating the write operation. For a read operation, only the address along with the read command bit is written to the indirect address register. The requested data is returned in the indirect data register. In both cases, when memory access has completed, the busy bit in the indirect address register is cleared.

13.6.4 Tributary Path Functional Block Interrupt Service

Upon entering any interrupt condition (and the corresponding interrupt is enabled) the interrupt signal INT of the functional block in an interrupt condition is pulsed. These INT signals may be read by the microprocessor at the top level registers bits VTPIINT, RTTBINT, RTOPINT, and VTPAINT. The protocol for servicing interrupts is as follows. All interrupt status registers in the functional block in interrupt are read. The status registers will narrow the search for the tributary containing an interrupt condition by indicating to the user which tributary(s) contain an interrupt service request. If multiple interrupt service requests exist, the priority and order of service is determined by the user. Knowledge of which tributary(s) contains interrupt service requests allows the user to perform an indirect access to retrieve status and interrupt information corresponding to the affected tributary(s).

For example, if Interrupt Source Register #1 in the VTPI indicated an interrupt condition in Register offset 0x06H and a subsequent read of Register 0x06H revealed an interrupt condition in tributary #5, the user would then initiate an indirect read access of tributary #5 to determine what interrupt condition occurred for that tributary. Prior to servicing a tributary, the corresponding interrupt status register bit TRIB_INT[X][Y][Z] must be cleared via the writing of a ‘1’ to that bit where X indicates STM-0 # ranging from 1 to 12, Y indicates TUG-2 # ranging from 1 to 7, and Z indicates tributary # ranging from 1 to 4.

13.6.5 Bypass Path

The Bypass Path is used to process Bypass STS-1 traffic including contiguous concatenated payloads. The Bypass path processes any legal mix of STS-1/3c/12c (VC-3/4/4-4c) payloads, i.e. including contiguous concatenation frame structures. The full range of frame structures supported by the Bypass Path can be summarized as:

- AU3/VC3/C3
- AU4/VC4/TUG3/TU3/VC3/C3
- AU4-4c
- AU4-16c (with four Payload Processor subsystems)

The Bypass path supports AU4 to AU3 conversion in the absence of TUG2's:

- AU4/VC4/TUG3/TU3/VC3/C3 to **3x** AU3/VC3/C3

Note that the Bypass path will always convert an AU4 to an AU3 in the above manner. The Bypass path should not be used in the presence of TUG2's – the Tributary path should be used to process those payloads instead.

The Bypass path also supports Transparent Bypass mode. The Transparent Bypass Mode passes frames unaltered from the payload processor input, to the payload processor output.

13.6.6 SVCA_R Operation

The SVCA_R can be configured in a similar manner to the Tributary path functional block (VTPI, RTTB336, RTOP336, and VTPA). The internal SVCA Payload Configuration register is used to set up the SVCA_R incoming frame configuration. An indirect access mechanism is used to further configure/interrogate the SVCA_R at an STS-1/STM-0 level.

13.6.7 SVCA_R Interrupts

The SVCA_R can generate interrupts on its INT signal. This INT signal may be read by the microprocessor at the top-level registers bit SVCA_INT in top level register 0DH. The SVCA_R will only generate interrupts when:

- A negative or a positive pointer justification event occurs in the outgoing data stream.
- An underflow or an overflow event occurs in the internal FIFO.

In the first case, a pointer justification is not a cause for concern. An underflow or overflow of the internal FIFO is a serious error and generally indicates that excessive consecutive high order justifications have taken place in violation of the standards or that the NTHRES[3:0] and PTHRES[3:0] SVCA internal register bits have been set to an incorrect value. Interrupts due to justifications could be disabled without affecting the performance of the SVCA_R. Interrupts due to FIFO underflow and overflow events should not be disabled.

13.6.8 SVCA_R Latency Reduction

The SVCA_R functional block is designed to bridge across plesiochronous input and output clocks among other things. As the input and output clocks vary with respect to each other, high order justifications are generated to compensate. However in the payload processor the SVCA_R is not used in this way and both input and output clocks are driven by the same clock source. In the payload Processor subsystem, the SVCA_R is used to realign the incoming frame to a new reference, to insert valid A1, A2, H1 and H2 bytes and to convert from AU4 to AU3 (receive path only) in the absence of TUG2's.

Since a large source of high order justifications is not present in the payload processor (i.e. plesiochronous input and output clocks), the restrictions on the internal FIFO may be tightened so as to reduce latency through the SVCA_R.

A bias is created towards negative justifications and the FIFO depth can be reduced overall because of the lack of internally generated justifications from plesiochronous input and output clocks. In doing so, the FIFO tends towards a low fill level, which reduces the latency by as much as 45%.

The SVCA_R can be configured to operate in this manner by setting the following bits in the internal SVCA Pointer Justification Thresholds register, 09H:

- NTHRES[3:0] = “1111”
- PTHRES[3:0] = “0011”

The latency of the SVCA_R using the default values for NTHRES[3:0] and PTHRES[3:0] is:

- Minimum latency = 1.18 µs
- Typical latency = 2.25 µs
- Maximum latency = 3.30 µs

Using the new values for NTHRES[3:0] and PTHRES[3:0] (above) the latency of the SVCA_R is reduced to:

- Minimum latency = 0.53 µs
- Typical latency = 1.19 µs
- Maximum latency = 1.825 µs

13.6.9 PP Subsystem SVCA_R Bypass

The SVCA_R blocks within the PP Subsystem may be optionally bypassed by setting the ISVCA_ESDIS bit of the Ingress SVCA Configuration register to a logic 1. Similarly, each SVCA_R block can be bypassed independently from the others within the PP subsystem by setting the ESDIS bit of the associated SVCA Miscellaneous Register to a logic 1. When bypassed, the SVCA_R does not re-align the input data to a new transport frame alignment, the internal FIFO is locked, and data is passed with minimal delay.

13.6.10 PP Subsystem Modes of Operation

The Payload Processor Subsystem supports seven modes of operation. Some modes can be simultaneously supported at an STS-1/STM-0 or STS-3/STM-1 granularity. Others are only supported individually at an STS-12/STM-4 or STS48/STM-16 (with four payload processors) granularity. The modes are:

- Tributary Mode
- Bypass STS-1 Mode
- AU4 to AU3 Tributary Mode
- AU4 to AU3 Bypass Mode
- AU3 to AU4 Tributary Mode 1

- AU3 to AU4 Tributary Mode 2
- Transparent Bypass Mode

The following sections describe in detail each mode of operation, the restrictions with respect to simultaneous support of other modes and an overview of how to configure the payload processor to support each mode.

Either the Tributary Path or the Bypass Path supports each mode. Both paths will process the incoming STS-12/STM-4 frame regardless of the mode of operation. However, only the path that supports that mode will produce a valid output. The Tributary-Bypass Mux at the output side of the Payload Processor is used to select the valid data from either Tributary or Bypass paths at an STS-1/STM-0, STS-3/STM-1 or STS-12/STM-4 granularity. Which of the Tributary or Bypass paths is chosen for a given SONET/SDH high order path is configured using the TBM_STS1_SELECT[12:1] bits of the Tributary-Bypass Mux Configuration and Status Registers. The Tributary-Bypass Mux must be configured for all modes of operation.

Modes that can be supported simultaneously with other modes at an STS-1/STM-0 or STS-3/STM-1 granularity will be referred to as *Simultaneous* modes. Modes that can only be supported individually at an STS-12/STM-1 or STS-48/STM-16 granularity will be referred to as *Individual* modes.

The VTPA glue logic unequipped enable bit (VIG_UNEQ_EN) of the VIG configuration register configures the device to optionally set the EIDLE_HTPOHEN output pin when unequipped is detected by the RTOP. Configure the VIG_UNEQ_EN to achieve the desired behavior. Note configuring the VIG_UNEQ_EN bit is only required when the Payload Processor Loopback mode is used.

The VTPA operates in a LOCKED mode where the high order pointer in the outgoing data stream is fixed. Specify the desired high order pointer and SS value in the VTPA outgoing data stream by programming the Locked Mode High Order Pointer and Locked Mode Concatenation Indicator registers, respectively. The locked mode high order pointer register defaults to the recommended pointer value of 522.

When converting from and AU3 to AU4 and vice versa, the path overheads of the resulting VC4's and VC3's are shown in Table 29.

Table 29 Outgoing Path Overhead after AU3 to/from AU4 Conversions

Incoming Payload	Outgoing Payload	Outgoing VC4 Path Overhead	Outgoing VC3 Path Overhead
AU4/VC4/TUG3/TUG2	AU3/VC3/TUG2	N/A	All zero (*)
AU3/VC3/TUG2	AU4/VC4/TUG3/TUG2	All zeros (*)	N/A
AU3/VC3/C3	AU4/VC4/TUG3/TU3/VC3/C3	All zeros (*)	Same as Incoming VC3 Path Overhead
AU4/VC4/TUG3/TU3/VC3/C3	AU3/VC3/C3	N/A	Same as Incoming VC3 Path Overhead

13.6.11 Tributary Mode

Tributary Mode is the default mode of the Tributary Path. The incoming and outgoing frame configurations are the same.

Tributary Mode is a simultaneous mode.

Table 30 Tributary Mode Configuration

Functional Block or Glue Block	Description
VTPI	Set frame configuration using top level registers. Set frame and tributary configuration using internal registers and indirect accesses. Enable interrupts on paths in this mode.
RIG	Enable inputs for SUSPEND generation as required.
RTTB336 / RTOP336 / TASR	Set frame configuration using top level registers. Set frame and tributary configuration using internal registers and indirect accesses. Enable interrupts on paths in this mode.
VTPA	Set frame configuration using top level registers. Set frame and tributary configuration using internal registers and indirect accesses. Enable interrupts on paths in this mode. Set LOCKED mode high order pointer and SS values.
Tributary-Bypass Mux	Set TBM_STS1_SELECT[12:1] to ‘1’ for paths in this mode.
SIG	Set frame configuration.
SVCA_R	Set frame configuration using top level registers. Set frame and path configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.

13.6.12 Bypass STS-1 Mode

Bypass STS-1 Mode is the default mode of the Bypass Path. The incoming and outgoing frame configurations are the same except when the incoming frame contains AU4/VC4/TUG3/TU3/VC3/C3. In this case, the outgoing frame is converted to AU3/VC3/C3. Bypass STS-1 mode supports contiguous concatenated payloads. Bypass STS-1 mode is a simultaneous mode for payloads of STS-1/STM-0 and STS-3/STM-1. Bypass STS-1 mode is an individual mode for payloads of STS-12/STM-4 and STS-48/STM-4.

Table 31 Bypass STS-1 Mode Configuration

Functional Block or Glue Block	Description
VTPI	Set frame configuration using top level registers. Set frame and 'dummy' tributary configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.
RIG	Enable inputs for SUSPEND generation as required.
RTTB336 / RTOP336 / TASR	Set frame configuration using top level registers. Set frame and 'dummy' tributary configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.
VTPA	Set frame configuration using top level registers. Set frame and 'dummy' tributary configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode. Set LOCKED mode high order pointer and SS values.
Tributary-Bypass Mux	Set TBM_STS1_SELECT[12:1] to '0' for paths in this mode.
SIG	Set frame configuration. Set SIG_TUG3=1 if conversion is required. If in STS-48c/AU-4-16c mode the SIG in the first payload processor should be configured as a Master (BYPASS_SLAVE = 0). The SIG's in the other 3 payload processors should be configured as slaves (BYPASS_SLAVE=1)
SVCA_R	Set frame configuration using top level registers. Set frame and path configuration using internal registers and indirect accesses. Enable interrupts on paths in this mode. If in STS-48c/AU-4-16c mode the SVCA_R in the first payload processor should be configured as a Master (SLAVE = 0). The SVCA_R's in the other 3 payload processors should be configured as slaves (SLAVE=1)

13.6.13 AU4 to AU3 Tributary Mode

The Tributary Path supports AU4 to AU3 Tributary Mode. The incoming and outgoing frame configurations are different. Details of the frame configurations supported are shown in Section 13.6.1 but in general contain TUG2's:

- AU4/VC4/TUG3/TUG2 -> **3x** AU3/VC3/TUG2
- AU4 to AU3 Tributary Mode is a simultaneous mode.

Table 32 AU4 to AU3 Tributary Mode Configuration

Functional Block or Glue Block	Description
VTPI	Set frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as input frame configuration. Enable interrupts on paths in this mode.
RIG	Enable inputs for SUSPEND generation as required.
RTTB336 / RTOP336 / TASR	Set frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as input frame configuration. Enable interrupts on paths in this mode.
VTPA	Set input frame configuration using top level registers as input frame configuration. Set output frame configuration using top level registers as output frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as output frame configuration. Enable interrupts on paths in this mode. Set LOCKED mode high order pointer and SS values.
Tributary-Bypass Mux	Set TBM_STS1_SELECT[12:1] to '1' for paths in this mode.
SIG	Set frame configuration.
SVCA_R	Set frame configuration using top level registers. Set frame and path configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.

13.6.14 AU4 to AU3 Bypass Mode

The Bypass path supports AU4 to AU3 Bypass Mode. The incoming and outgoing frame configuration are different. Details of the frame configurations supported are shown in Section 13.6.5 but in general do not contain TUG2's.

- AU4/VC4/TUG3/TU3/VC3/C3 -> **3x** AU3/VC3/C3

AU4 to AU3 Bypass Mode is a simultaneous mode.

AU4 to AU3 Bypass Mode can be implemented using the same configuration as for Bypass STS-1 Mode as shown in Table 31.

In this mode, the RTTB336 and RTOP336 may be enabled for the AU4 timeslot(s) to process the VC3 path overhead. This is the only time that the RTTB336 and RTOP336 should be enabled for bypass traffic.

13.6.15 AU3 to AU4 Tributary Mode 1

The Tributary Path supports AU3 to AU4 Tributary Mode. The incoming and outgoing frame configurations are different. Details of the frame configurations supported are shown in Section 13.5.1 but contain TUG2's.

- **3x** AU3/VC3/TUG2 -> AU4/VC4/TUG3/TUG2

AU3 to AU4 Tributary Mode 1 is a simultaneous mode.

Table 33 AU3 to AU4 Tributary Mode Configuration

Functional Block or Glue Block	Description
VTPI	Set frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as input frame configuration. Enable interrupts on paths in this mode.
RIG	Enable inputs for SUSPEND generation as required.
RTTB336 / RTOP336 / TASR	Set frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as input frame configuration. Enable interrupts on paths in this mode.
VTPA	Set input frame configuration using top level registers as input frame configuration. Set output frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as output frame configuration. Enable interrupts on paths in this mode. Set LOCKED mode high order pointer and SS values.
Tributary-Bypass Mux	Set TBM_STS1_SELECT[12:1] to '1' for paths in this mode.
SIG	Set frame configuration.
SVCA_R	Set frame configuration using top level registers. Set frame and path configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.

13.6.16 AU3 to AU4 Tributary Mode 2

The Tributary path supports AU3 to AU4 Tributary Mode 2. The incoming and outgoing frame configurations are different. Details of the frame configurations supported are shown in Section 13.6.1 but do not contain TUG2's.

- **3x** AU3/VC3/C3 -> AU4/VC4/TUG3/TU3/VC3/C3

AU3 to AU4 Tributary Mode 2 is a simultaneous mode.

When the incoming AU3/VC3/C3 payloads are in AIS condition, the VTPA block cannot automatically propagate the high order AIS signal (AU3/VC3) to the low order payload (TU3/VC3). Instead, the VTPA will generate a valid (non-AIS) TU3/VC3 pointer. In order to correctly insert AIS in the VTPA, the IPAIS bit (Bit 5 Indirect Reg 01H in VTPA) should be set to logic one when AIS is detected on the incoming AU3/VC3/C3 in the SARC-48 block. This configuration only applies to AU3 to AU4 Tributary Mode 2.

Detailed procedure:

1. For the paths that are in AU3/VC3/C3 to AU4/VC4/TUG3/TU3/VC3/C3 conversion, monitor the SARC 48 PAISPTRV [48:1] status bit (21D4H to 21D7H) and the SARC 48 PAISPTRI [48:1] interrupt status bit (21DCH to 21DFH) for high order AIS indications.

2. When the PAISPTRV bits are asserted, for the corresponding paths, set the VTPA IPAIS bit (VTPA indirect register 01H, bit 5) to ‘1’.

3. When the PAISPTRV bits are de-asserted, for the corresponding paths, clear the VTPA IPAIS bit to ‘0’.

Note that the maximum BUSY bit assertion time for VTPA indirect register access is 345 REFCLK cycles (345 x 12.86ns = 4.44 us).

Table 34 AU3 to AU4 Tributary Mode 2

Functional Block or Glue Block	Description
VTPI	Set frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as input frame configuration. Disable interrupts on paths in this mode.
RIG	Enable inputs for SUSPEND generation as required.
RTTB336 / RTOP336 / TASR	Set frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as input frame configuration. Disable interrupts on paths in this mode.
VTPA	Set input frame configuration using top level registers as input frame configuration. Set output frame configuration using top level registers as input frame configuration. Set frame and tributary configuration using internal registers and indirect accesses as output frame configuration. Enable interrupts on paths in this mode. Set LOCKED mode high order pointer and SS values.
Tributary-Bypass Mux	Set TBM_STS1_SELECT[12:1] to '1' for paths in this mode.
SIG	Set frame configuration.
SVCA_R	Set frame configuration using top level registers. Set frame and path configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.

13.6.17 Transparent Bypass Mode

The Bypass path supports Transparent Bypass mode. The incoming and outgoing frame configurations are the same. The frame is not processed in any way but is simply passed transparently to the output of the Payload Processor. The Transparent Mode is an Individual Mode. All legal SONET/SDH frame configurations are supported.

Table 35 Transparent Bypass Mode Configuration

Functional Block or Glue Block	Description
VTPI	Set frame configuration using top level registers. Set frame and 'dummy' tributary configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.
RIG	Enable inputs for SUSPEND generation as required.
RTTB336 / RTOP336 / TASR	Set frame configuration using top level registers. Set frame and 'dummy' tributary configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode.
VTPA	Set frame configuration using top level registers. Set frame and 'dummy' tributary configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode. Set LOCKED mode high order pointer and SS values.
Tributary-Bypass Mux	Set TBM_STS1_SELECT[12:1] to '0' for paths in this mode.
SIG	Set frame configuration.
SVCA_R	Set frame configuration using top level registers. Set frame and path configuration using internal registers and indirect accesses. Disable interrupts on paths in this mode. Set ISVCA_ESDIS = 1 in top level register

13.6.18 TASR Operation

The TASR is configured using a mixture of direct and indirect accesses. Each tributary must be configured through the indirect access mechanism.

To read the per-tributary configuration:

1. Poll the BUSY in the Indirect Tributary Address register bit until it is low.
2. Write the Indirect Tributary Address register, setting the RWB bit high and setting the STM1, TUG3, TUG2, and TU bits to indicate the tributary you wish to access.
3. Poll the BUSY bit in the Indirect Tributary Address register bit until it deasserts.
4. Read the Indirect Data Register #1.
5. Return to step 2 to read the configuration and status of another tributary.

To write the per-tributary configuration and status:

1. Poll the BUSY in the Indirect Tributary Address register bit until it is low.

2. Write the desired configuration to the Indirect Data Register #1.

3. Write the Indirect Tributary Address register, setting the RWB bit low and setting the STM1, TUG3, TUG2, and TU bits to the desired values. (The data written in step 2 will take effect for the selected tributary once the BUSY in the Indirect Tributary Address register bit deasserts.)

4. Return to step 1 to configure another tributary.

Interrupt Service Routine

Each tributary within the TASR has an interrupt bit for the signal fail (SF) alarm. The interrupt sources for SF are summarized in Table 15.

The TASR generates TRIB_INT[X][Y][Z] interrupts based on transitions in the value of tributaries' SFV register bit. When the SFV register bit for a tributary transitions from either 1 to 0 or 0 to 1, the TRIB_INT[X][Y][Z] interrupt is generated.

If the SFE bit of the TASR Indirect Data Register #1 is programmed to logic 1 and the SFV bit transition occurs, the corresponding TRIB_INT[X][Y][Z] interrupt status bit will get asserted. The device INTB output will be asserted if the INTE bit of the TASR configuration register is set to logic 1. The contribution of interrupts from the TASR block to the device INTB will be masked if the INTE bit is a logic 0.

Note that the device INTB pin and TASR TRIB_INT[X][Y][Z] register bits will not become asserted if the SFE enable bit is asserted after the SFV transition occurs. The SFE interrupt enable bit must be set to logic 1 before the SFV changes status.

Once a device interrupt has been asserted as a result of a TASR interrupt, the TASR interrupt can only be cleared by clearing the TRIB_INT[X][Y][Z] interrupt status register bits. TRIB_INT[X][Y][Z] register bits are write-one-to-clear bits. In other words, to clear a TRIB_INT[X][Y][Z] register bit, the user must write a logic 1 to the register bit. Note also that the interrupt bits within the TASR Interrupt Source #1 and TASR Interrupt Source #2 registers clear automatically and instantaneously when the corresponding TRIB_INT[X][Y][Z] bit (or bits) are cleared.

To aid in quick identification of interrupts, the TASR provides a hierarchy of interrupt summary bits . Using the interrupt summary bits to guide the search, an interrupt on any of the 336 tributaries is identifiable with 2 steps. To do so, first identify the register containing the tributary interrupt summary bit by reading the Interrupt Source #1 and the Interrupt Source #2 registers. Next, identify which tributary is generating the interrupt by reading the appropriate STM-0 #X Interrupt Status register.

13.7 Tributary Bit Error Rate Monitoring (TBER) Features

The TBER power-up default operation mode is the TU11/VT1.5. The TBER is configured through indirect address registers. For a write operation, the data is first written to the indirect data registers. The address along with the write command bit is written to the indirect address register thus initiating the write operation. For a read operation, only the address along with the read command bit is written to the indirect address register. The requested data is returned in the indirect data registers. In both cases, when memory access has completed, the busy bit in the indirect address register is cleared. The Busy bit will never stay high more than 25 clock cycles, and will usually be high for ~10 clock cycles.

The Tributary Bit Error Rate Monitor (TBER) block counts and monitors BIP-2 errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. Table 36 lists the recommended contents of the Lookup Table registers for different VT levels (VT1.5, VT2, VT3 and VT6, and their TU-equivalents) and for different BER monitoring levels for both declaration and removal. The individual Tributaries can be programmed to individually monitor any BER between 10-3 to 10-12.

These values must be written to the Lookup Table RAM. The Declaration Period and Declaration Threshold settings should be written to IP[35:0] and ERROR_THR[4:0], respectively with SET_CLEAR = 0. Meanwhile, the Removal Period and Removal Threshold settings should be written to IP[35:0] and ERROR_THR[4:0], respectively with SET_CLEAR = 1.

The recommended method for cleanly reconfiguring a path can be summarized as follows:

1. Disable the path.

2. Clear the interrupt status corresponding to this path in indirect register 03H: TBER Indirect Data #3 (TU RAM Access).

3. Program all fields for this path in indirect registers: 01H: (TU RAM Access) and 01H to 03H (LOOKUP TABLE RAM Access). The values to use for these registers depend on the type of BER test, the traffic concatenation level and the error rate which is to be monitored. Refer to settings listed in Table 36 for recommended values.

4. Re-enable the path.

The recommended method for simply disabling a path is to perform steps #1 – 2 only from the list above. If the path is to be re-enabled later, then steps #3 – 4 can be performed.

Table 36 Recommended BER Monitor Settings

VT Path Type	BER	Declaration Period	Declaration Threshold	Removal Period	Removal Threshold
VT1.5	1.00E-03	000000028	10	00000002D	07
VT1.5	1.00E-04	000000162	10	000000190	09
VT1.5	1.00E-05	000000D59	10	000000F7A	09
VT1.5	1.00E-06	0000084FE	10	000009A7E	09
VT1.5	1.00E-07	000053171	10	0000608A5	09
VT1.5	1.00E-08	00033EDF1	10	0003C562E	09
VT1.5	1.00E-09	002074AF0	10	0025B5D84	09
VT1.5	1.00E-10	01448ECEB	10	01791A6E4	09
VT1.5	1.00E-11	0CAD940B2	10	0EBB0849F	09
VT1.5	1.00E-12	7EC7C86F4	10	934E52E36	09
VT2	1.00E-03	000000028	12	000000028	08
VT2	1.00E-04	00000010B	10	000000148	0A
VT2	1.00E-05	0000009EE	10	000000C81	0A
VT2	1.00E-06	0000062CF	10	000007CC1	0A
VT2	1.00E-07	00003DB99	10	00004DF3D	0A
VT2	1.00E-08	000269383	10	00030B814	0A
VT2	1.00E-09	00181C2A7	10	001E7307D	0A
VT2	1.00E-10	00F119A11	10	01307E494	0A
VT2	1.00E-11	096B00430	10	0BE4EED7B	0A
VT3	1.00E-03	000000028	16	000000028	0C
VT3	1.00E-04	0000000B5	11	0000000EB	0B
VT3	1.00E-05	000000693	10	000000845	0A
VT3	1.00E-06	000004145	10	000005265	0A
VT3	1.00E-07	000028C35	10	0000337A8	0A
VT3	1.00E-08	000197995	10	000202C4A	0A
VT3	1.00E-09	000FEBF5B	10	00141BA99	0A
VT3	1.00E-10	009F37915	10	00C9149AD	0A
VT3	1.00E-11	06382BA54	10	07DACE076	0A
VT3	1.00E-12	3E31B4748	10	4E8C0C49C	0A
VT6	1.00E-03	000000028	1E	000000028	11
VT6	1.00E-04	000000066	12	00000007A	0A
VT6	1.00E-05	00000036A	11	000000463	0A
VT6	1.00E-06	0000021A6	11	000002B8D	0A
VT6	1.00E-07	000015001	11	00001B332	0A
VT6	1.00E-08	0000D1F8F	11	00010FFA7	0A
VT6	1.00E-09	000833B14	11	000A9FC35	0A
VT6	1.00E-10	005204E4A	11	006A3D9BF	0A

VT Path Type	BER	Declaration Period	Declaration Threshold	Removal Period	Removal Threshold
VT6	1.00E-11	033430E61	11	042668123	0A
VT6	1.00E-12	2009E8FCA	11	298010B5E	0A
TU3	1.00E-03	000000005	16	000000006	0E
TU3	1.00E-04	000000019	11	000000023	0C
TU3	1.00E-05	0000000F3	11	00000014D	0B
TU3	1.00E-06	000000968	11	000000CF1	0B
TU3	1.00E-07	000005DFD	11	000008159	0B
TU3	1.00E-08	00003ABCA	11	000050D67	0B
TU3	1.00E-09	00024B5D5	11	0003285FB	0B
TU3	1.00E-10	0016F1A3E	11	001F93BBD	0B
TU3	1.00E-11	00E57065C	11	013BC5550	0B
TU3	1.00E-12	08F663F98	11	0C55B5520	0B

Notes

- The declaration period and removal period values above are designed to meet or exceed both ITU and Telcordia maximum detection and clearing time requirements with the required confidence.

The TBER can suspend counting and monitoring of the BIP-2 errors. This can be used to suppress SD/DEXC threshold crossings during AIS, LOP, LOM, UNEQ, PDI, TIM, and TIU alarms reported by the RTOP block. The suspend feature is enabled by setting the SUSPEND_EN bit of the TASR Configuration Register. A LOM or LOP alarm will halt the BER count for the associated tributary if the LOPLOMPDI of the RTOP Indirect Tributary Data Register #5 is set to a logic 1. Similarly, the RTOP AIS, UNEQ, PDI, TIM or TIU alarms will halt the BER count for a tributary if the associated RTOP AISPDI, UNEQPDI, PDIVPDI, TIMPDI, or TIUPDI bit, respectively, is set to a logic 1.

13.8 Wideband Switch Fabric Subsystem Operation

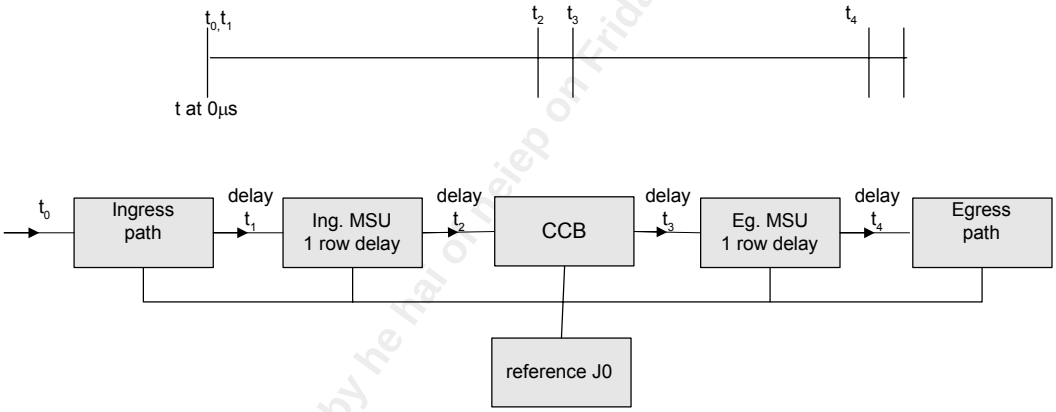
This section describes operation of the Wideband Switch Fabric in TUPP 2488.

13.8.1 "J0" Synchronization for Wideband Switches

Any Wideband Time/Space/Time fabric can be viewed as a collection of "columns" of devices. For example in a Hairpinning application in TUPP 2488: column 0 consists of the ingress flow (e.g., Payload processing sub-system); column 1 consists of the ingress flow through the ingress MSUs; column 2 consists of the CCB; column 3 consists of the egress flow through the egress MSUs; and column 4 consists of the egress flow through the SVCAs. Path-aligned STS-12 frames are pipelined through this structure in a regular fashion, under control of a single clock source and frame pulse. There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.

A reference pulse (EJ0) is generated externally and fed to each switch in a fabric. Each switch has a delay register which contains the count of 77.76 MHz clock ticks that device should delay from the reference timing pulse before expecting the J0 characters of the egress STS-12 frames to have arrived. The base timing pulse is called *t*. The delays from *t* based on the settings of the delay registers in the successive columns of the devices are called t_0, … t_4. The first signal, t_1(equal to t_0), determines the start of an STS-12 frame; this signal is used to instruct the egress load devices (column 0) to start emitting an STS-12 frame (with its special "J0" control character) at that time. t_i is determined by the customer, based on device and wiring delays to be approximately the earliest time that all "J0" characters will have arrived in the egress FIFOs of the t_i column of devices. t_i is selected to provide assurance that all "J0" characters have arrived at the i^{th} column. The i^{th} column of devices use the t_i signal to synchronize emission of the STS-12 frames. The egress FIFOs permit a variable latency in J0 arrival of up to 16 clock cycles.

Figure 40 "J0" Synchronization Control



13.8.2 Synchronized Control Setting Changes For CCB and MSU

The Wideband Switches support dual switch control settings. These dual settings permit one bank of settings to be operational while the other bank is updated as a result of some new connection requests. The CMP inputs select the current operational switch control settings. CMP is sampled by TUPP 2488 on EJ0. The internal blocks sample the registered CMP value as they receive the next J0 character –after a delay defined by software.

The new CMP value is applied on the first A1 character of the following STS-12 frame. This switchover is hitless; the control change does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted (see the discussion of the connection routing algorithm in this document).

The Column granularity switch settings RAM in organized into two control setting banks, these are switched by the above mechanisms on frame boundaries.

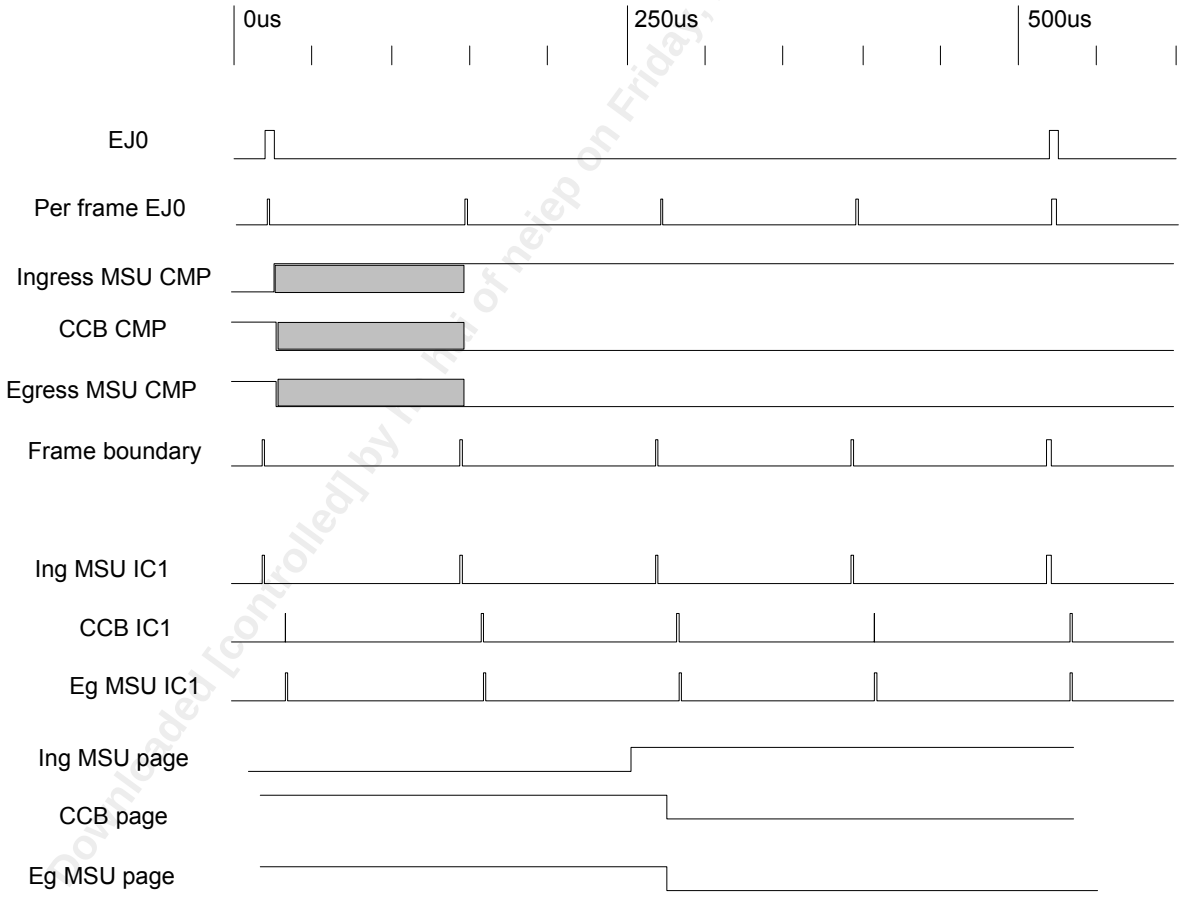
13.8.3 Wideband Column Switching

The TUPP 2488 wideband switching supports low latency, low power switching. The MSUs and CCB are column switches. One row (1080 columns) worth of switch addresses is to be programmed in each block

When doing column switching only one row of the frame structure needs to be stored before switching can take place.

Figure 41 shows the system timing for this mode of operation. A similar approach can apply to any number of SBS devices and NSE external to TUPP 2488s system side.

Figure 41 Column Switching (Hairpinning Example)



In the figure shown, an internal flywheeled, per frame EJ0 is shown. Note that CMP should not change for any switch during the per frame EJ0 pulse, as this is where CMP is sampled for all switches. The IC1(J0) at the input to each switch is shown, along with the location where each switches actual internal CMP changes.

13.8.4 CPU Interaction With the Switching Cycle When Using the ILC

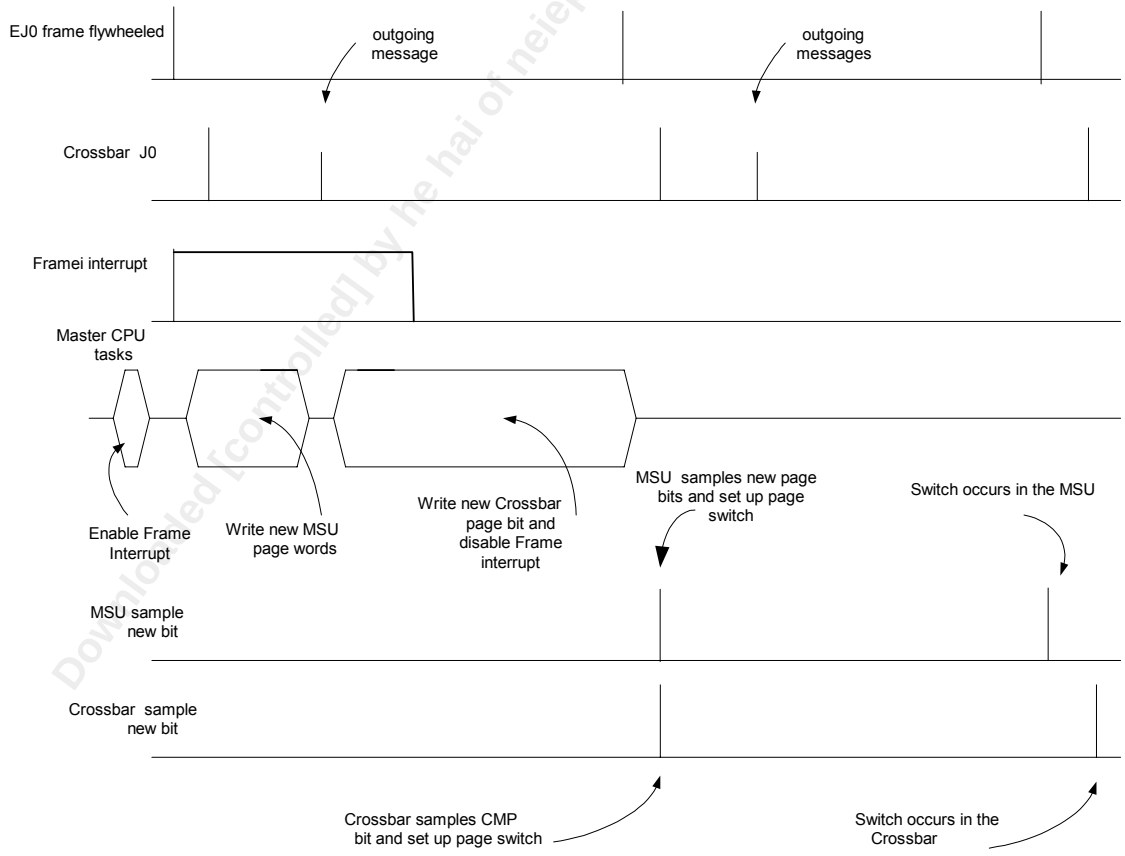
When sending CMP changes via TILC to external devices, care needs to be taken when changing the CMP value. An interrupt is made available to the TUPP 2488 CPU called the Frame Interrupt. This occurs when CMP would normally be sampled (at the EJ0 frame flywheeled pulse). This interrupt is maskable and would normally be masked.

The CPU will need to enable this interrupt before a page switch is required, then respond to this interrupt immediately and complete writing the new page bit settings within 27 µs.

This is required since the TILC will sample the page bits once during the frame before the first message is assembled and sent (starting at the beginning of row 3). If the page bits are updated late, the Slave switches' (MSUs) pages will switch a frame later than those of the Master switch (crossbar) causing 1 frame of data corruption.

The Master's CPU will have the rest of the frame to signal a page switch to the Crossbar as this is sampled on the next frame.

Figure 42 Page Switching Via ILC



13.8.5 Wideband Column Switch Components

The OC-48 wideband switch in TUPP 2488 caters for multicast applications and thus requires 8 OC-12 MSUs in each direction and a 16*OC-12 input CCB. The switching system appears as in Figure 43. Note that the muxes out of the Egress MSUs select (on a per column basis) which of the OC-12 MSUs are sending information onto the OC-12 egress busses. These muxes are controlled by the EMSU_SEL lines which are set up in the MSU configuration RAMs.

Figure 43 OC-48 Wideband Switch Elements

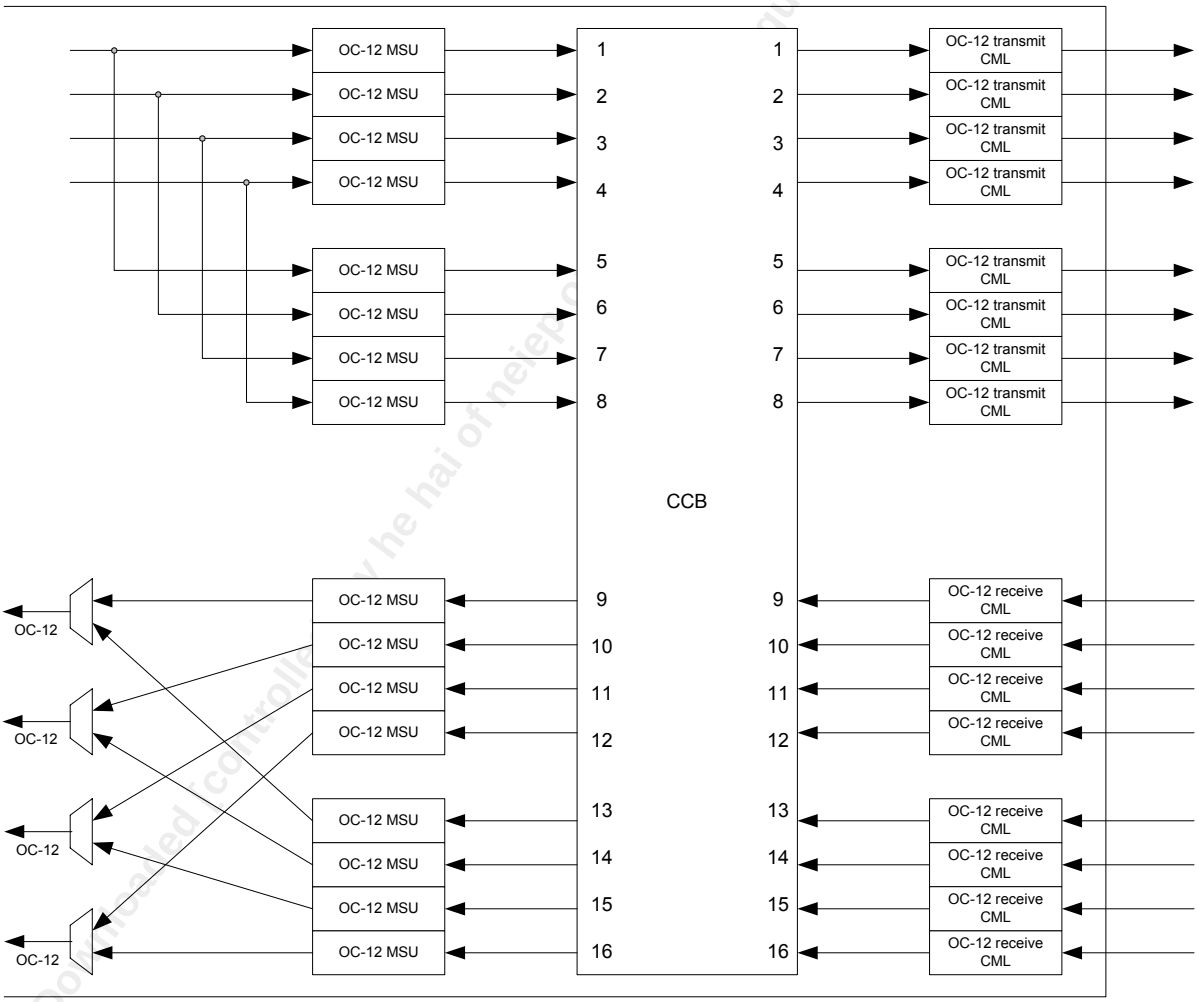
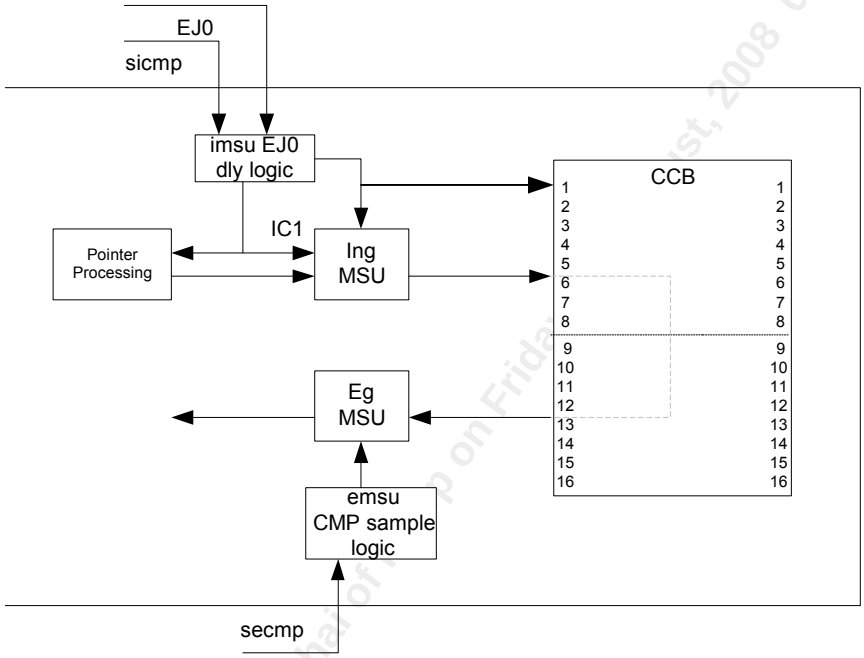


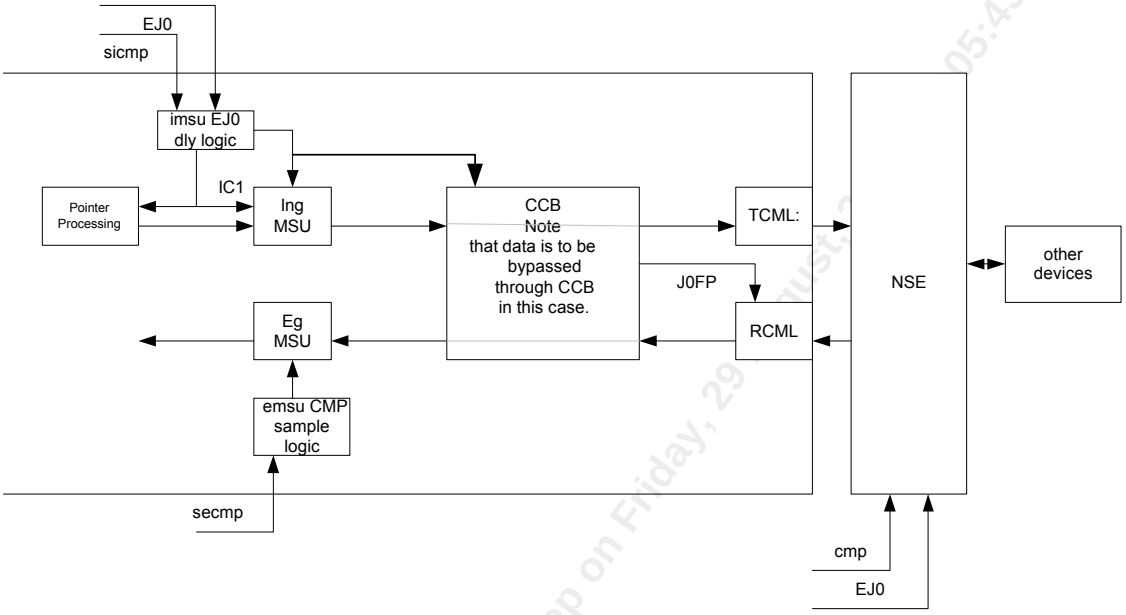
Figure 44, Figure 45, and Figure 46 outline different combinations of switches. The ingress MSUs and egress MSUs are bunched together to simplify the diagrams.

Figure 44 Hairpinning in TUPP 2488



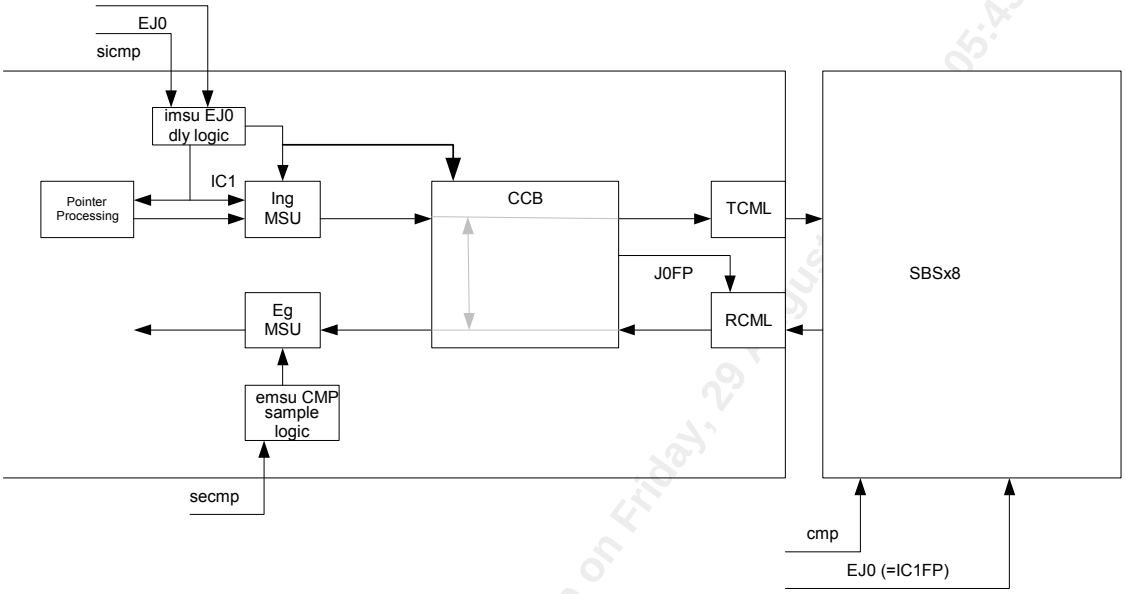
In the above case, the Ingress MSU EJ0 delay value is 0 clocks. CCB internal CMP sampling delay is delay through Ingress MSU.

Figure 45 TUPP with External NSE



When an external NSE is used**,** CCB is bypassed**.** Ingress MSU EJ0 delay value is 0 clocks if NSE is only talking to other TUPP 2488s. If there are also SBS devices concerned, then EJ0 is IC1FP for those SBS devices and the delay is the time between EJ0 and input to TUPP 2488s Ingress MSU. Note that all inputs to DCB within NSE must arrive at the same time. CCB internal delay is to dictate when the J0FP to the RCML block should be sent.

Figure 46 ADM Applications Using CCB



The above diagram shows when the internal CCB is used in an ADM**.** EJ0 is IC1FP for those SBSs and the IMSU delay time is the time between EJ0 and input to TUPP 2488s Ingress MSU. Note that all 16 input data busses to CCB must arrive at the same time. CCB internal delay is to dictate when the J0FP to the RCML block should be sent.

13.8.6 MSU-Lite and CCB Control

There are a number of different methods of changing configuration pages in TUPP 2488. These are outlined in Table 37.

Table 37 Wideband Fabric Switch System Configuration

Application	Block	CMP Source
Hairpin	Ingress MSUs	SICMP pin, or top level register
Hairpin	CCB	SICMP pin, or top level register.
Hairpin	Egress MSU	SECMP pin or top level register
ADM	Ingress MSU	SICMP pin, or top level register
ADM	CCB	SICMP pin, or top level register
ADM	Egress MSU	SECMP pin, or top level register
ADM	External SBS MSUs	CMP pins, top level registers in SBS or via TILC overhead OPage bits
External NSE ADM	Ingress MSU	SICMP pin, top level register or inband via the TILC OPage bits
External NSE ADM	CCB	No switching in CCB - bypassed in this setup and is only used to create reference pulses
External NSE ADM	Egress MSU	SECMP pin, top level register or inband via the TILC OPage bits
External NSE ADM	External NSE	CMP pin or top level pin. NSE can pass Page change info to TUPP 2488 via RILCs.

13.8.7 MSU-Lite Operation

Correct operation of the MSU-Lite requires that the entire time switch control ram be configured. Switching between the two pages of Switch Control RAM is controlled through the CMP input. CMP is only sampled during the C1 byte position of the input frame. A page swap occurs on the first byte of the next frame. The SWAP_PENDINGV bit in the MSU Configuration register reflects the state of the page swap circuitry. When SWAP_PENDINGV is logic 1, a change to CMP has been recognized but the page swap has not yet occurred. When in this state, the Switch Control Ram should not be written to. A change of state of SWAP_PENDINGV can be configured to generate an interrupt by setting the SWAP_PENDINGE bit. Reading the Interrupt Status and Memory Page Update register clears the interrupt.

The MSU provides a mechanism for the on-line page to be copied to the off-line page. To initiate a page copy, the Interrupt Status and Memory Page Update register must be written to. A page copy will take approximately 15us to complete. Page copies may also be done automatically whenever the two pages are swapped. To enable this automated update, the AUTO_UPDATE bit of the MSU Configuration register must be set to logic 1. During a page copy, reads or writes of the time switch ram are not permitted. The UPDATEV bit contains the current status of the page copy circuit and can be used to determine when it is okay to access the time switch ram. The UPDATEI bit is set on a change of state from high to low of the UPDATEV status, indicating that the update is finished and it is once again okay to update the time switch ram. An interrupt can be configured to occur whenever the UPDATEV bit changes state from high to low by setting the UPDATEE bit to a logic 1. This can be used to indicate to the microprocessor that a page update has finished. Reading the Interrupt Status and Memory Page Update register clears the interrupt. The UPDATEI bit is cleared when the Interrupt Status and Memory Page Update register is read.

To perform an indirect read/write to the Switch Control RAM, the following steps must be followed.

Poll BUSY bit

If BUSY bit is low, write to REG offset 03H

Write to REG 02H.

The MSU-Lite has the ability of overwrite its outputs when an invalid address is programmed into the Switch RAM. When a location in the Switch RAM is programmed with bits [13:12] = ‘b11, the value output on the MSU-Lite output signals will be as shown in Table 38. Note that V5 and TPL are unused in the egress path

Table 38 IN_BYTE Format

IN_BYTE						
[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
1	1	MODE[2]	MODE[1]	MODE[0]	Reserved	ODATA[7:0]

Table 39 Overwrite Function Lookup Table

MODE [2:0]	Mnemonic	Setting of Outputs from MSU PL	TPL	J1	V5	Description
000	Overwrite TOH bytes	0	0	0	0	Overwrite output byte with ODATA[7:0] (all rows)
001	Overwrite POH bytes	1	0	1 for 1st row, 0 for rows 2-9	0	Mark byte as a SPE byte (all rows). Mark byte as a J1 byte (first row only). Overwrite output byte with 111111CC (row 6) where CC identifies the frame (1 to 4) of the multi-frame. Overwrite output byte with ODATA[7:0] (rows 1,2,3,4,5,7,8 and 9)
010	Insert STUFF bytes	1	0	0	0	Mark byte as a SPE byte (all rows). Overwrite output byte with ODATA[7:0] (all rows)
011	Diagnostic insertion of V1, V2, V3 and V4 bytes	1	0 for 1st row, 1 for rows 2-9	0	0	Mark byte as a SPE byte (all rows). Mark byte as a tributary payload byte (rows 2 through 9 only). Overwrite output byte with ODATA[7:0] (all rows)
100	Diagnostic overwrite tributary payload	1	1	0	0	Mark byte as a SPE byte (all rows). Mark byte as a tributary payload byte (all rows). Overwrite output byte with ODATA[7:0] (all rows)
101	Diagnostic insertion of V5	1	1	0	1 for 1st row of first frame in a multiframe only, 0 otherwise	Mark byte as a SPE byte (all rows). Mark byte as a tributary payload byte (all rows). Mark byte as a V5 byte (first frame of a multiframe and first row of the frame only). Overwrite output byte with ODATA[7:0] (all rows)
110	Diagnostic insertion of TU 11/TU 12 UNEQ	1	0 for first row, 1 for rows 2-9	0	1 for 2nd row of first frame in a multiframe only, 0 otherwise	Mark byte as a SPE byte (all rows). Mark byte as a tributary payload byte (rows 2 through 9 only). Mark byte as a V5 byte (row 2 of first frame of a

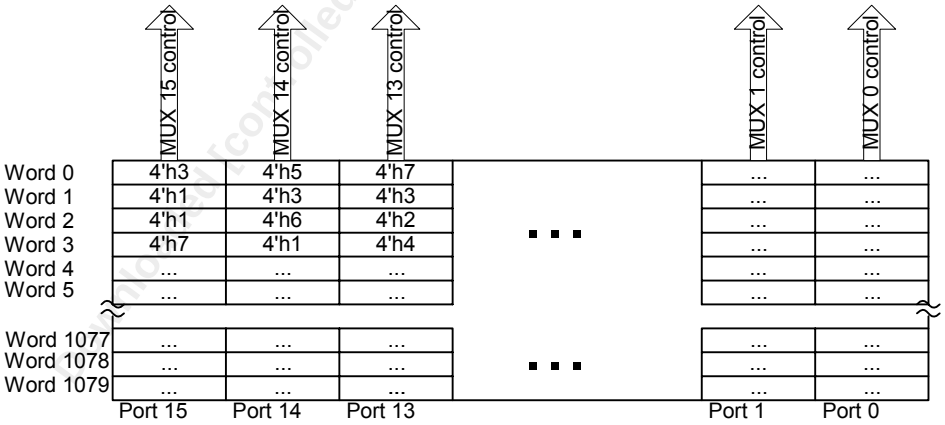
MODE [2:0]	Mnemonic	Setting of Outputs from MSU PL	TPL	J1	V5	Description
						multiframe only). Overwrite output byte with ODATA[7:0] for the first row of the first frame of a multi-frame only (e.g. V1). Otherwise, overwrite the output byte with 0x00.
111	Diagnostic insertion of TU 3 UNEQ	1	0	0	0	Mark byte as a SPE byte (all rows). Overwrite output byte with ODATA[7:0] for the first row only. Otherwise, overwrite the output byte with 0x00.

13.8.8 CCB Operation

Accessing the Connection Page RAMs

The connection memory pages consist of 1080 words of 64 bits per page. Each page stores the different switch setting for the column cross bar switch. A two-page architecture allows a page to be active while the offline page is being updated by the microprocessor. Each connection memory page is further subdivided into smaller partitions so that inactive partitions are powered down. An example of a connection memory page entry is shown in Figure 47 below:

Figure 47 Organization of a Configuration Memory Page



Port Transfer Mode Writing

In port transfer mode the microprocessor updates only one configuration entry within a word of offline connection memory page. The procedure operates in a Read-Update-Write fashion. First the existing configuration is read and internally stored. Then a port mapping is changed and written back to the connection memory page by writing to the Access Mode register. The steps to perform a port transfer are shown in the following example:

Example: If you want to change the cross bar to map the input data bus DIN[7][13:0] to the output data bus DOUT[6][13:0] for just the 1025th column of the frame.

Steps:

1. CPU writes 0x0E6 to the Port Selection register (i.e. PORTCFG[3:0]=0x07, PORTADDR[3:0]=0x06).

2. CPU writes 0x4400 to the Access Mode register (i.e., RWB='1', ACCESS_MODE='0', WORDADDR[10:0]=0x400). This triggers a read from the offline memory connection page at location 0x400.

3. Wait 4 REFCLK cycles. Polling the BUSY bit in the Access Mode register provides a platform independent way of ensuring this condition is satisfied. The BUSY bit will remain high while the read is in progress.

4. CPU writes 0x400 to the Access Mode register (i.e. RWB='0', ACCESS_MODE='0', WORDADDR[10:0]=0x400). This triggers a write to the offline connection memory page at location 0x400 with the updated port configuration.

5. Wait 4 REFCLK cycles before returning to step 1 to perform another mapping change. Again the BUSY bit can be used to ensure this condition is satisfied.

Word Transfer Mode Writing

In word transfer mode, the microprocessor updates an entire word of offline connection memory page. The steps to perform a word transfer are shown in the following example:

Example: If you want to change the entire cross bar mapping from DIN to DOUT for the 1025th column of the frame.

Steps:

1. CPU writes new mapping to the Configuration 3-0 Input Port register.

2. CPU writes new mapping to the Configuration 7-4 Input Port register.

3. CPU writes new mapping to the Configuration 11-8 Input Port register.

4. CPU writes new mapping to the Configuration 15-11 Input Port register.

5. CPU write 0x1400 to the Access Mode register (i.e. WORDADDR[10:0] = 0x400, RWB = '0', ACCESS_MODE = '1'). This triggers a write of WORDCFG to the offline connection memory page at address 0x400. The BUSY bit will remain high while the write takes place.

6. Go to step 1 to begin the mapping change for another column in the frame.

Configuration Reading

It is possible to read configurations from the offline connection memory page. The following example shows this reading operation.

Example: If you want to read which DIN ports map are to the DOUT ports for the 1025th column within the offline connection memory page.

Steps:

1. CPU writes 0x1400 to the Access Mode register (i.e. WORDADDR[10:0] = 0x400, ACCMDE = '1').

2. Wait for 6 REFCLK cycles. The BUSY bit will remain high while the read takes place.

3. CPU reads the mapping from the Configuration Output registers.

Notes

1. The Access Mode register should NOT be accessed more frequently than once ever 4 REFCLK cycles when initiating write transfers.
2. When initiating a read from the offline connection memory page to the Configuration Output register, there is a latency of 6 REFCLK cycles from when a read is initiated till when valid data appears on CFGO.
3. Polling the BUSY bit provides a platform independent way of ensuring the above conditions is satisfied.
4. User should perform this operation only when there is no page swap pending (PAGE_SWAP_PENDINGV = '0') and page copy is inactive (UPDATEV = '0')

Online to Offline Memory Page Copy

There are two ways in which a connection memory page copy can occur: forced and automatic.

- In forced mode, the CPU initiates a page copy by writing to the Interrupt Status & Memory Update register. The page copy begins immediately after being initiated.
- In automatic mode, the AUTO_PAGE_COPY_EN field must be set to '1'. When a connection memory page swap occurs, the online connection memory page is copied to the offline connection memory page.

Interrupt generation to signal the page copying status can be enabled to simplify software scheduling by setting the UPDATEE field in the Configuration register to '1'. In this mode, the UPDATEI field in the Interrupt Status & Memory Update register can be used as the interrupt signal to control the microprocessor.

Alternatively, the microprocessor can poll the UPDATEV field within the Configuration register to detect the status of the connection memory page update logic. '1' indicates copying in progress and '0' indicates copying complete.

Warning: Attempting a page copy while a page swap is pending can lead to corruption of both online and offline memory pages if the page swap occurred while the page copy is in progress.

CCB and J0

In operation all 1080 words of the configuration RAM pages are utilized. This same configuration is repeated 9 times to switch an entire 9720 byte OC-12 frame. Page swaps can occur every frame. CMP input is sampled every frame at the per frame EJ0 location. If enabled, FRAMEI will also occur every frame at the per frame EJ0 position. The OJ0FP output pulse that is used to resynchronize system CML is a delayed version of the per frame EJ0.

Event Sequencing with respect to EJ0

The main reference point available is the FRAMEI interrupt status bit which indicates that sampling of the CMP signal have occurred.

If CMP has changed, the PAGE_SWAP_PENDINGV will be asserted and correspondingly PAGE_SWAP_PENDNGI will be asserted. This indicates that a page swap is pending.

The latency between when CMP is sampled until the actual page change occurs is one frame plus a programmed delay in the top level register bits. When CMP is sampled the page change pending flag is set if a page change is required. Connection memory page swaps can only occur at frame boundaries. The page change pending flag will only be cleared when connection memory page is swapped. If interrupt generation is enabled, an interrupt is generated when a page change takes place. Therefore, caution must be taken when accessing the offline connection memory page after a page swap request.

Attempting to write to the offline connection memory pages close to page swap boundary can lead to corruption of both connection pages. Users are advised NOT to perform write accesses when PAGE_SWAP_PENDINGV is active.

Also, users are advised NOT to perform page copy when PAGE_SWAP_PENDINGV is active.

13.9 Egress SVCA Operation

Refer to the description of the SVCA_R in the payload processing subsystem description (sections 13.6.6 through 13.6.8). Bypass of the egress SVCA_R blocks is not supported.

13.10 HPOH Subsystem Operation

The HPOH Subsystem has three modes of operation:

- Normal Mode
- Loopback Mode

- Transparent Mode

For each mode, all digital blocks should be configured as set out in the register document, while taking into account the comments here.

13.10.1 Normal Operation

Normal mode configures the HPOH to terminate the high order path overhead.

The HPOH Receive Configuration (0020H) register should be configured to reflect the payload configuration of the STS-48/STM-16 stream in the receive (ingress) direction.

The HPOH Transmit Configuration (0021H) register should be configured to reflect the payload configuration of the STS-48/STM-16 stream in the transmit (egress) direction, with HPOH_LBEN=0.

The HPOH Transmit Alarm Preprocessing Configuration (0022H-0025H) registers should be configured to reflect the presence of STS-1/AU3's in the payload configuration of the STS-48/STM-16 stream in the transmit (egress) direction.

13.10.2 Loopback Mode

The HPOH subsystem has a Loopback mode that is enabled by setting HPOH_LBEN=1. In this mode the output of the RHPP_R's are looped back into the THPP_R's.

The HPOH Receive Configuration register should be configured to reflect the payload configuration of the STS-48/STM-16 stream in the loopback.

The HPOH Transmit Configuration register should also be configured to reflect the payload configuration of the STS-48/STM-16 stream in the loopback.

The HPOH Transmit Alarm Preprocessing Configuration registers may be left at its default value.

The SHPIs and SVCA_R's are not active in this mode their interrupt generation mechanisms should be disabled using their internal registers, or else any interrupts from the SHPIs and SVCA_R ignored.

This mode is intended for debugging and validation purposes only.

13.10.3 Transparent Mode

The RHPP_R, THPP_R and SHPI blocks in the HPOH subsystem could be optionally configured into transparent mode (see Table 40). A block configured in this mode performs no functions except passing control signals and data transparently through the block with a fixed pipeline delay. It is recommended to disable all the interrupts to avoid unexpected interrupts when the block is configured in transparent mode.

Table 40 HPOH Functional Block Transparent Mode

Blocks	Applications	Settings	Granularity
RHPP_R	The upstream line side device has a high order path processor. It sends out PL, J0, J1 and PAIS control signals to the TUPP2488 via 777.6 MHz 8B/10B encoded or parallel Telecombus interface. H1H2 could contain invalid value. The PL, J0, J1 control signals and data are transparent through the RHPP_R. The PAIS control signal is passed transparently in the HPOH subsystem.	Set TU3 bit in the RHPP_R to '1'. Set HPOH_RPAIS_BPEN bit to '1'. Ignore SARC-48 receive path processing	STS-48/STM-16
THPP_R	The downstream line side device has a high order path processor. Valid path overheads are inserted in the downstream device. The PL, J0, J1 and PAIS control signals and data are transparent through the THPP_R.	Set the TDIS indirect register bit to '1'.	STS-1/STM-0
SHPI	The upstream system side device has a high order path processor. It sends out PL, J0, J1 and PAIS control signals to the TUPP2488 via 777.6 MHz 8B/10B encoded Telecombus interface. H1H2 could contain invalid value. The PL, J0, J1 and PAIS control signals and data are transparent through the SHPI.	Set the PT_PATH[x] register bit in the SHPI to '1'. Configure SARC-48 transmit path processing (TPAISPTRCFG and TPAISPTREN).	STS-1/STM-0

13.10.4 AU3 to AU4 Conversion

Payloads consisting of AU3's in the transmit (egress) direction may be optionally converted to AU4's by the SVCA. By default, AU3's are not converted to AU4's in the SVCA. To enable AU3 to AU4 conversion set the relevant TUG3 bits high in the SVCA normal mode register 02H.

13.10.5 SHPI Operation

STS-1

- Nothing to configure. Default mode of operation.

STS-3c

- Enable the appropriate STS3C bit (Register offset 02h).

STS-12c

- Either set the top level HPOH_TSTS12C bit to '1' or enable the STS12c register bit (Register offset 02h).

STS-48c

- Configure the first SHPI as a master (STS12C = 1 and STS12CSL = 0) and the remaining 12c slices as slaves (STS12C = 1, STS12CSL = 1).

13.10.6 Making the SHPIs Transparent in Normal Mode

The SHPIs may be optionally made transparent on a per STS-1/AU-3 path basis in Normal mode. This may be required where the SHPI receives valid J1and PL input signals, but not a valid H1/H2 pointer on the incoming data stream.

The internal SHPI Register offset 06H: SHPI PT_PATH Enable should be set accordingly.

13.10.7 TTTP OPERATION

The TTTP generates a one byte, 16 bytes or 64 bytes trail trace message. To generate a one-byte message, BYTEEN register bit must be set to logic one. The trail trace byte is placed at address offset 40H. To generate a 16-byte message, BYTEEN register bit must be set to logic zero and LENGTH16 register bit must be set to logic one. The trail trace message is placed between address offset 40H and offset 4FH. To generate a 64-byte message, both BYTEEN and LENGTH16 register bits must be set to logic zero.

The trail trace message must include synchronization because the TTTP does not add synchronization to the message. The synchronization mechanism is different for a 16-byte message and for a 64-byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has is MSB set high. The byte with its MSB set high is the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 48 One-byte Trail trace Message

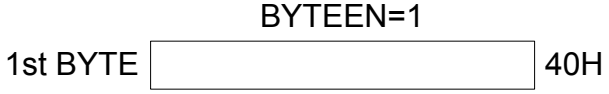
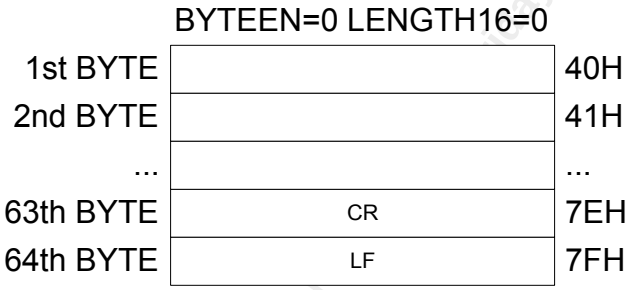


Figure 49 16-bytes Trail trace Message

Figure 50 64-byte Trail trace Message



To avoid generating an unstable/mismatch message, the TTTP can be configured (with the ZEROEN register bit) to generate an all zeros trail trace message while the microprocessor updates the internal message. The enabling and disabling of the all zeros message is not done on message boundary since the receiver is required to perform filtering on the message.

13.10.8 RHPP_R Operation

STS/AU Mode

- Leave the TU3 register at its '0' default in the RHPP_R
  - **STS-1**: Nothing to configure. Default mode of operation.
  - **STS-3c**: Enable the appropriate STS3C bit (Register offset 02h)
  - **STS-12c**: Either set the top level HPOH_RSTS12C register bit or enable the STS12C register bit (Register offset 02h).
  - **STS-48c:** Configure the first RHPP_R as a master (STS12C = 1 and STS12CSL = 0) and the remaining RHPP_Rs as slaves (STS12C = 1, STS12CSL = 1).

13.10.9 THPP_R Operation

To process an STS-48C with 4 slices:

Set to logic one the STS12C bit in the direct register offset 02h for all THPP_Rs. Set to logic one the STS12CSL bit in the direct register offset 02h for the 3 THPP_R slaves.

To process an STS-12C with 1 slice:

Set to logic one the STS12C bit in the direct register offset 02h THPP_Rs

To process 4 VC-4 with 1 slice:

Set to logic one the 4 STS3C bits in the direct register offset 02h THPP_Rs. See the register document for more details on the STS3C register bits.

To process 12 VC-3 in AU-3 with 1 slice

- Default mode

-

- Set to logic one the 4 STS3C bits in the direct register offset 02h for non-TUG3 THPP_Rs. See the register document for more details on the STS3C register bits.

Setting TDIS bit in the indirect register for an STS-48C

- Set TDIS to logic one from the path 1 to path 4 of all the THPP_Rs.

Setting TDIS bit in the indirect register for an STS-12C

- Set TDIS to logic one from the path 1 to path 4 of the THPP_R.

Setting TDIS bit in the indirect register for an STS-3C/VC-4

- Set TDIS to logic one for the path corresponding to the path overhead of the STS-3C of the THPP_R. Path may only be equal to 1, 2, 3 or 4.

Setting TDIS bit in the indirect register for a VC-3 in AU-3

- Set TDIS to logic one for the corresponding path of the VC-3 in the non-TUG3 THPP_R.

-

Fixed stuff bytes insertion for a STS-48C

- Set FSBEN to logic one and FSB[7:0] to the desired value from path 2 to path 4 of the master THPP_R and path 1 to 4 of the 3 slaves THPP_Rs.

Fixed stuff bytes insertion for a STS-12C

- Set FSBEN to logic one and FSB[7:0] to the desired value from path 2 to path 4 of the THPP_R.

Fixed stuff bytes insertion for a STS-3C/VC-4

- No fixed stuff bytes.

Fixed stuff bytes insertion for a VC-3 in AU-3

- Set FSBEN to logic one and FSB[7:0] to the desired value for the corresponding path of the VC-3 in the THPP_R.

-

Setting a payload unequipped for a STS-48C

- Set UNEQ to logic one and UNEQV to the desired value for path 1 of the master and slaves THPP_Rs.

Setting a payload unequipped for an STS-12C

- Set UNEQ to logic one and UNEQV to the desired value for path 1 of the THPP_R.

Setting a payload unequipped for a STS-3C/VC-4

- Set UNEQ to logic one and UNEQV to the desired value for the STS-3C/VC-4 corresponding path: 1, 2, 3 or 4.

13.10.10 Setting a payload unequipped for a VC-3 in AU-3

- Set UNEQ to logic one and UNEQV to the desired value for the corresponding path of the VC-3 in the THPP_R.

-

13.10.11 RTTP Operation

The RTTP monitors a one-byte, 16-byte or 64-byte trail trace message. To monitor a one-byte message, ALGO register bits must be set to 11 (algorithm 3). The trail trace byte is captured at address offset 40H. To monitor a 16-byte message, ALGO register bits must be set to 01/10 (algorithm 1/2) and LENGTH16 register bit must be set to logic one. The trail trace message is captured between address offset 40H and offset 4FH. To monitor a 64-byte message, ALGO register bits must be set to 01/10 (algorithm 1/2) and LENGTH16 register bit must be set to logic zero. The trail trace message is captured between address offset 40H and offset 7FH.

When SYNC_CRLF is low, the synchronization is based on the MSB of the trail trace byte. Only one of the bytes has its MSB set high. The byte with its MSB set high is the first byte of the message. When SYNC_CRLF is high, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 51 One-byte Trail trace Message

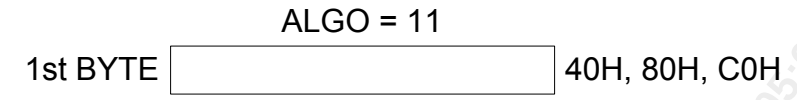


Figure 52 16-byte Trail trace Message, sync on MSB

ALGO = 01/10 , LENGTH16 = 1 , SYNC_CRLF = 0		
1st BYTE	MSB SET HIGH	40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
…		…
15th BYTE		4EH, 8EH, CEH
16th BYTE		4FH, 8FH, CFH

Figure 53 16-byte Trail trace Message, Sync on CR/LF

ALGO = 01/10 , LENGTH16 = 1 , SYNC_CRLF = 1		
1st BYTE		40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
…		…
15th BYTE	CR	4EH, 8EH, CEH
16th BYTE	LF	4FH, 8FH, CFH

Figure 54 64-byte Trail trace Message, Sync on MSB

ALGO = 01/10 , LENGTH16 = 0 , SYNC_CRLF = 0		
1st BYTE	MSB SET HIGH	40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
…		…
63th BYTE		7EH, BEH, FEH
64th BYTE		7FH, BFH, FFH

Figure 55 64-byte Trail trace Message, Sync on CR/LF

ALGO = 01/10 , LENGTH16 = 0 , SYNC_CRLF = 1

1st BYTE		40H, 80H, C0H
2nd BYTE		41H, 81H, C1H
...		...
63th BYTE	CR	7EH, BEH, FEH
64th BYTE	LF	7FH, BFH, FFH

To avoid declaring an unstable/mismatch defect when the transmitter updates the trail trace message, the RTTP considers an all zeros message to be matched. An all zeros captured message in algorithm 1 and an all zeros accepted message in algorithm 2 are not validated against the expected message but are considered match, i.e. a match is declared when the captured or accepted message is all zeros regardless of the expected message. This feature can be turned off by setting the ZEROEN register bit to logic one.

Note: The transmitter is required to force an all zeros trail trace message when the trail trace message is updated.

13.10.12 SARC-48 Operation

Receive Path Processing

The SARC-48 Receive Path processes all path defects detected by the overhead processor and prepares the consequent action indications. Four consequent action indications are defined: the receive path alarm (RPALM, which is connected to chip output HRALM), the receive path AIS insertion (RPAISINS) which is forwarded to downstream Payload Processor Subsystem, the transmit path REI insertion (TPREIINS[3:0]), and the transmit path ERDI insertion (TPERDIINS[2:0]) indications which are forwarded to the transmit THPP_R block.

The first step for generating consequent action indications is to monitor the ALLPAISC, PAIS, PAISC, PLOP, and PLOPC signals in order to generate PAISPTR and PLOPTR defects. With the PAISPTR and PLOPTR defects, the Receive Path can prepare the receive path alarm (RPALM), the receive path AIS insertion (RPAISINS), and the transmit path ERDI insertion (TPERDIINS[2:0]) indications.

PAISPTR alarms are declared according to Equation 2. PAISPTRCFG[1:0] bits exist for each path. A path AIS defect is declared when the selected Equation 1 is true. A path AIS defect is removed when the selected Equation 1 is false. An interrupt is generated when a PAISPTR defect is declared and also when a PAISPTR defect is removed. For slave slices in concatenated payloads, the PAISPTRCFG[1:0] should be left at 00b.

Equation 1:

PAISPTRCFG[1:0]	PAISPTR
"00"	PAIS
"01"	PAIS or PAISC
"10"	PAIS and ALLPAISC
Others	'0'

PLOPTR alarms are declared according to Equations 3 and 4. A path LOP defect is declared when the selected Equation 3 is true. A path LOP defect is removed when the selected Equation 3 is false. An interrupt is generated when a PLOPTR defect is declared and also when a PLOPTR defect is removed. PLOPPTRCFG[1:0] bits exist for each path. Optionally, a PLOPTR defect can be terminated by a PAISPTR defect. The PLOPTREND bit is a register configuration bit that defines if PLOPTR is terminated by PAISPTR or not. A PLOPTREND bit exists for each path. When the PLOPTR is terminated by PAISPTR and this PAISPTR is true the PLOPTR is forced false, in any others case it takes PLOPTR_NOEND value. For slave slices in concatenated payloads, the PLOPTRCFG[1:0] should be left at 00b.

Equation 2:

PLOPTRCFG[1:0]	PLOPTR_NOEND
"00"	PLOP
"01"	PLOP or PLOPC
"10"	PLOP or PLOPC or PAIS or PAISC
Others	'0'

Equation 3:

PLOPTREND	PAISPTR	PLOPTR
'0'	Don't care	PLOPTR_NOEND
'1'	'0'	PLOPTR_NOEND
	'1'	'0'

The receive RPALM indication is defined by Equation 4. The bits from and including PLOPTREN to PTIMEN are register configuration bits that individually enable or disable each defect. The bits exist for each path. The RPALM is indicated on chip output HRALM.

Equation 4:

```
Alarm =    (PLOPTR     AND   PLOPTREN     ) OR
              (PAISPTR     AND   PAISPTREN    ) OR
              (PPLU         AND   PPLUEN       ) OR
              (PPLM         AND   PPLMEN       ) OR
              (PUNEQ       AND   PUNEQEN      ) OR
              (PPDI         AND   PPDIEN        ) OR
              (PRDI         AND   PRDIEN       ) OR
              (PERDI        AND   PERDIEN       ) OR
```

```
                (PTIU        AND  PTIUEN      ) OR
                (PTIM        AND  PTIMEN      )
```

The RPAISINS indication is defined by Equation 5. The bits from and including PLOPTREN to PTIMEN are register configuration bits that individually enable or disable each defect. The bits exist for each path. The RPAISINS is used to insert P-AIS on the receive SONET/SDH stream. PAIS is inserted by inserting an all-ones pattern on the H1-H2 and the SPE bytes. Optionally, it can be inserted on the transport overhead bytes.

Equation 5:

```
Alarm =         (PLOPTR   AND  PLOPTREN    ) OR
                (PAISPTR  AND  PAISPTREN   ) OR
                (PPLU       AND  PPLUEN    ) OR
                (PPLM       AND  PPLMEN    ) OR
                (PUNEQ     AND  PUNEQEN    ) OR
                (PPDI       AND  PPDIEN    ) OR
                (PRDI       AND  PRDIEN    ) OR
                (PERDI      AND  PERDIEN   ) OR
                (PTIU       AND  PTIUEN    ) OR
                (PTIM       AND  PTIMEN    )
```

The Path ERDI[2:0] insertion indication (PERDIINS) is defined in Table 41. A RDIEN bit exists for each path. P-ERDI alarms are used to generate the receive in-band P-RDI alarm. They are also used to return P-RDI to the far-end device.

Table 41 Functional Description of Path ERDI (TPERDIINS) Encoding

RDIEN	PLOPTR or PAISPTR	PUNEQ or PTIU or PTIM	PPLU or PPLM	Path ERDI[2:0] (TPERDIINS)
0	1	Don't care	Don't care	101
	0	1	Don't care	110
		0	1	010
			0	001
1	1	Don't care	Don't care	100
	0	Don't care	Don't care	000

The Received Path detects BIP-8 error. The BIP error count is fed back to the transmit side to be returned as REI-P to the far-end device.

Transmit Path Processing

The SARC-48 Transmit Path processes path defects detected by the egress pointer interpreter SHPI. A consequent action is a transmitted path AIS insertion (TPAISINS) which is forwarded to the egress SVCA_R block. The first step to the generation of the consequent action indications is to monitor the TALLPAISC, TPAIS, TPAISC, TPLOP, and TPLOPC signals generated by the egress path pointer interpreter and to generate TPAISPTR and TPLOPTR defects. With the TPAISPTR and TPLOPTR defects and the external TPAIS information, the Transmit Path can prepare the transmit path AIS insertion (TPAISINS). The TPAISPTRCFG[1:0] bit is the register configuration bit that defines the TPAISPTR defect. Only one TPAISPTRCFG[1:0] bit exists for 48 transmit paths. A transmit path alarm indication signal defect is declared when the selected Equation 6 is true. A transmit path alarm indication signal defect is removed when the selected Equation 6 is false. No interrupt is generated with this defect.

Equation 6:

TPAISPTRCFG[1:0]	TPAISPTR
“00”	TPAIS
“01”	TPAIS or TPAISC
“10”	TPAIS and TALLPAISC
Others	‘0’

The TPLOPTRCFG[1:0] bit is the register configuration bit that defines the TPLOPTR_NOEND defect. Only one TPLOPPTRCFG[1:0] bit exists for 48 transmit paths. The TPLOPTR defect can be optionally terminated by a TPAISPTR defect.

The TPLOPTREND bit is the register configuration bit that defines if TPLOPTR is terminated by TPAISPTR or not. Only one TPLOPTREND bit exists for 48 transmit paths. When the TPLOPTR is terminated by TPAISPTR and this TPAISPTR is true the TPLOPTR is forced to false, in any others case it takes TPLOPTR_NOEND value. A transmit path loss of pointer defect is declared when the selected Equation 8 is true. A transmit path loss of pointer defect is removed when the selected Equation 8 is false. No interrupt is generated with this defect.

Equation 7:

TPLOPTRCFG[1:0]	TPLOPTR_NOEND
“00”	TPLOP
“01”	TPLOP or TPLOPC
“10”	TPLOP or TPLOPC or TPAIS or TPAISC
Others	‘0’

Equation 8:

TPLOPTREND	TPAISPTR	TPLOPTR
‘0’	Don’t care	PLOPTR_NOEND
‘1’	‘0’	PLOPTR_NOEND
	‘1’	‘0’

The transmit path AIS TPAISINS insertion is defined by Equation 9. ADDPAISEN to TPAISPTREN are register configuration bits that individually enable or disable each defect. The bits from and including ADDPAISEN to TPAISPTREN exist for each path.

Equation 9:

```
Alarm =       (TPAIS       AND  ADDPAISEN) OR
              (TPLOPTR     AND  TPLOPTREN) OR
               (TPAISPTR    AND  TPAISPTREN)
```

13.11 RASIO™ CML Transmitter and Receiver Termination

13.11.1 Transmitter Interface Configuration

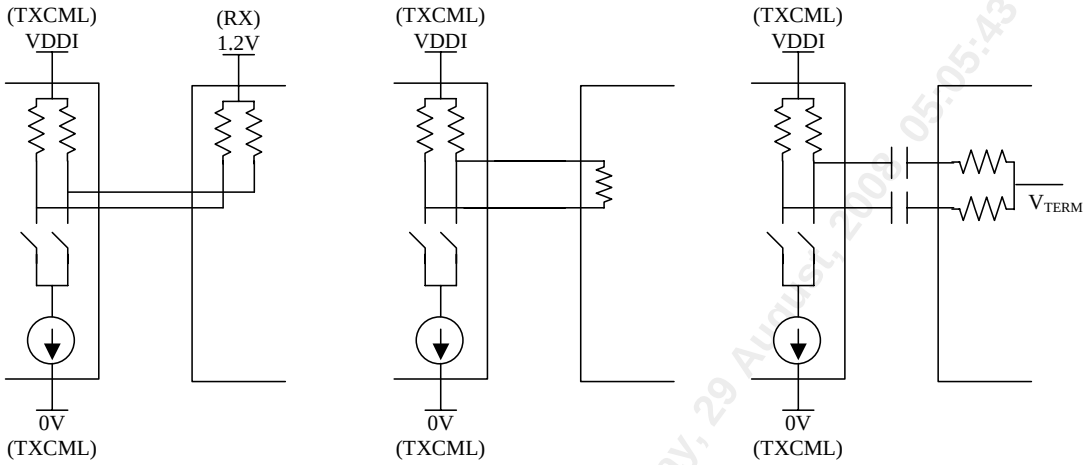
The RASIO™ CML (current-mode logic) transmitter includes an on-chip termination. The transmitter is capable of driving the following types of receiver terminations:

50Ω to 1.2Volt (Figure 56a)

100Ω floating (Figure 56b)

100Ω AC-coupled (Figure 56c)

Figure 56 Transmitter Interface Configurations

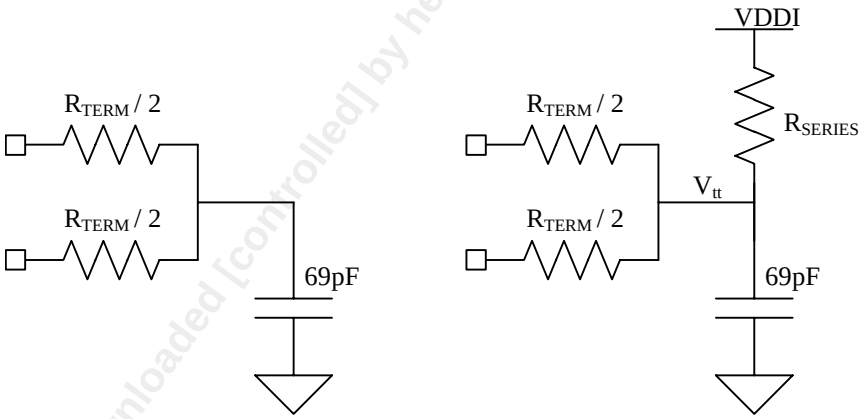


a) 50Ω to 1.2V b) 100Ω floating c) 100Ω AC coupled

13.11.2 Receiver Termination

The receiver termination can be configured to be either floating or to be connected to the 1.2V supply. This can be controlled by the RX_TERM register bit as shown in Figure 57.

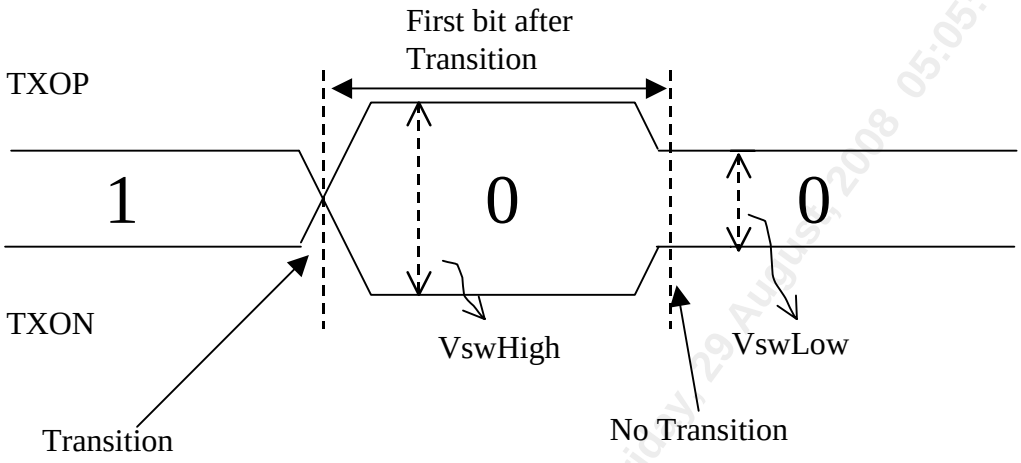
Figure 57 Receiver Termination Modes



13.11.3 Pre-emphasis

When using transmit pre-emphasis, the first bit that follows a transition from 1 to 0 or from 0 to 1 has a greater amplitude than bits that do not follow transitions. This is illustrated in Figure 58.

Figure 58 Output Waveform using Pre-emphasis



This increased amplitude of bits following transitions helps to counteract frequency dependent attenuation incurred with transmission over PCB traces and cables. The high speed RASIO CML transmitter provides programmable ratios of VswHigh to VswLow to provide optimal performance over a wide range of trace lengths.

For guidance on the usage of pre-emphasis, refer to Application Note PMC-2021098.

13.11.4 Receive Equalization

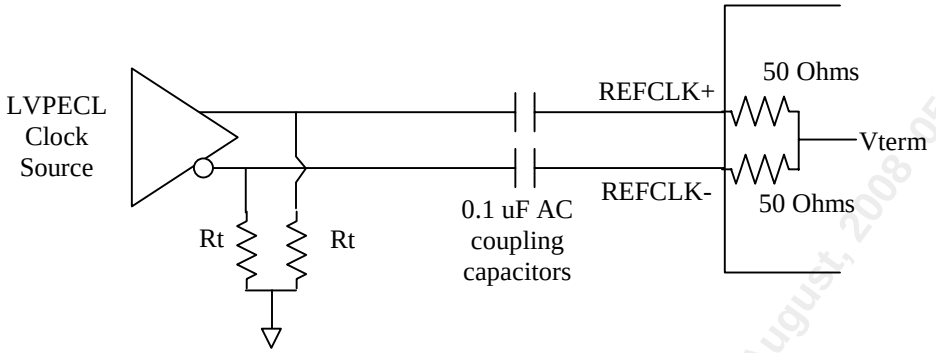
Receive equalization boosts the high frequency content of received signals, counteracting some of the high frequency attenuation incurred with transmission over PCB traces and cables. The RASIO CML receiver provides 3 levels for equalization – no equalization, low equalization, and high equalization level.

High Equalization (RECEIVE_EQ_MODE = 10b) is the default for most applications. However, some system designs may see improved performance with a different Receive Equalization configuration. For guidance on the optimization of receive equalization, refer to Application Note PMC-2021098.

13.11.5 LVPECL REFCLK Inputs

The LVPECL LREFCLK and SREFCLK inputs require AC coupling capacitors between the inputs and the clock source as shown in Figure 59. The LVPECL REFCLK inputs are internally biased and have internal termination resistors therefore no external biasing or terminating resistors for the receiver are required. Resistors are still required to bias the outputs of the LVPECL clock source (Note: Rt value is dependent on the LVPECL driver).

Figure 59 AC Coupling for LVPECL Clock Signal to REFCLK Inputs



13.11.6 Analog Power Filtering

Analog pins supplying power for the CML links should be filtered. Please refer to section 3.2 of PMC-2020238, “TUPP 2488 Hardware Design Guidelines”.

13.12 RASIO™ CML Operation

This section describes the operation of the CML Subsystem and its components. Refer to the TUPP 2488 Register Description document for operation details on the TSEC and PIPM.

13.13 RASIO™ CML Reset Sequence

The reset strategy implemented in the SERDES complicates the CML reset sequence somewhat. Table 42 shows the CML major functional blocks and Table 43 shows the register bits that are used to reset the functional blocks. A suggested reset sequence of the CML subsystems only is also presented as follows.

Table 42 CML Functional Blocks

Functional Blocks	Components
SERDES	PISO_3330, TXCML_3330, RA013_DCRU, RX_3330 and RA013_CSU
Line Side CML	4 RX Slices, 4 TX Slices, one CSU Interface, 4 CML RX Slice and TX Slice Registers
System Side CML	8 RX Slices, 8 TX Slices, one CSU Interface, 8 CML RX Slice and TX Slice Registers
RX Slice	RSEF, PIPM, RILC (system side only), Align FIFO, TIM FIFO, TCB Decoder and DMUX FIFO (line side slice#1 only)
TX Slice	TSEC, TILC (system side only), TIM FIFO, TCB ENCODER and MUX FIFO (line side slice#1 only)

Table 43 CML Reset Register Bits

Register Bit	Number of Bits	Reset Level
SRSET or RSTB (PIN)	1	Device
LSCML_RST	1	Line Side CML
SSCML_RST	1	System Side CML
SS_SERDES_RST	1	System side SERDES block (excluding RA013_CSU).
SS_CSU_RST	1	System side RA013_CSU
LS_SERDES_RST	1	Line side SERDES blocks (excluding RA013_CSU).
LS_CSU_RST	1	line side RA013_CSU
Lx_RX_SLICE_RESET (x=1,2)	4 (line side) 8 (system side)	RX Slice
Lx_TX_SLICE_RESET (x=1,2)	4 (line side) 8 (system side)	TX Slice
Lx_PIPM_RESET (x=1,2)	4 (line side) 8 (system side)	PIPM

CML reset sequence:

1. Assert device reset on RSTB and TRSTB pins.

2. Deassert device reset on RSTB and TRSTB pins.

The performance monitoring circuitry in the RHPP_R, SVCA_R, SHPI, RSEF, PIPM blocks and the CENTER bit of the timing and MUX FIFOs may lock up when the device is reset during a specific timing window. After the device reset, read the LCML_TIP, SCML_TIP and HPOH_TIP bits in register 001DH to ensure they are not set to '1'. If one or more of these bits are set to '1', perform a software reset as follows:

- Wait 5 REFCLK (5x 12.86 ns) cycles.
- Set SRESET to '1' (Master Reset #1: Register 0x0000)
- Wait 200 ns
- Set SRESET to '0' (Master Reset #1: Register 0x0000)
- Wait 100 ns
- Read LCML_TIP, SCML_TIP and HPOH_TIP to ensure they are not set to '1'. If one or more of these bits are set to '1', perform a hardware or software reset again

3. As the subsystem reset in the MPIF defaults to active, deassert subsystem reset by writing to appropriate register in the MPIF (SCML_RST and LCML_RST).

4. The SERDES will be held in reset by default. Take this time to write to the CSUI MPIF registers to configure the CSU. Configuration is not required if an interface is to operate at 622 Mbit/s. If the links are to operate at 777 Mbit/s (system and line side) or 2.488 Gbit/s (line side) the C_MODE[15:0] bits must be configured as follows:

- Set C_MODE[15:0] to the desired value
- Disable overwrite of the C_MODE[15:0] bits by setting CMODE_OVWR to a logic 0.
- Initialize per-channel SERDES registers for both the receive and transmit sides:
- Set the STS48_EN bit to the desired value
- Setup frequency, phase, line rate, etc.
- Enable DCRU, disable test modes. etc.
- Enable transmitter, configure PISO for line rate and data width, etc.

5. Wait for 1 ms.

6. Deassert LS_CSU_RST/SS_CSU_RST.

7. Wait for 1 ms.

8. Deassert LS_SERDES_RST/SS_SERDES_RST.

9. Wait for 10 ms.

10. Deassert slice resets, if asserted in step 4.

11. Configure the device once lock has been achieved.
    - Configure the receive 8B/10B decoding option, 622NRZ mode and de-scrambling mode.
    - Configure the transmit 8B/10B encoding option, A1A2 insertion, B1 re-calculation and scrambling mode.
    - Center all the transmit TIM FIFOs and MUX FIFOs (2488 mode only).

The CENTER circuitry in the timing and MUX FIFOs may lock up when the device is reset. Center the timing and MUX FIFO's by writing a logic 1 to the Lx_CENTER_MUXTX and Lx_CENTER_TIMTX bits of the CML Tx Slice Config Register and then read the bits after the first device centering operation to ensure they are not set to '1'. If one or more of these bits are set to '1', write the bits to a logic '0' to remove the lockup condition. Checking for the lockup condition is only necessary after the first centering operation.

13.13.1 Configuration of the RSEF

Once the RSEF has been brought out of reset, all interrupts within the block are masked by default. Since the initial RSEF input data is not character aligned, it is recommended that the LCVI and BIP8I interrupts remain masked until character alignment has been achieved.

With a valid bit stream, character alignment will occur after one frame and frame alignment after two frames. In 8B/10B mode, if an LCV occurs after character alignment and before frame alignment, then frame alignment is delayed by CLEAN_FRM_CNT frames. Setting CLEAN_FRM_CNT to 0 (its default) disables this feature. Setting this value to 3 is recommended and makes the framing algorithm more robust against false frame when a link is floating.

By default, the RSEF will go out of character alignment if the number of LCVs in a 15-character window exceeds four. This can be changed by setting the LCV_OOF_ERROR threshold through the MPIF. Setting LCV_OOF_ERROR to 0 provides immunity to a possible false framing pattern such as a single K28.5 character followed and entire frame of AIS characters and is the recommended setting. The higher this value, the more tolerant the RSEF is of LCVs without losing character alignment.

13.13.2 TILC and RILC Operation

The TILC and RILC implement the Transmit and Receive functions of the ILC (Inband Link Controller). They transmit and receive inband commands and control information between serial links. These sit only on the system side CML of TUPP 2488.

Table 44 Inband Message Header Fields

Field Name	Purpose
LINK[1:0]	Indicates which Link to use. The protocol of the bits in specifying Working or Protecting Link is up to software. Transmitted immediately.
PAGE[1:0]	Each bit indicates which control page to use, page 1 or 0, two bits, bit 1 for the ingress and bit 0 for the egress. Only transmitted from beginning of the first message in the frame.
USER[2:0]	User defined register indication to reflect hardware signal outputs. Transmitted immediately.
AUX[7:0]	User defined auxiliary register indication. Transmitted immediately.

These bits will not be processed by the receive block if the received message CRC-16 indicates an error.

Interrupts can be generated when the USER[0] bit changes state to a '1'. There is no inherent flow control provided by the Inband Link Controller. The attached microprocessor is able to provide flow control via interrupts when the inband message FIFO overflows and via the USER[0] bit in the header.

13.13.3 Transmit Inband Link Controller Microprocessor Interface

Message Transmit Registers

- Two 16-bit registers to which the TX microprocessor writes the 32 bytes of information to be transmitted in the message payload.
- A Transmit Control register that allows the configuration of Transmit message header bits, TX_AUX, TX_LINK. This register also enables CRC-16 swizzling (reversal) in the transmit logic for use in diagnostic testing and verification of ILC. This register also contains the TX_BYPASS bit that disables the ILC message transmit.
- A Transmit Status Register (RO) that returns status from the message transmit logic indicating number of messages queued for transmit and the transmit FIFO busy status. Also contained in this register is the status of the transmit header bits that are controlled through ILC inputs, PAGE and USER. The TX_LINK value is read shadowed here to allow for one location that shows the value of the Header1 bits.
- A Transmit FIFO Synch Register (WO) that aligns the write message pointers to the start of a message and facilitates the use of short messages

Note

- The Transmit Status Register and Transmit FIFO Synch Register share the same address.

13.13.4 Transmit CPU Operations

Accessing the Transmit Message FIFO

When writing to the transmit FIFO in the TILC, the following procedure should be followed:

1. Write a logic 1 to the TX_XFER_SYNC bit of the Transmit Status and FIFO Synch Register. This will ensure the subsequent writes to the FIFO start at the beginning of a message.

2. Write to the Transmit FIFO Data Low and Transmit FIFO Data High registers. Writing to the Transmit FIFO Data Low register will initiate a transfer of the Transmit FIFO Data Register into the transmit FIFO.

3. Read the TX_FI_BUSY bit in the Transmit Status and FIFO Synch Register or wait a minimum of 3 REFCLK cycles. If TX_FI_BUSY is a logic 0, continue to step 4. If it is a logic 1, continue polling the TX_FI_BUSY bit.

4. Loop back to Step 2 until the entire message has been written in to the FIFO.

When transmitting multiple 32 byte messages, the TX_XFER_SYNC bit does not have to be written to between each message.

When transmitting a message shorter than 32 bytes, the TX_XFER_SYNC bit should be set after writing the last byte of the message into the FIFO. This will allow the short message to be transmitted and move the FIFO to the next 32 byte partition.

Handling the Transmit Header

PAGE Bits

If the IPAGE bits are changed, they are not sent in the header bits until the next frame. They will be continually sent for each message in subsequent frames until they change again.

USER, LINK and AUX Bits

When any of these bits change they are sent in the header bits of the next message. They will be continually sent for each subsequent message until they change again.

Bypass Function

TILC transmit function can be disabled by writing a ‘1’ to TX_BYPASS in the Transmit Control register. When in bypass mode the message FIFO ram is disabled and writes to the transmit FIFO are ignored.

The TILC functions as a two-stage pipeline in bypass mode.

13.13.5 Receive Inband Link Controller Microprocessor Interface

Message Receive Registers

- Two 16-bit registers (Receive FIFO Data), from which the RX microprocessor reads the 32 bytes of information that have been received in the message payload.
- A Receive Control register that is used to enable CRC-16 swizzling (reversal) in the receive logic for use in diagnostic testing and verification of ILC.

- A Receive Status Register (RO) that returns status from the message receive logic indicating number of messages received and stored in the Receive FIFO and the receive FIFO busy status. Also contained in this register is the status of the received header bits, LINK, PAGE and USER.
- A Receive Auxiliary Register (RO) is used o return the status of the received AUX bits.
- A Receive FIFO Synch Register (WO) that aligns the read message pointers to the start of a message and facilitates the use of short messages and skipping of message buffers.

Note

- The Receive Status Register and Receive FIFO Synch Register share the same address.

Interrupt Registers

- An Interrupt Enable and Control Register is used to enable interrupts for different events and configure interrupt variables such as thresholds and timeouts.
- An Interrupt Reason Register indicates status of each of the interrupt events. The status of these bits is updated irrespective of whether the corresponding interrupt enable is set or clear.

13.13.6 RILC CPU Operations

Accessing the Receive Message FIFO

When reading messages from the receive FIFO in the RILC, the following procedure should be followed:

1. Write a logic 1 to the RX_XFER_SYNC bit of the Receive Status and FIFO Synch Register. This will initiate a read from the receive FIFO.

2. Read the RX_FI_BUSY bit in the Receive Status and FIFO Synch Register or wait a minimum of 4 SYSCLK cycles. If RX_FI_BUSY is a logic 0, continue to step 3. If it is a logic 1, continue polling the RX_FI_BUSY bit.

3. Read the Receive Status and FIFO Synch Register and check the state of the CRC_ERR. If this bit is a logic 1, the current message in the FIFO had a CRC error and the data is not reliable and the user may want to skip to the next message.

4. Read the Receive FIFO Data High and Receive FIFO Data Low Registers.

5. Read the RX_FI_BUSY bit in the ILC Receive Status and FIFO Synch Register or wait a minimum of 4 SYSCLK cycles. If RX_FI_BUSY is a logic 0, continue to step 6. If it is a logic 1, continue polling the RX_FI_BUSY bit.

6. Loop back to Step 4 until the entire message has been read out of the FIFO.

When reading more than one message from the receive FIFO, the RX_XFER_SYNC does not have to be set between each message.

Before reading any messages, the software may want to check how many messages are contained in the receive FIFO. This can be done by reading the RX_MSG_LVL[3:0] bits in the Receive Status and FIFO Synch Register. When reading these bits, the RX_STTS_VALID bit must also be checked. If RX_STTS_VALID is a logic 1, the RX_MSG_LVL[3:0] bits are valid. If RX_STTS_VALID is a logic 0, the RX_MSG_LVL[3:0] bits are not valid and this register should be read again until RX_STTS_VALID is a logic 1.

Receive Message Header Bytes

PAGE, USER. LINK, an AUX Bits

The receive message header is available in the Receive Status and FIFO Synch Register. The information in the register is only updated when the receive message CRC is correct.

Handling Interrupts

All interrupts are masked on startup, and should not be enabled until the link initializes.

Bypass Function

RILC receive function can be disabled by writing a '1' to RX_BYPASS in the Receive Control register. When in bypass mode the message FIFO ram is disabled and reads from the receive FIFO return random data.

The RILC functions as a two-stage pipeline in bypass mode.

13.14 TUPP 2488 SERDES and CSU Operations

Configuration bits for the SERDES and CSU are all described in full in the register description for TUPP 2488. The recommended default settings should be used for SERDES and CSU.

13.15 Receive RASIO™ CML Link Electrical Monitoring

Each RSEF block incorporates a DC balance monitor, a consecutive identical digit (CID) detector, and a transition detector. The monitors optionally forces the state machine into the out of frame alignment condition should the quality of the received data stream degrade. The contribution of the DC balance / CID / transition monitors to the RSEF state machine is enabled by setting the CID_TRAN_DC_EN bit to a logic 1. Electrical monitoring is recommended for links configured for scrambled NRZ mode only (i.e. operating at 622 Mbit/s or 2.488 Gbit/s) as 8b/10b encoded links operating at 777 Mbit/s ensure adequate transitions and DC balance.

13.15.1 DC Balance Monitor

The DC balance monitor has 3 programmable parameters to provide sufficient flexibility in modeling the external link. The three parameters are the decay period (DECAY_PER), the decay factor (DECAY_FAC) and the threshold (DC_BAL_THRESH).

Figure 60 compares the actual decay of the DC voltage on a link with the value calculated by the DC balance monitor. The time constant is 10 ms and the input is assumed to have a balanced number of ones and zeros. The smooth exponential curve is the actual voltage. The approximation with smaller steps uses a decay factor of 1/8 and a decay period set to 430. The second approximation uses a decay factor of 1/4 and a decay period of 850. The DC_BAL_EN bit must be set to logic 1 in addition to setting the CID_TRAN_DC_EN bit to logic 1 for the DC balance monitor to be enabled.

Figure 60 DC Balance Decay

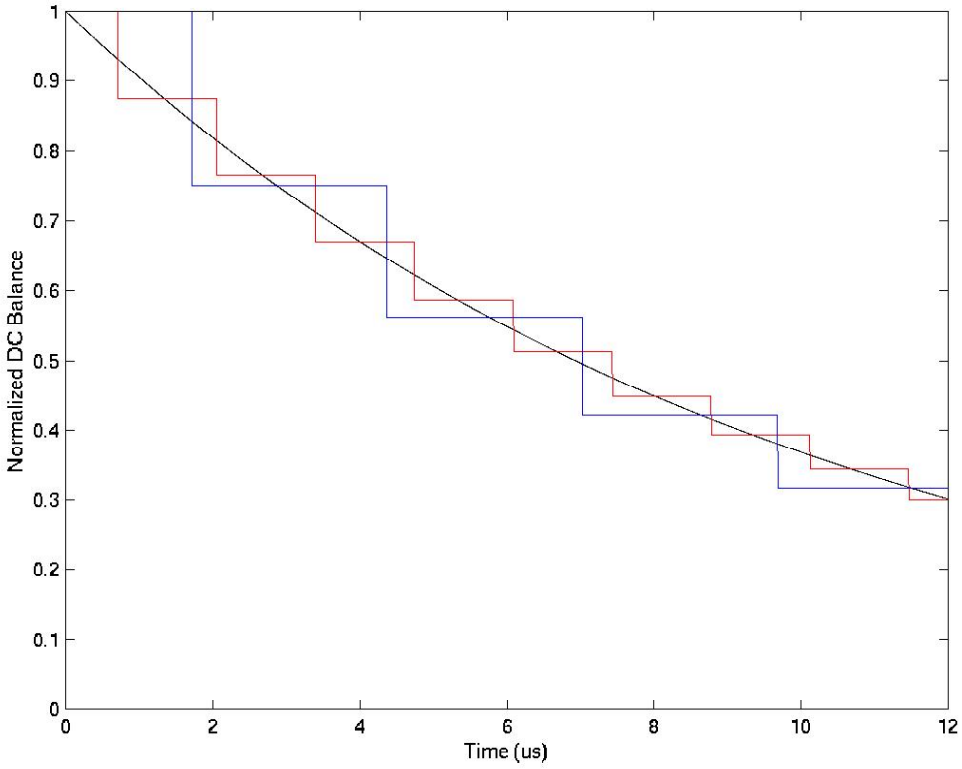
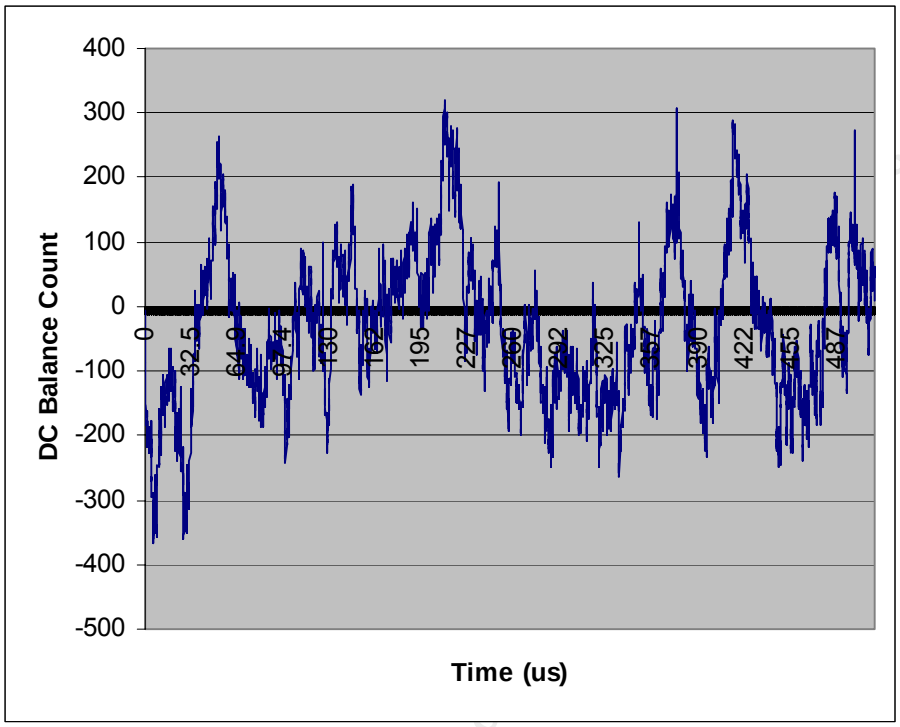


Figure 61 shows the DC balance count over a few frames times with scrambled random data. The decay period is set to 430 and the decay factor is 1/8. Simulations have shown that random data with no bias has maximum DC balance counts of approximately +/-350. With 51% ones and 49% zeros the maximum DC balance counts are around +/-900. Normal SONET data will have a ones density between 49.5% and 50.5% a threshold of 1000 is recommended.

Figure 61 DC Balance Count with Random Data



Suggested settings for DECAY_PER, DECAY_FAC and DC_BAL_THRESH are 108, 1/8, and 500 for 622 Mbit/s links and 430, 1/8, and 1000 for 2.488 Gbit/s links, respectively. The numbers given are to be used guidelines. It is recommended that simulations be run to derive parameters for specific applications.

The parameters that configure the DC balance should not be changed while the device is in normal operation as the effects are non-deterministic and may cause spurious errors.

13.15.2 CID Detector

The recommended setting for the CID threshold is 16 for both 622 Mbit/s and 2.488 Gbit/s links. A threshold of 16 will produce an error if 128 to 135 CIDs are received. The exact number required to generate an error depends on the byte alignment. For example, a CID threshold of 16 bytes (128 bits) may take up to 17 bytes of consecutive ones or zeroes to trigger the CID interrupt and force the RSEF out of frame alignment.

The CID_EN bit must be set to logic 1 in addition to setting the CID_TRAN_DC_EN bit to logic 1 for the CID detector to be enabled.

13.15.3 Transition Detector

Normal SONET data has a ones density between 49.5% and 50.5% over a large data sample. Simulations with random data having a ones density of 55% have shown that the minimum number of transitions in 255 bytes is 898 (44.0%). To configure the transition detector the transition threshold must be set to one of the values enumerated in Table 45. The suggested setting for both 622 Mbit/s and 2.488 Gbit/s links is 7.

Table 45 Transition Thresholds

TRAN_THRESH[2:0]	Threshold	Transition Density
0	disabled	disabled
1	128	6.3%
2	256	12.5%
3	384	18.8%
4	512	25.1%
5	640	31.4%
6	768	37.6%
7	896	43.9%

13.16 Bypasses

There are a number of bypasses available in the TUPP 2488 used for device debug. Some bypasses are also required for normal applications to work correctly.

13.16.1 MSU-Lite Bypasses

Each bank of MSUs can be bypassed separately. The top level registers to do this are IMSU_BYPASS and EMSU _BYPASS. These bypass the entire STS-48 (4 MSUs) since bypassing the MSUs individually will cause latency mismatches between different OC-12s.

Bypassing MSU has the exact effect of sending column 1 input to column 1 output etc. (but avoids the need of setting up configuration RAMs with a 1 to 1 mapping). This should only be used when debugging the device.

13.16.2 CCB Bypass

CCB can be bypassed by asserting the CCB_BYPASS register. This bypasses the entire STS-192 worth of information through the CCB. The main use of this feature is described in Figure 45.

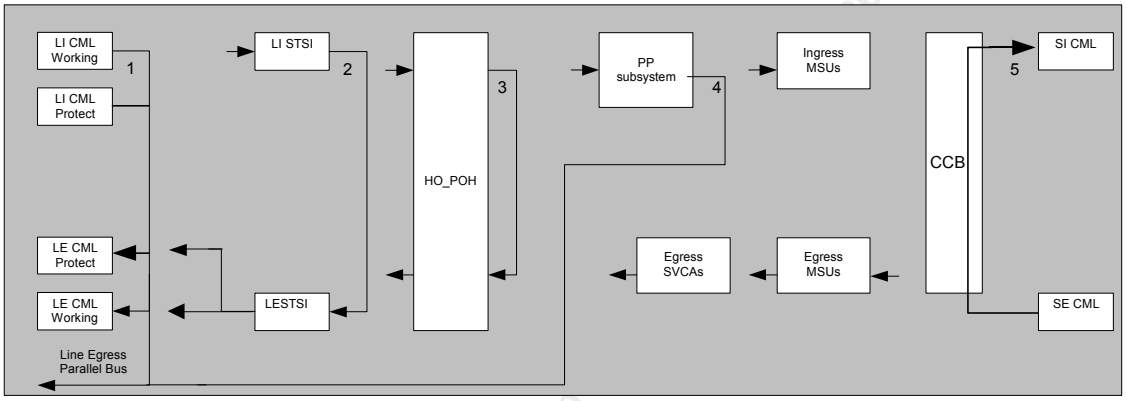
13.16.3 ILC Bypasses

The TX_BYPASS and RX_BYPASS in the TILC and RILC respectively bypass the message transmission and receive capabilities of the ILC blocks. All signals passing through the ILCs are unaffected.

13.17 Loopbacks

There are a number of Loopback options provided in TUPP 2488. These are mostly to aid debug but some are also used in everyday applications.

Figure 62 Loopbacks in TUPP 2488



The Loopbacks in Figure 62 are described in Table 46.

Table 46 Loopback Options in TUPP 2488

Loopback	Description	Register	Comment
1	Line Loopback	LLBEN	Can also Loopback to the Egress Parallel Bus.
2	STSI Loopback	STSI_LBEN	Write passthru switch settings for STSI bypass
3	HO-POH Loopback	HPOH_LBEN	—
4	PP Subsystem Loopback	PP_LBEN	Loopback from the Payload Processor outputs to the Line Egress Parallel Outputs. Used for parallel Payload Processing only applications.
5	System Loopback	Configure CCB	Write loopback switch settings for CCB connection memory.

- You can disable the line egress parallel bus by setting the LINE_EG_PAR_DISABLE register to save power when using the Line Serial links.
- Ti_MLBEN: Enable Transmit Metallic Loopback – also assert Ri_MLBEN
- Ri_DLBEN: Enable Receive Diagnostic Loopback – also assert Ti_DLBEN
- Ti_DLBEN: Enable Transmit Diagnostic Loopback – also assert Ri_DLBEN
  - o
  - o LEPROT1-LIPROT1
  - o SIPROT6-SEPROT8
  - o SIPROT5-SEPROT7

- SIPROT2-SEPROT4
- SIPROT1-SEPROT3
- SIWORK6-SEWORK8
- SIWORK5-SEWORK7
- SIWORK2-SEWORK4
- SIWORK1-SEWORK3

13.18 System Egress Working Vs. Protect

In the System Egress, data can come from both working and protect sources. When operating TUPP 2488, the user must chose between working and protect.

To do this, assert the SEWSEL input to select the working path for all lines on the system egress if the SEWSEL_SRC register is high. Must be stable at least two clocks before it is sampled. If SEWSEL_SRC is low, then the value in SEWSEL_VAL selects working (0) or protect (1).

All system side working protect changes are synchronized to the next frame boundary at the working/protect boundaries.

13.19 Line Ingress Working Vs. Protect

In the Line Ingress data can come from both working and protect sources.

On the Line Ingress side, there are two options for working/protect selection. If the LIWSEL_EN register is set then LIWSEL operates in the same way as SEWSEL and overrides the ingress STSI LIWTSEN bits. If the LIWSEL_EN register is cleared then the programmable bits in the STSI are used. These are set per STS-1.

Taking STS-1 #1: if the programmable bit for this is cleared in the WORKING STSI (LIWTSEN), then the working STS-1 #1 is passed through. To pass through protect links, assert LIWTSEN. All line ingress working protect changes are synchronized to the frame boundary at the working/protect location. Software (TSEN) settings occur on the frame boundary after change. Hardware (LIWSEL) changes occur on the second frame boundary after change.

If using the parallel ingress inputs, then LINE_PARALLEL register is set high. In this case the user should set the LIWSEL to working.

13.20 Programmable I/O Operation

The Programmable I/O should be set to the required voltage values as per register 001Fh in the master registers (2.2v or 3.3v). MPI_HV controls the MPIF data bus to 2.5v or 3.3v and EGR_HV programs the Parallel Egress bus and the REFCLK input.

Pullups may also be enabled using EGR_PUEN and MPI_PUEN (these default to ON). Note that there is no pullup option on REFCLK input.

13.21 DLL Operation and Recovering from Clock Failure

When the DLL comes out of reset its EXTEND bit should be set to '1' to enable the DLL to operate at 77.76 MHz. When the DLL achieves zero phase offset between the REFCLK pin and the internal device REFCLK it asserts the RUN bit in the DLL status register 0123h.

The DLL can be bypassed using the OVERRIDE bit, or force a phase offset using the VERN_EN and VERNIER bits.

If the DLL is unable to achieve phase lock on the REFCLK and core REFCLK signals it asserts the ERRORI interrupt.

If the phase offset changes the CHANGEI interrupt is asserted.

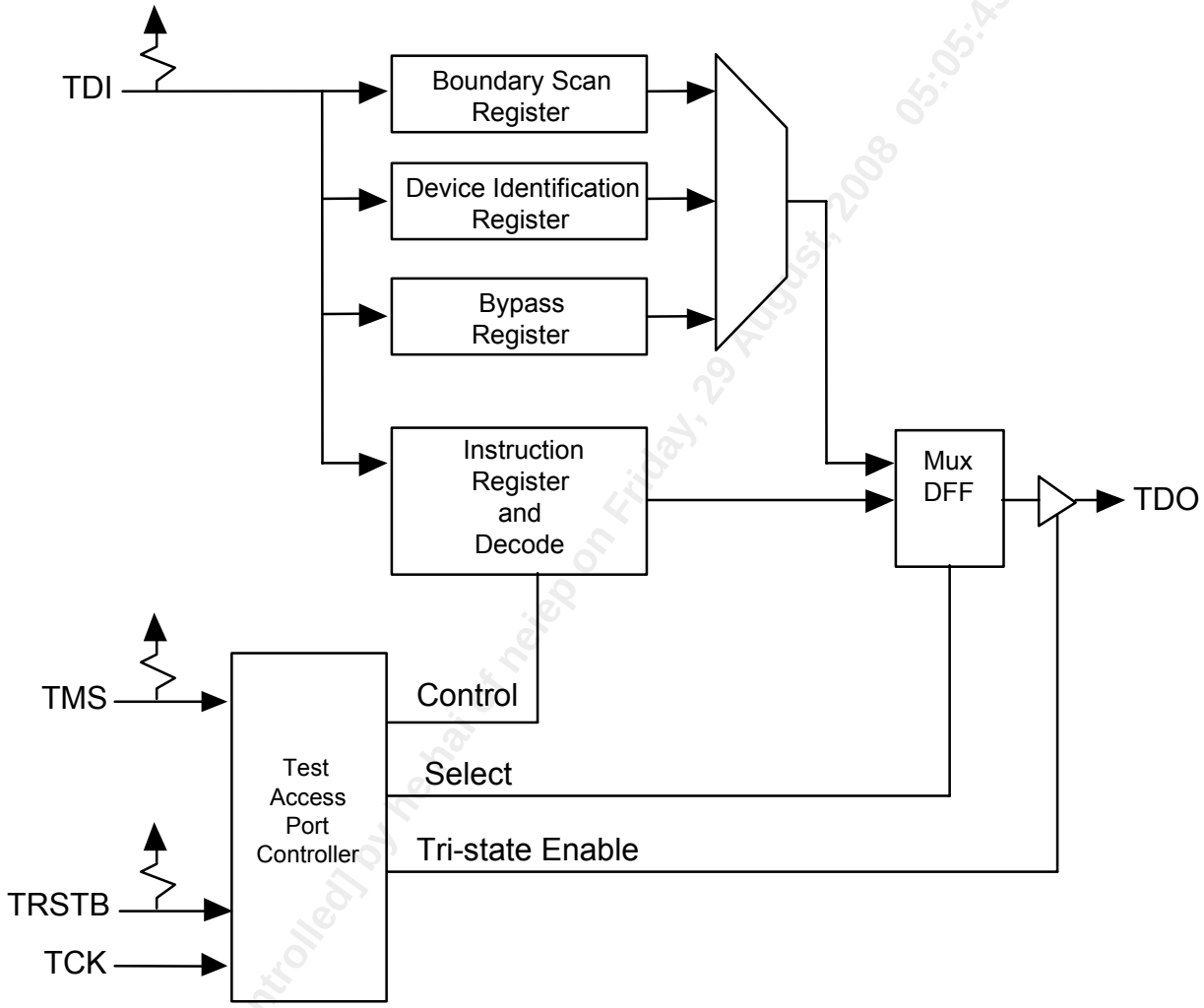
The TUPP2488 has limited capability to detect REFCLK clock failures. When the REFCLK input is disabled and the serial line side is configured for 2.488 Gbit/s operation, the transmit DMUX FIFO's will report a FIFO error. Re-centering of the FIFO is required to resume normal operation. The DLL REFCLKI bit can be used to monitor activity, check the bit periodically to ensure REFCLK is active.

Correct operation of the devices requires the REFCLK device input to operate at the specified frequency. The DLL will report an ERRORI interrupt if the REFCLK frequency is significantly less than or greater than the recommended frequency. Internal timing paths within the device will fail under such circumstances and device behavior is not guaranteed. Soft or hard reset of the device is required to resume normal operation.

13.22 JTAG Support

The TUPP 2488 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 63.

Figure 63 Boundary Scan Architecture



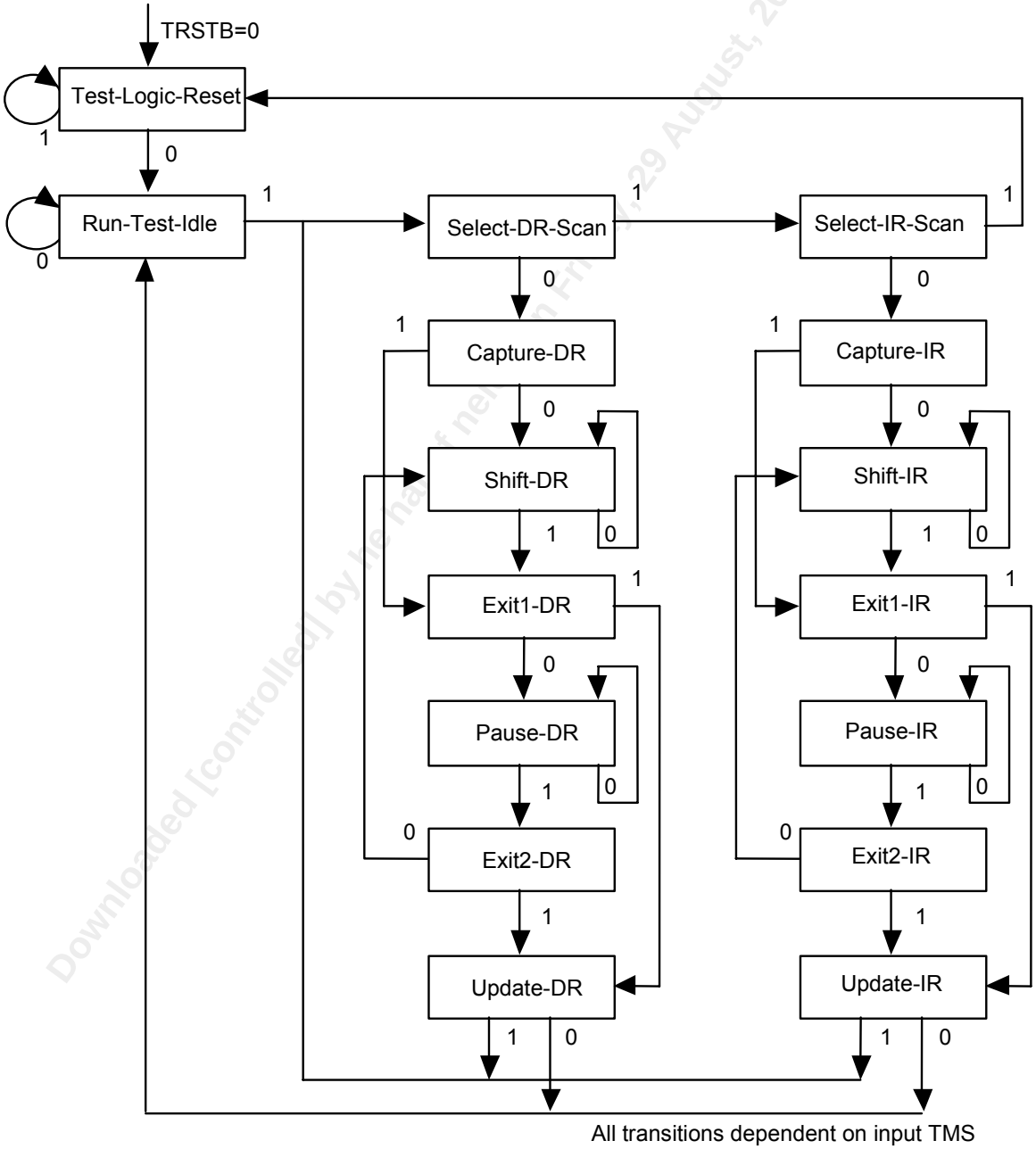
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.22.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 64 TAP Controller Finite State Machine



13.22.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.22.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.22.4 Limitation

The LEWORK_P/N [4:1], LEPROT_P/N [4:1], SIWORK_P/N [8:1] and SIPROT_P/N [8:1] pins on the TUPP 2488 device are not fully compliant with IEEE 1149.1 JTAG. These pins respond correctly to the JTAG EXTEST instruction, but do not respond correctly to the SAMPLE and BYPASS instructions. During the SAMPLE and BYPASS instructions, these pins are driven by the JTAG controller with a steady state value. According to the JTAG standard, the correct behavior during SAMPLE and BYPASS instructions is to allow normal data activity to continue on the pin.

All other high speed receivers LIWORK_P/N [4:1], LIPROT_P/N [4:1], SEWORK_P/N [8:1] and SEPROT_P/N [8:1]) and low speed I/Os are fully compliant with the IEEE 1149.1 standard and support all relevant test and debug operations.

13.23 Performance Monitor Clock

The performance monitor clock is used to transfer the content of the performance counters and then reset the counters. It is recommended to assert performance clock for one second, but it is not required. The RHPP_R, SHPI, SVCA, VTPI, RTOP and VTPA functional blocks prefer one second of clock period to accumulate various events. The RSEF and PIPM blocks do not have preference.

There are three ways to assert LCLK in TUPP2488:

Internally generated one-second performance monitor clock

- Set LCLK_SRC bit to logic ‘0’.

Software controllable performance monitor clock

- Set LCLK_SRC bit to ‘1’ and assert LCLK pin to ‘0’.
- Toggle LCLK_VAL bit.

External performance monitor clock using LCLK pin

- Set LCLK_SRC bit to logic ‘1’ and LCLK_VAL bit to logic ‘0’.

13.24 Unreliable Interrupt Indications in VTPA

When configured to process TU3 payload, some VTPA interrupt bits are unreliable if the automatic PMON transfer features are used.

The affected VTPA interrupt bits include:

ESEI - This bit indicates if an Elastic Storage Error (ESE) event has occurred.

PJEI - This bit indicates if a positive pointer movement has occurred

NJEI - This bit indicates if a negative pointer movement has occurred

OVR - This bit indicates if a previous transfer has not been acknowledged (an indirect read has not occurred)

PEND - This bit indicates is asserted when the LCLK is triggered and is cleared when it is read.

The other register bits such as the ESEV, PJEV, NJEV, PJE[12:0], NJE[12:0] in the VTPA are not affected by this. In addition, the TRIB_INT[x][y][z] bits are functioning proper. This means when the ESEE bit is set to 1, the TRIB_INT[x][y][z] will indicate a ESE interrupt status reliably.

To address this issue, a hardware workaround and a software workaround are available.

Hardware:

The VTPA interrupt bit will only be unreliable when the LCLK is triggered at the moment when the VTPA is processing the fixed stuff byte right below the TU3 H3 byte. The hardware workaround is to control the assertion time of the LCLK pin to avoid this byte. Since the AU4 H1/H2 pointer is fixed to 522 or 0, the TU3 pointer as well as the sensitive byte will be in a known location in reference with the system-side frame pulse (EJ0).

Internally generated one-second performance monitor clock and software controllable performance monitor clock can not be used in this situation.

If the LCLK can be controlled to avoid this sensitive byte, the VTPA interrupt bit will be asserted reliably. However, in some cases, two reads are needed for clearing the affected bits.

The following formula can be used to determine the timing window that the LCLK assertion should be avoided.

- If the AU4 pointer is set at 522, the sensitive byte is located on row 4.

```
LCLK assertion window to avoid  = EJ0 + PP_FRM_ALIGN_DLY[15:0] + 3240
(3*90*12) + window size
```

- If the AU4 pointer is set at 0, the sensitive byte is located on row 7.

```
LCLK assertion window to avoid = EJ0 + PP_FRM_ALIGN_DLY[15:0] + 6480
(6*90*12) + window size
```

Note that the numerical values in the above equations represent 77.76 MHz REFCLK clock cycles. For example, assume PP_FRM_ALIGN_DLY[15:0] = 0, and AU4 pointer = 522. Using a plus/minus half of the SONET/SDH row as the window size, ie. window size = +/- (45*12) = +/- 540. Therefore, the timing windows that LCLK should be avoided is from EJ0 +3240-540 to EJ0+3240+540, or from EJ0 + 34.72 ms to EJ0 + 48.61 ms.

Software:

To address this issue in software, the following alternate indications can be used to replace the function of the affected interrupt bits.

For ESEI: Because the TRIB_INT[x][y][z] bits are not affected by this issue, for ESEI indication, the TRIB_INT[x][y][z] can be used. To do this the ESEE bit must be set to '1', and PJE and NJE must be set to '0'.

For PJEI: The PJE[12:0] bit can be used.

For NJEI: The NJE[12:0] bit can be used.

For OVR and PEND: The OVR and PEND bits in RTOP 336 register 300AH can be used to replace this function.

13.25 SVCA_R Pointer Corruption

Pointer corruption may occur when configuring SONET/SDH payload in the SVCA_R block from a concatenated stream to a channelized stream. A software workarounds are available for this issue.

1. Ensure the pointer is recalculated when the payload is configured.

2. After payload configuration.

- Set Diag_NDFREQ bit 5 to ‘1’ in “SVCA Diagnostic/Configuration” indirect register 0x02.
- Clear Diag_NDFREQ bit 5 to ‘0’ in “SVCA Diagnostic/Configuration” indirect register 0x02.

13.26 Performance Monitoring Circuitry Lock Up

The performance monitoring circuitry in the RHPP_R, SVCA_R, SHPI, RSEF, PIPM blocks may lock up when the device is reset during a specific timing window.

After the TUPP 2488 device is powered up, read the LCML_TIP, SCML_TIP and HPOH_TIP bits in register 001DH to ensure they are not set to ‘1’. If one or more of these bits are set to ‘1’, perform a hardware or software reset as follows:

Hardware Reset

1. Wait at least 5 REFCLK (5x 12.86 ns) cycles.
2. Assert the RSTB pin (Pull it low)
3. Wait a minimum of 1 ms (Keep it low)
4. De-assert RSTB (Pull it high).
5. Read LCML_TIP, SCML_TIP and HPOH_TIP to ensure they are not set to ‘1’. If one or more of these bits are set to ‘1’, perform a hardware or software reset again.

Software Reset

1. Wait at least 5 REFCLK (5x 12.86 ns) cycles.
2. Set SRESET to ‘1’ (Master Reset #1: Register 0x0000)
3. Wait 200 ns
4. Set SRESET to ‘0’ (Master Reset #1: Register 0x0000)
5. Wait 100 ns
6. Read LCML_TIP, SCML_TIP and HPOH_TIP to ensure they are not set to ‘1’. If one or more of these bits are set to ‘1’, perform a hardware or software reset again.

14 Functional Timing

This section shows the functional relationship between inputs and outputs. It also shows effects on timing due to various configuration options. No propagation delays are shown.

14.1 Line Side Ingress Parallel TelecomBus

Figure 65 shows the timing of the ingress TelecomBus interface. Timing is provided by REFCLK. SONET/SDH data is carried in the IDATA[*X*][7:0], where '*X*' denotes one of the four sections of the Incoming TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Figure 65 shows a timeslot naming strategy and assignment on an IDATA[*X*][7:0] bus. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IJ0J1[*X*] is set high with IPL[*X*] set low to mark the J0(C1) byte of a transport frame. IJ0J1[*X*] is set high with IPL[*X*] also set high to mark the J1 byte of all the streams within IDATA[*X*][7:0]. The J0 byte position on all four buses must be aligned.

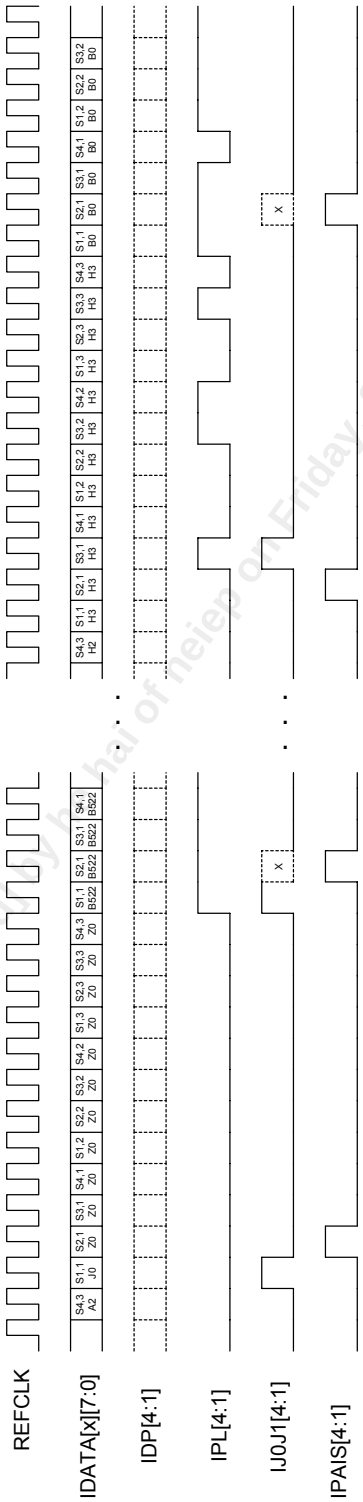
High order (path) streams in AIS alarm are indicated by the IPAIS[*X*] signal. In Figure 65 timeslots numbers S1,x, S2,y, and S4,z are configured as STS-1/STM-0 operation. Timeslot number S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on IPL[*X*] and IJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (IPAIS[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by IJ0J1[*X*] being set high at byte S3,1/H3 and IPL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3.

Stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on IPL[*X*] at byte S4,1/B0. Stream S4,2 is shown to undergo a negative pointer justification event as indicated by the high level on IPL[*X*] at byte S4,2/H3.

For the case where an STS-48c/STM-16c is carried on the four buses IDATA[X][7:0], the J0 indication is expected on all four buses (IJ0J1[X] = 1 and IPL[X] = 0). The J1 indication is expected only on the first bus (IJ0J1[1] = 1 and IPL[1] = 1, IJ0J1[4:2] = 0 and IPL[1] = 1).

The arrangement shown in Figure 65 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 65 Ingress TelecomBus Timing



14.2 Line Egress Parallel TelecomBus

Figure 66 shows the timing of the Line Egress TelecomBus interface. Timing is provided by REFCLK. SONET/SDH data is carried in the EDATA[*X*][7:0], where '*X*' denotes one of the four sections of the Line Egress TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. The STSI block can be used to rearrange timeslots between the system side and the line side of the SPECTRA 2488.

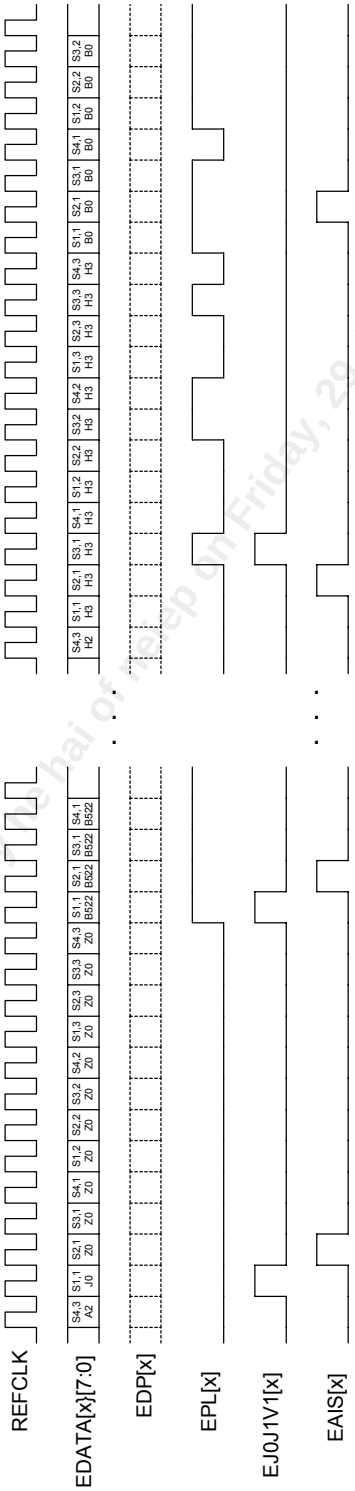
The timeslot naming strategy and assignment is shown in Figure 66. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The EPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. All four EJ0J1[4:1] signals are set high with all four EPL[4:1] signals set low to mark the J0 (C1) byte of a transport frame. EJ0J1[*X*] is set high with EPL[*X*] also set high to mark the J1 byte of all the streams within EDATA[*X*][7:0]. High order streams in alarm are indicated by the EAIS[*X*] signal. This signal is used for low order tributary alarms when PP loopback is enabled.

In Figure 45, timeslots S1,x, S2,y, and S4,z are configured for STS-1/STM-0 operation. Timeslot S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on EPL[*X*] and EJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path alarm (EAIS[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by EJ0J1[*X*] being set high at byte S3,1/H3 and EPL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3. Stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on EPL[*X*] at byte S4,1/B0. Stream S4,2 is shown to undergo a negative pointer justification event as indicated by the high level on EPL[*X*] at byte S4,2/H3.

For the case where an STS-48c/STM-16c is carried on the four buses EDATA[4:1][7:0], the J0 indication is given on all four buses (EJ0J1[X] = 1 and EPL[X] = 0) at the same time. The J1 indication is given only on the first bus (EJ0J1[1] = 1 and EPL[1] = 1, EJ0J1[4:2] = 0 and EPL[1] = 1).

The arrangement shown in Figure 66 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

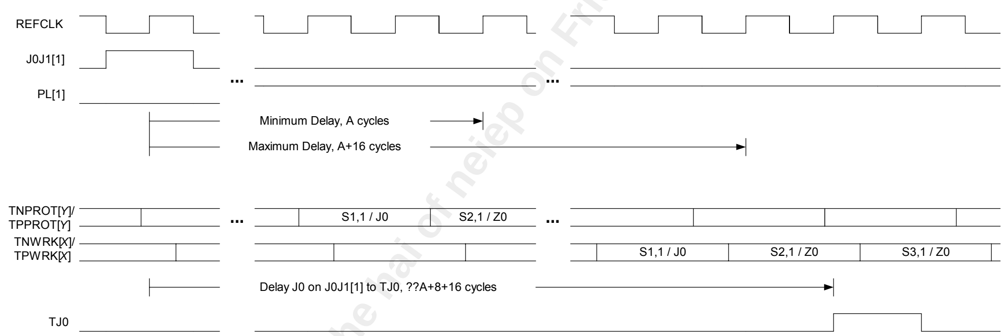
Figure 66 Egress TelecomBus Timing



14.3 Transmit Serial Buses

Figure 67 shows the delay from the Incoming parallel TelecomBus stream to the transmit serial TelecomBus links. For example, this applies to be the outgoing Line Egress serial bus. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 16 REFCLK cycles. The minimum delay (A REFCLK cycles) is shown to be incurred by one of the transmit protection serial data links (TPPROT[*X*]/TNPROT[*X*]) and is the delay through the TCB encode + TSEC slice (+TILC on system side + MUX FIFO on STS-48 slices). See section 10.10 for details. The maximum delay (A+16 cycles) is shown to be incurred by one of the transmit working serial data links (TPWRK[*X*]/TNWRK[*X*]). TheTJ0 identifies the time at which all the transmit serial links have transmitted their respective J0 characters (and in the case of Line Egress is relative to IJ0). The relative phases of the links in Figure 67 are shown for illustrative purposes only.

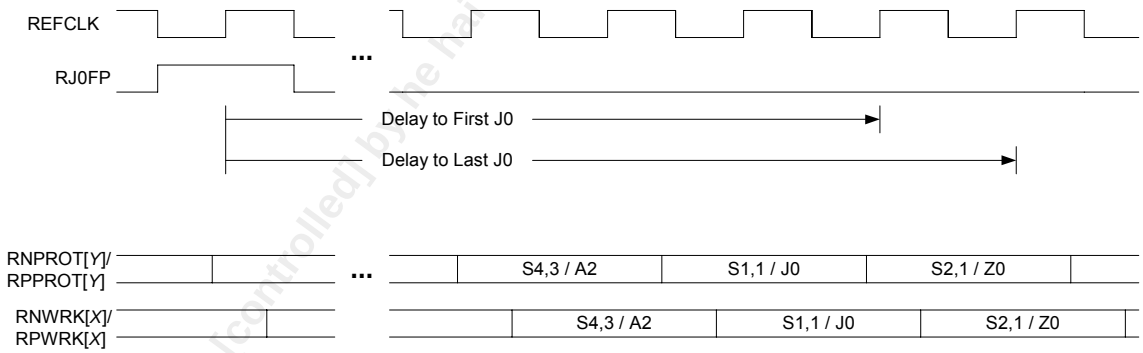
Figure 67 Incoming Parallel TelecomBus to Transmit Serial Telecom Bus Timing



14.4 Receive Serial Buses

Figure 68 shows the relative timing of the receive serial TelecomBus links. Links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (J0FP). RJ0FP in the case of the Line side of TUPP 2488 bus is IJ0. In the case of the System Egress, RJ0FP is SYSTEM_EGRESS_REF_DLY after EJ0. Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other (within a tolerance level of 16+8=24 byte times) but are frequency locked. The delay from RJ0FP being sampled high to the first and last J0 character is shown in Figure 68. In this example, the first J0 is delivered by one of the four protection links (RNPROT[4:1]/RPPROT[4:1]). The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, one of the auxiliary links is shown to be the slowest (RNWRK[4:1]/RPWRK[4:1]). The minimum value for the internal programmable delay is the delay to the last J0 character plus 15. The maximum value is the delay to the first J0 character plus 31. Consequently, the external system must ensure that the relative delays between all the receive RASIO™ CML links be less than 16 bytes. The relative phases of the links in Figure 68 are shown for illustrative purposes only.

Figure 68 Receive Serial TelecomBus Link Timing

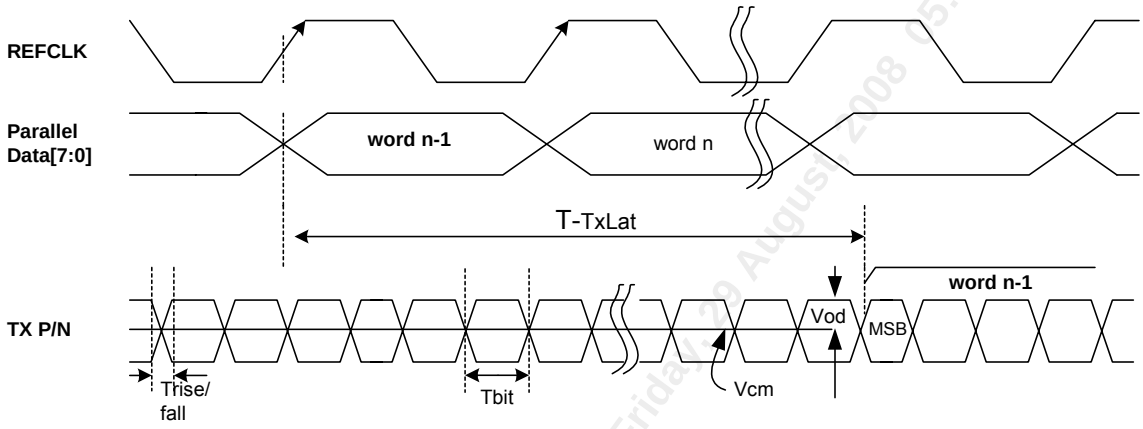


14.5 RASIO™ CML Functional Timing

Every one of the 77.76 MByte/s STS12 transmit channels received carries a byte-stream. These are named “Parallel Data[7:0]” in Figure 69 and Figure 70and are synchronous to REFCLK. After CML Subsystem processing eight serial bit-streams are transmitted to the differential RASIO™ CML pads on the line side, or sixteen serial bit-streams are transmitted to the differential RASIO™ CML pads on the System side.

In Figure 69, the transmit serial lines are generalized as “TX P/N.”

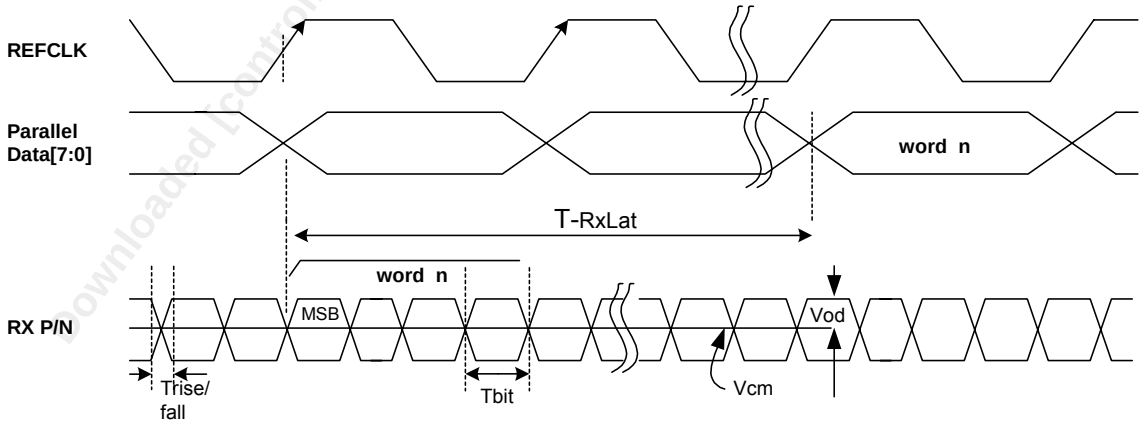
Figure 69 RASIO™ CML Transmit



After CML Subsystem processing eight 77.76 MByte/s STS12 channel byte streams are transmitted on the parallel data bus synchronous to REFCLK on the line side (or 16 on the system side)

Every one of the eight/sixteen 77.76 MByte/s STS12 receive channels carries a serial bit-stream received from the differential RASIO™ CML pads. In Figure 70, the receive serial lines are generalized as “RX P/N.”

Figure 70 RASIO™ CML Receive



14.6 Tributary Path Overhead and Serial Alarm Timing

This section describes Tributary Serial Path Overhead and Alarm Output Timing per STS-12/STM-4 slice.

The Tributary Path Overhead and Alarm (TPOH) port outputs the entire path overhead and alarm indications for all tributaries for external processing (to a maximum of 336 per STS-12/SDH-4 data stream). The TPOH port includes device pin TPOH[4:1], TPOHEN[4:1], TPOHFP[4:1] and TRAD[4:1].

All signals on the TPOH port are referenced to the 77.76 MHz reference clock (REFCLK), and they are updated on the rising edge of REFCLK.

The TPOHFP signal provides synchronization between the TPOH port and the transport frame. It asserts high for 1 REFCLK clock cycle for every 250 µs interval, and it identifies the most significant bit of the V5 or J1 byte for the first tributary on TPOH. Two TPOHFP frame pulses are asserted in a 500 µs multiframe to denote the overhead transmission of 2 entire tributaries (up to 336 timeslots).

During the extraction, the tributary path overhead bytes (V5, J2, Z6/N2, and Z7/K4 or J1, B3, C2, G1, F2, H4, F3, K3 and N1 for the TU3 tributary) are extracted serially from the most significant to the least significant bit through the TPOH signal. Since the tributary path overhead bytes are output 2 times per 500 µs multiframe, in order to distinguish the first presentation of an overhead byte from subsequent repeated presentations, TPOHEN is used. If TPOHEN is asserted high, the path overhead byte on TPOH is new, and if TPOHEN is asserted low, the path overhead byte is repeated.

Timeslot assignment on TPOH is unrelated to the tributary group configuration. The timeslots for 4 tributaries are always reserved for any TUG2 even if it is configured for TU12, TU2 or VT3. Hence, 336 timeslots are always available on the TPOH. At timeslots devoted to non-existent tributaries; for example, tributary 2, 3 and 4 of a TUG2 configured for TU2, TPOH and TPOHEN will set low.

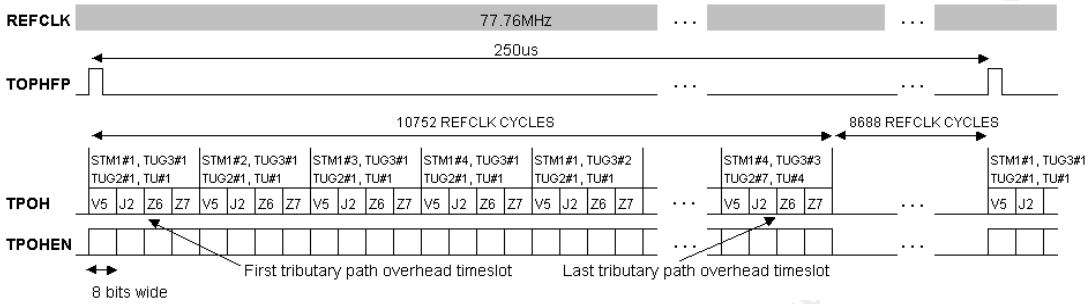
The tributary path overhead output sequence on TPOH is arranged in the same order as on the incoming STS-12/STM-4 data stream. Each STS-12/STM-4 data stream can contain up to 336 tributaries. Table 47 summarizes the completed sequence. The first path overhead output on TPOH is from tributary STM-1#1, TUG3#1,TUG2#1, TU#1. The second path overhead output is from tributary STM-1#2, TUG3#1,TUG2#1, TU#1. The last path overhead output is from tributary STM-1#4, TUG3#3, TUG2#7, TU#4. The completed sequence is repeatedly output on TPOH every 250 µs.

Table 47 Tributary Output Sequence in TPOH

TU Number	TUG2 Number	TUG3 Number	STM-1 Number
1	1	1	1
:	:	:	:
1	1	1	4
1	1	2	1
:	:	:	:
1	1	2	4
1	1	3	1
:	:	:	:
1	1	3	4
1	2	1	1
:	:	:	:
1	2	3	4
1	3	1	1
:	:	:	:
1	7	3	4
2	1	1	1
:	:	:	:
2	7	3	4
3	1	1	1
:	:	:	:
4	7	3	4

Figure 71 shows the functional timing of the TPOH signal with non-TU3 tributary. A total of 336 sets of path overhead (V5, J2, Z6 and Z7) timeslots are reserved between every two 250 µs TPOHFP assertions. As shown in Figure 71, the 336 timeslots only occupy the first 10,752 REFCLK cycles in each 250 µs interval. The remaining 8,688 REFCLK cycles are set to 0.

Figure 71 Tributary Path Overhead (TPOH) with non-TU3 Tributary



In the event where the STS-12/STM-4 frame contains TU3 tributaries, the TPOH pin will output the 9 path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) on its dedicated timeslots. A summary of the mapping of TU3 overhead byte timeslots to lower order overhead byte timeslots is shown in Table 48. A complete enumeration of the ordering of path overhead bytes presented on the TPOH pin is shown in Table 49.

Table 48 TPOH Bytes Mapping in TU3 Mode

TU3 POH	Lower Order Tributary Overhead Timeslots			
	Extraction Opportunity Time Slot #1	Extraction Opportunity Time Slot #2	Extraction Opportunity Time Slot #3	Extraction Opportunity Time Slot #4
TU3, J1	TUG2#1, TU#1, V5	TUG2#1, TU#2, V5	TUG2#1, TU#3, V5	TUG2#1, TU#4, V5
TU3, B3	TUG2#1, TU#1, J2	TUG2#1, TU#2, J2	TUG2#1, TU#3, J2	TUG2#1, TU#4, J2
TU3, C2	TUG2#1, TU#1, Z6	TUG2#1, TU#2, Z6	TUG2#1, TU#3, Z6	TUG2#1, TU#4, Z6
TU3, G1	TUG2#1, TU#1, Z7	TUG2#1, TU#2, Z7	TUG2#1, TU#3, Z7	TUG2#1, TU#4, Z7
TU3, F2	TUG2#2, TU#1, V5	TUG2#2, TU#2, V5	TUG2#2, TU#3, V5	TUG2#2, TU#4, V5
TU3, H4	TUG2#2, TU#1, J2	TUG2#2, TU#2, J2	TUG2#2, TU#3, J2	TUG2#2, TU#4, J2
TU3, Z3	TUG2#2, TU#1, Z6	TUG2#2, TU#2, Z6	TUG2#2, TU#3, Z6	TUG2#2, TU#4, Z6
TU3, Z4	TUG2#2, TU#1, Z7	TUG2#2, TU#2, Z7	TUG2#2, TU#3, Z7	TUG2#2, TU#4, Z7
TU3, Z5	TUG2#3, TU#1, V5	TUG2#3, TU#2, V5	TUG2#3, TU#3, V5	TUG2#3, TU#4, V5

Table 49 Path Overhead Byte Ordering on the TPOH Port

byte_num	stm1	tug3	tug2	tu	trib_num	trib_poh	tu3	tu3_poh
1	1	1	1	1	1	V5	1	J1
2	1	1	1	1	1	J2	1	B3
3	1	1	1	1	1	Z6	1	C2
4	1	1	1	1	1	Z7	1	G1
5	2	1	1	1	2	V5	2	J1
6	2	1	1	1	2	J2	2	B3
7	2	1	1	1	2	Z6	2	C2
8	2	1	1	1	2	Z7	2	G1
13	4	1	1	1	4	V5	4	J1
14	4	1	1	1	4	J2	4	B3
15	4	1	1	1	4	Z6	4	C2
16	4	1	1	1	4	Z7	4	G1
17	1	2	1	1	5	V5	5	J1
18	1	2	1	1	5	J2	5	B3
19	1	2	1	1	5	Z6	5	C2
20	1	2	1	1	5	Z7	5	G1
29	4	2	1	1	8	V5	8	J1
30	4	2	1	1	8	J2	8	B3
31	4	2	1	1	8	Z6	8	C2
32	4	2	1	1	8	Z7	8	G1
33	1	3	1	1	9	V5	9	J1
34	1	3	1	1	9	J2	9	B3
35	1	3	1	1	9	Z6	9	C2
36	1	3	1	1	9	Z7	9	G1
45	4	3	1	1	12	V5	12	J1
46	4	3	1	1	12	J2	12	B3
47	4	3	1	1	12	Z6	12	C2
48	4	3	1	1	12	Z7	12	G1
49	1	1	2	1	13	V5	1	F2
50	1	1	2	1	13	J2	1	H4
51	1	1	2	1	13	Z6	1	Z3
52	1	1	2	1	13	Z7	1	Z4
...								
93	4	3	2	1	24	V5	12	F2
94	4	3	2	1	24	J2	12	H4
95	4	3	2	1	24	Z6	12	Z3
96	4	3	2	1	24	Z7	12	Z4
97	1	1	3	1	25	V5	1	Z5
98	1	1	3	1	25	J2	1	0
99	1	1	3	1	25	Z6	1	0
100	1	1	3	1	25	Z7	1	0

byte_num	stm1	tug3	tug2	tu	trib_num	trib_poh	tu3	tu3_poh
101	2	1	3	1	26	V5	2	Z5
102	2	1	3	1	26	J2	2	0
103	2	1	3	1	26	Z6	2	0
104	2	1	3	1	26	Z7	2	0
...								
141	4	3	3	1	36	V5	12	Z5
142	4	3	3	1	36	J2	12	0
143	4	3	3	1	36	Z6	12	0
144	4	3	3	1	36	Z7	12	0
145	1	1	4	1	37	V5	1	0
146	1	1	4	1	37	J2	1	0
147	1	1	4	1	37	Z6	1	0
148	1	1	4	1	37	Z7	1	0
...								
333	4	3	7	1	84	V5	12	0
334	4	3	7	1	84	J2	12	0
335	4	3	7	1	84	Z6	12	0
336	4	3	7	1	84	Z7	12	0
337	1	1	1	2	85	V5	1	J1
338	1	1	1	2	85	J2	1	B3
339	1	1	1	2	85	Z6	1	C2
340	1	1	1	2	85	Z7	1	G1
341	2	1	1	2	86	V5	2	J1
342	2	1	1	2	86	J2	2	B3
343	2	1	1	2	86	Z6	2	C2
344	2	1	1	2	86	Z7	2	G1
345	3	1	1	2	87	V5	3	J1
346	3	1	1	2	87	J2	3	B3
347	3	1	1	2	87	Z6	3	C2
348	3	1	1	2	87	Z7	3	G1
349	4	1	1	2	88	V5	4	J1
350	4	1	1	2	88	J2	4	B3
351	4	1	1	2	88	Z6	4	C2
352	4	1	1	2	88	Z7	4	G1
353	1	2	1	2	89	V5	5	J1
354	1	2	1	2	89	J2	5	B3
355	1	2	1	2	89	Z6	5	C2
356	1	2	1	2	89	Z7	5	G1
...								
381	4	3	1	2	96	V5	12	J1
382	4	3	1	2	96	J2	12	B3
383	4	3	1	2	96	Z6	12	C2
384	4	3	1	2	96	Z7	12	G1

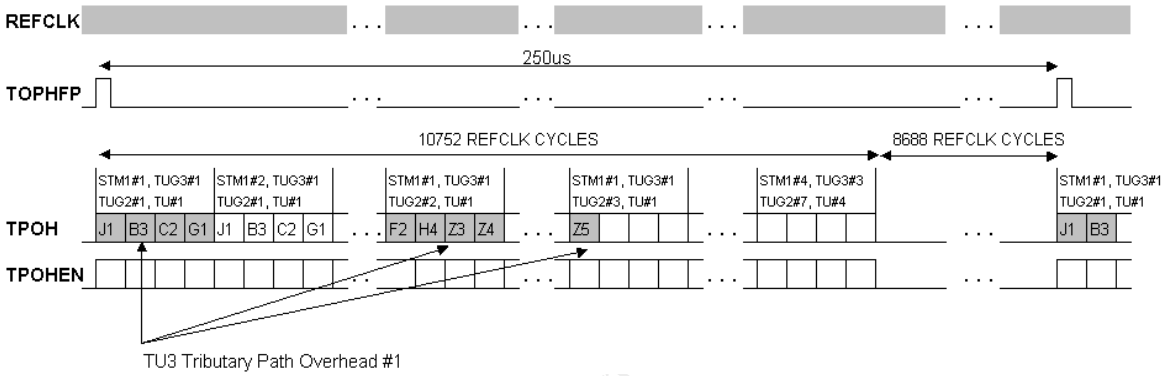
byte_num	stm1	tug3	tug2	tu	trib_num	trib_poh	tu3	tu3_poh
385	1	1	2	2	97	V5	1	F2
386	1	1	2	2	97	J2	1	H4
387	1	1	2	2	97	Z6	1	Z3
388	1	1	2	2	97	Z7	1	Z4
...								
429	4	3	2	2	108	V5	12	F2
430	4	3	2	2	108	J2	12	H4
431	4	3	2	2	108	Z6	12	Z3
432	4	3	2	2	108	Z7	12	Z4
433	1	1	3	2	109	V5	1	Z5
434	1	1	3	2	109	J2	1	0
435	1	1	3	2	109	Z6	1	0
436	1	1	3	2	109	Z7	1	0
437	2	1	3	2	110	V5	2	Z5
438	2	1	3	2	110	J2	2	0
439	2	1	3	2	110	Z6	2	0
440	2	1	3	2	110	Z7	2	0
...								
670	4	3	7	2	168	J2	12	0
671	4	3	7	2	168	Z6	12	0
672	4	3	7	2	168	Z7	12	0
673	1	1	1	3	169	V5	1	J1
674	1	1	1	3	169	J2	1	B3
675	1	1	1	3	169	Z6	1	C2
676	1	1	1	3	169	Z7	1	G1
677	2	1	1	3	170	V5	2	J1
678	2	1	1	3	170	J2	2	B3
679	2	1	1	3	170	Z6	2	C2
680	2	1	1	3	170	Z7	2	G1
765	4	3	2	3	192	V5	12	F2
766	4	3	2	3	192	J2	12	H4
767	4	3	2	3	192	Z6	12	Z3
768	4	3	2	3	192	Z7	12	Z4
769	1	1	3	3	193	V5	1	Z5
770	1	1	3	3	193	J2	1	0
771	1	1	3	3	193	Z6	1	0
772	1	1	3	3	193	Z7	1	0
773	2	1	3	3	194	V5	2	Z5
774	2	1	3	3	194	J2	2	0
775	2	1	3	3	194	Z6	2	0
776	2	1	3	3	194	Z7	2	0
813	4	3	3	3	204	V5	12	Z5
814	4	3	3	3	204	J2	12	0

byte_num	stm1	tug3	tug2	tu	trib_num	trib_poh	tu3	tu3_poh
815	4	3	3	3	204	Z6	12	0
816	4	3	3	3	204	Z7	12	0
817	1	1	4	3	205	V5	1	0
818	1	1	4	3	205	J2	1	0
819	1	1	4	3	205	Z6	1	0
820	1	1	4	3	205	Z7	1	0
821	2	1	4	3	206	V5	2	0
822	2	1	4	3	206	J2	2	0
823	2	1	4	3	206	Z6	2	0
824	2	1	4	3	206	Z7	2	0
825	3	1	4	3	207	V5	3	0
826	3	1	4	3	207	J2	3	0
827	3	1	4	3	207	Z6	3	0
828	3	1	4	3	207	Z7	3	0
829	4	1	4	3	208	V5	4	0
830	4	1	4	3	208	J2	4	0
831	4	1	4	3	208	Z6	4	0
832	4	1	4	3	208	Z7	4	0
833	1	2	4	3	209	V5	5	0
834	1	2	4	3	209	J2	5	0
835	1	2	4	3	209	Z6	5	0
836	1	2	4	3	209	Z7	5	0
...								
1004	3	3	7	3	251	Z7	11	0
1005	4	3	7	3	252	V5	12	0
1006	4	3	7	3	252	J2	12	0
1007	4	3	7	3	252	Z6	12	0
1008	4	3	7	3	252	Z7	12	0
1009	1	1	1	4	253	V5	1	J1
1010	1	1	1	4	253	J2	1	B3
1011	1	1	1	4	253	Z6	1	C2
1012	1	1	1	4	253	Z7	1	G1
...								
1340	3	3	7	4	335	Z7	11	0
1341	4	3	7	4	336	V5	12	0
1342	4	3	7	4	336	J2	12	0
1343	4	3	7	4	336	Z6	12	0
1344	4	3	7	4	336	Z7	12	0

TU3 path overhead bytes are shifted out 2 times per multi-frame (each shift out is 250 µs), and in each shifting cycle, 2 new TU3 overheads are shifted out as indicated by the TPOHEN signal from the 4 opportunity timeslots. In total, 4 new TU3 path overheads are shifted out in each multiframe.

Figure 72 shows the functional timing for TPOH in TU3 mode. The gray area in the TPOH stream is 1 of 4 of the reserved timeslots for the first TU3 Tributary Path Overhead bytes. Note that each set of TU3 path overhead only occupies 3 low-order tributary path overhead timeslots, the rest of the 25 timeslots are all set to 0.

Figure 72 Tributary Path Overhead (TPOH) in TU3 Mode



When the TRAD_BIPE_SEL bit (Reg. 004BH, etc) is set to '0', the Tributary Alarm Signals (TRAD) outputs the BIP-2 or BIP-8 (TU3 mode) error counts, RDI, RFI, PDI-P and LOM indications for all the tributaries. TRAD outputs the alarm signals in the sequence of B1, B2, R, AR, P, L, F and an empty bit (set to low). These bits are described in Table 50.

Table 50 TRAD Bit Descriptions

TRAD Bits	Descriptions
B1, B2	If the number of BIP-2 errors (BIP-8 in TU3) is 1, B1=H and B2=L. If the number of BIP-2 errors (BIP-8 in TU3) is 2, B1=H and B2=H.
R, AR	In normal RDI mode, R reports RDI and AR reports RFI status. In enhanced RDI mode, R reports RDI and AR reports ERDI . AR is not valid for TU3 traffic.
P	Reports PDI-P due to tributary path defect indication PDI-V, AIS, LOP and UNEQ states.
L	Reports LOM state. L is not valid for TU3 traffic.
F	Indicates RFI status in Enhanced RDI mode and ignores in normal RDI mode. F is not valid for TU3 traffic.

When the TRAD_BIPE_SEL bit is set to '1', the TRAD port only outputs the BIP-2 or BIP-8 (TU3 mode) error counts.

TRAD is arranged in the same order as the outgoing tributaries. This order is identical to the TPOH output sequence as shown in Table 47. Timeslot assignment on TRAD is unrelated to the configuration of the tributary group. The timeslots for 4 tributaries are always reserved for any tributary group even if it is configured for TU12, VT3 or TU2. For timeslots devoted to non-existent tributaries, for example, tributaries 2, 3 and 4 of a TUG2 configured for TU2, TRAD will be set low. Note that the TRAD timeslots and TPOH timeslots are not aligned.

Similarly, TOHFP identifies the beginning of a frame and it is asserted during the B1 bit of the first tributary on TRAD. The alarm signals for all tributaries are output twice per multi-frame. However, the TRAD is updated only once per multi-frame. The tributary alarm signals are repeated once. The timing diagram of the TRAD signals with non-TU3 tributary and when TRAD_BIPE_SEL = '0' is shown in Figure 73. The timing diagram of the TRAD signals with TU3 tributary and when TRAD_BIPE_SEL = '0' is shown in Figure 74.

Figure 73 Alarm Signal (TRAD) with non-TU3 Tributary (TRAD_BIPE_SEL = '0')

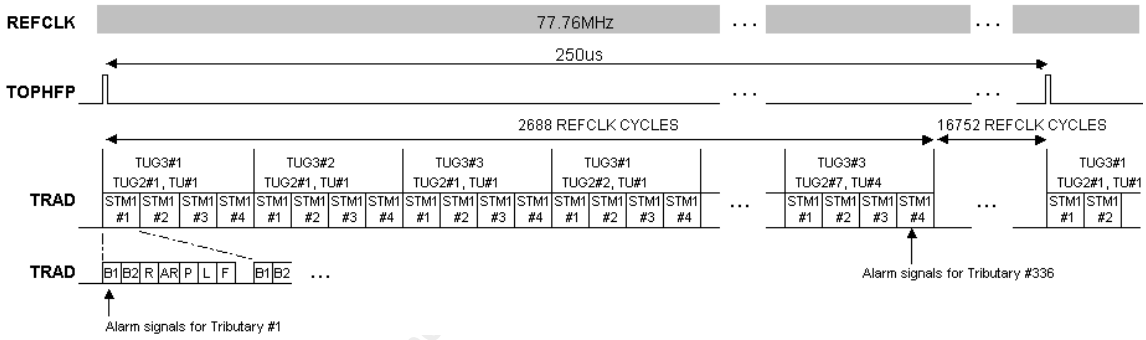
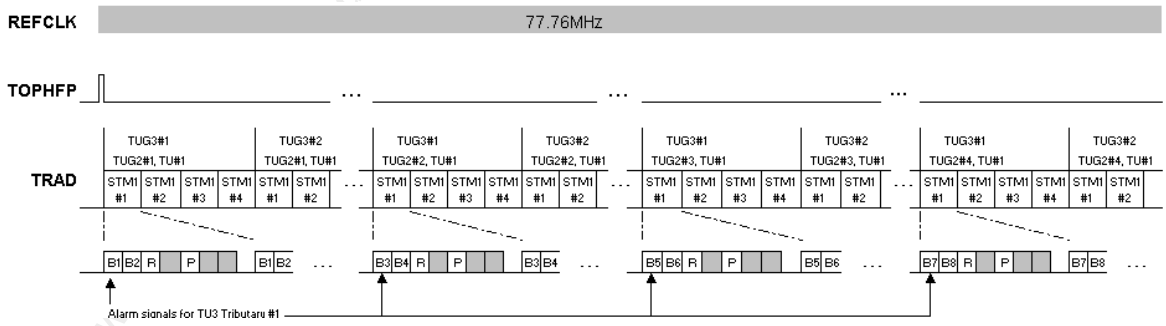


Figure 74 Alarm Signal (TRAD) with TU3 Tributary (TRAD_BIPE_SEL = '0')



The timing diagram of the TRAD signals with no TU3 tributary and when TRAD_BIPE_SEL = '1' is shown in Figure 75. The timing diagram of the TRAD signals with TU3 tributary and when TRAD_BIPE_SEL = '1' is shown in Figure 76.

Figure 75 Alarm Signal (TRAD) with non-TU3 Tributary (TRAD_BIPE_SEL = '1')

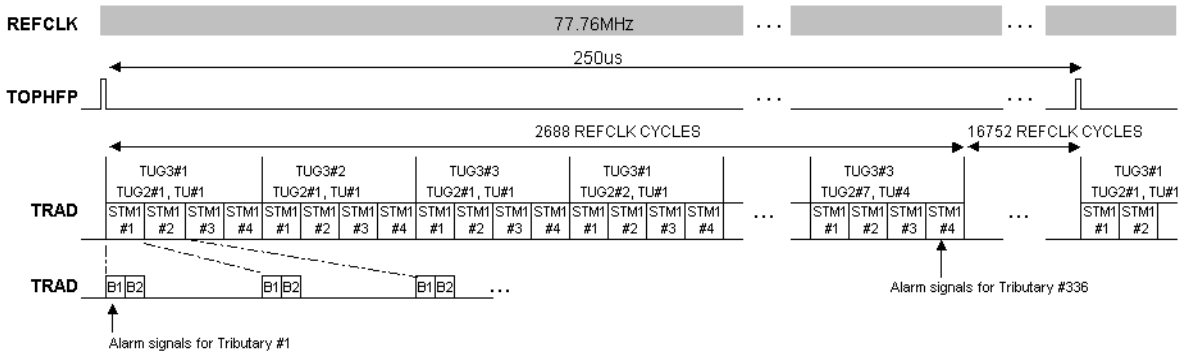
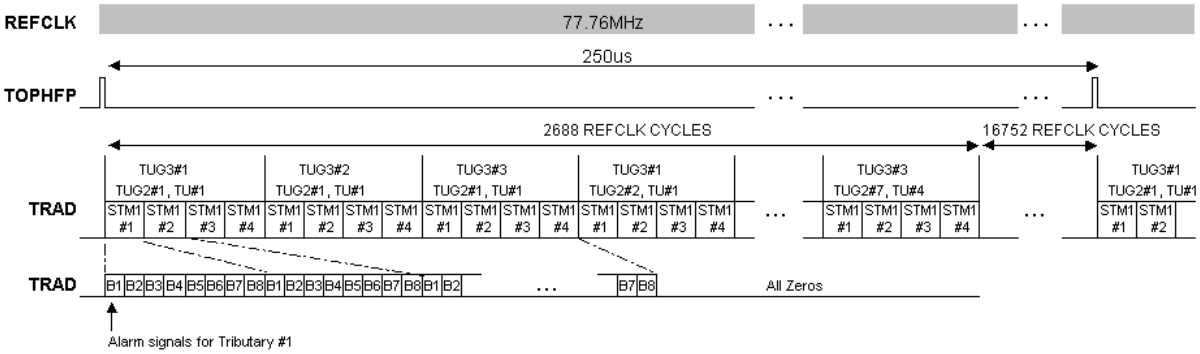


Figure 76 Alarm Signal (TRAD) with TU3 Tributary (TRAD_BIPE_SEL = '1')



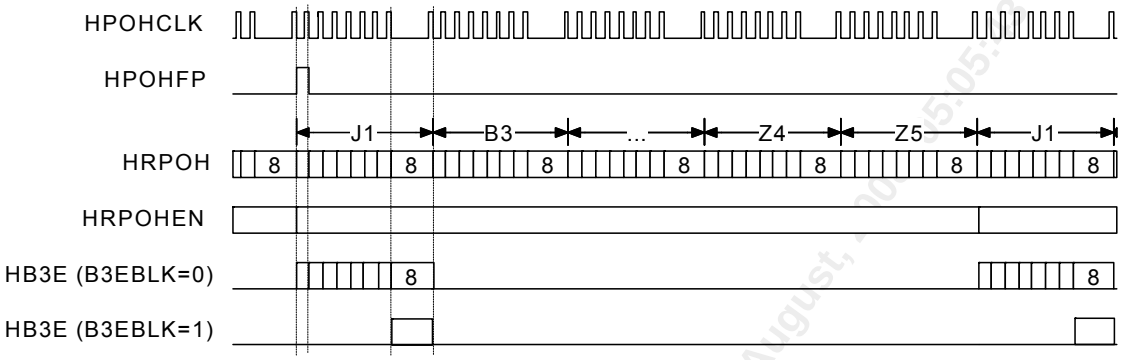
14.7 High Order Receive Path Overhead Port (High Order)

The High Order Receive Path Overhead (HRPOH) port (HRPOH, HRPOHEN and HB3E) is used to output the path overhead bytes and path BIP-8 error indications (HB3E) extracted from the ingress data stream. The POH bytes are output on HRPOH MSB first in the same order that they are received. Figure 77 shows HRPOH output timing. Since HPOHFP is synchronized on the transport frame, zero, one or two path overhead can be output per path per frame. HRPOHEN is used to indicate new POH bytes on HRPOH. HRPOHEN is either asserted or de asserted for the nine POH bytes. The path BIP-8 errors are output on HB3E at the same time the path trace byte is output on HRPOH.

Note:

- HRPOHEN will be asserted to validate zero, one or two opportunities per path per frame out of three possible opportunities to output a path overhead byte. HRPOHEN opportunities will alternate from path to path and from frame to frame based on pointer movement. Use HRPOHEN to determine which timeslot and which bits are valid.

Figure 77 HRPOH Output Timing



All signals on the HRPOH port are reference to a nominal 20.736 MHz 33% high duty cycle clock (HPOHCLK). HPOHCLK is generated by gapping an internal 25.92 MHz clock. This means that every 2 out of 10 clock edges are skipped to trigger exactly 2,592 clock pulses between each 125 µs interval. Note that all signals on the HRPOH port are updated on the falling edges of HPOHCLK.

- The HPOHFP signal provides synchronization between the HRPOH port and the transport frame. It asserts high for 1 HPOHCLK clock cycle for every 125 µs. HPOHFP can be used to identify the most significant bit of the J1 byte for the first path on HRPOH, and the first possible path BIP error on HB3E. In other words, it indicates the first clock pulse of the 2,592 clock pulses of each frame.
- During the extraction, the 9 path overhead bytes for each path (a total of 12) are output on the HRPOH pin, most significant bit first, in the same order that they are received. HRPOH is synchronized on the transport frame, and 3 timeslots on HRPOH are assigned per path per frame. 0, 1, or 2 sets of path overhead bytes can be output per path per frame. The same path overhead bytes are output repetitively until a new one is available.
- The HRPOHEN signal is used to indicate if the path overhead bytes on the HRPOH pin are new or if they are repeated. When HRPOHEN is high, the 9 path overhead bytes on HRPOH are new and they are ready for extraction. When HRPOHEN is low, the path overhead bytes on HRPOH are either not ready for extraction or they are repeated from the previous timeslots. Since the 9 path overhead bytes for each path are always output on HRPOH together, HRPOHEN is either asserted or de-asserted for the entire 9 path overhead bytes.

The BIP-8 errors for each path are output on the HB3E pin at the same time the J1 byte is output on HRPOH. The BIP-8 error indication is configurable in either block basis or bit basis. In block basis (B3EBLK = 1), there can only be 1 error per path per frame. In bit basis (B3EBLK = 0), there can be a maximum of 8 errors per path per frame.

The following section describes the mapping for the path overhead bytes on the HRPOH port when the STS-12/STM4 frame carries:

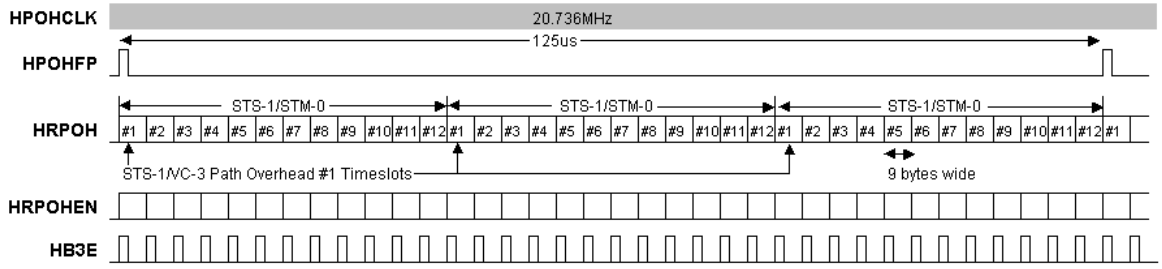
- 12x VC-3s,
- 4x STS-3c or 4x VC-4/C-4s,
- 4x STS-3c or 4x VC-4/TUG-3s, and
- 1x STS-12c or 1x VC-4-4c.
- Please note that when the ingress traffic is an STS-48c/VC-4-16c data stream, only the first of the 4 ports is used.

In the subsequent figures, each timeslot on the HRPOH signal represents 9 path overhead bytes.

STS-1/VC-3

Figure 78 shows an STS-12/STM-4 data stream carrying 12 VC-3 payloads. The timeslots are repeatedly assigned from STS-1/STM-0 #1 to #12 for 3 cycles in 1 frame. 0, 1 or 2 sets of path overhead can be output in one 125 µs interval. As described above, HRPOHEN is used to indicate when a new set of path overhead bytes is ready for sampling.

Figure 78 HRPOH Timeslots for STS-1/VC3 mapped with C3

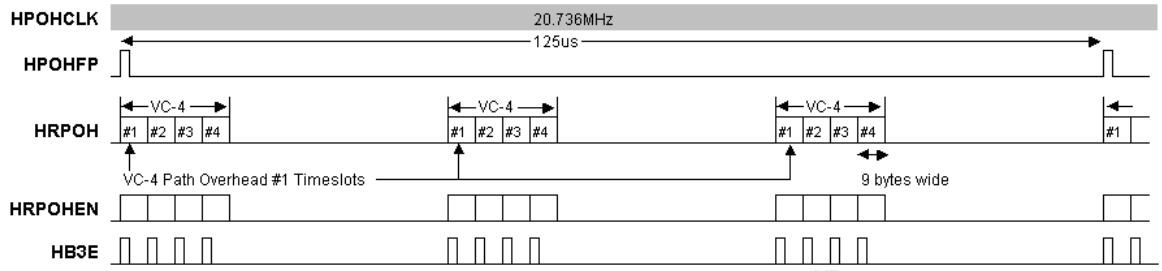


STS-3c/VC4

Just for description purpose, in this document the timeslots reserved for STS-1#1 to STS-1#4 are denoted as master and the timeslots reserved for STS-1#5 to STS-1#12 are denoted as slave.

Figure 79 shows an STS-12/STM-4 data stream carrying four STS-3c/VC-4/C-4 payloads. In this figure, only the master timeslots contain valid path overhead bytes. The slave timeslots contain all zeros. The four VC-4 path overhead timeslots can be outputted on any of the 3 master timeslots. The valid path overhead bytes are indicated by the HRPOHEN signal.

Figure 79 HRPOH Timeslots for STS-3c/VC4 Mapped with C4

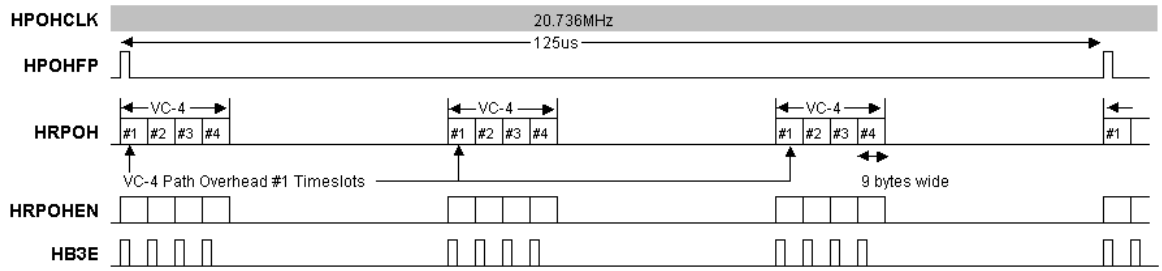


VC4 with TUG-3

Figure 80 shows an STS-12/STM-4 data stream carrying four VC-4 payloads, and each VC-4 carries three TUG-3 payloads. Only the master timeslots contain valid path overhead bytes, and the slave timeslot contain all zeros. The 4 sets of VC-4 path overhead can be output on any of the 3 master timeslots. The valid VC-4 path overhead bytes are indicated by the HRPOHEN signal. Note that the signal mapping is exactly the same as Figure 79.

The low-order path overhead bytes from tributaries mapped inside the TUG3s (TU11, TU12, TU2, and TU3) can be extracted via the Tributary Path Overhead Port (TPOH). Please see section 14.6.

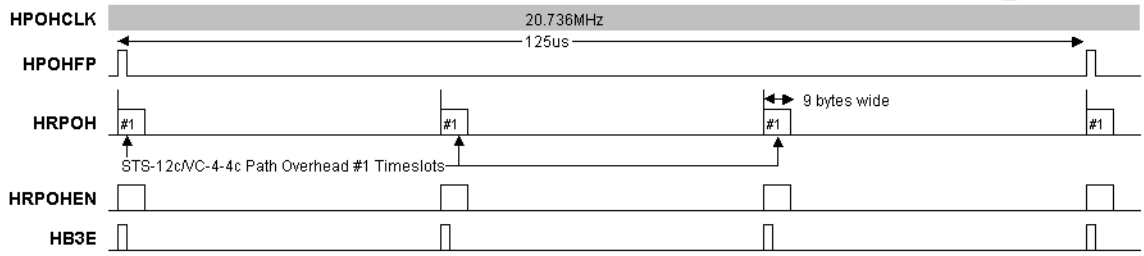
Figure 80 HRPOH Timeslot for VC-4 mapped with TUG3



STS-12c/VC4-4c

Figure 81 shows an STS-12/STM-4 data stream carrying an STS-12c/VC-4-4c payload. The VC-4-4c path overhead can be output on 1 of 3 master timeslots. The valid path overhead is indicated by HRPOHEN.

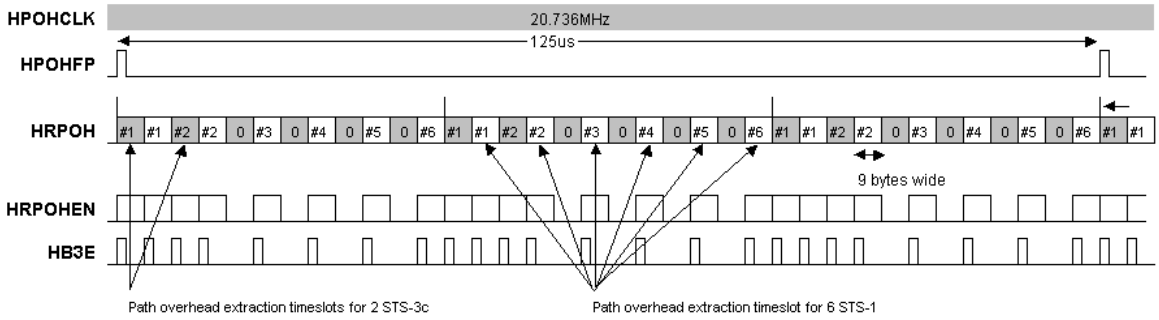
Figure 81 HRPOH Timeslot for STS-12c/VC4-4c



Legal Mix

The HRPOH port can also extract high-order path overheads from any legal mixture of payloads. Figure 82 shows an example of an STS-12/STM-4 data stream carrying 2 STS-3c/VC4 and 6 STS-1/STM-0.

Figure 82 HRPOH Timeslot for Mixture of 2 STS-3c/VC4 and 6 STS-1/STM-0



14.8 High Order Transmit Path Overhead

The High Order Transmit Path Overhead (HTPOH) port (ETPL_HTPOH, EIDLE_HTPOHEN and EV5_HTPOHRDY) is used to insert path overhead bytes to the egress data stream. The POH bytes are input on HTPOH MSB first in the same order that they are transmitted. To simplify description, ETPL_HTPOH, EIDLE_HTPOHEN and EV5_HTPOHRDY are denoted as HTPOH, HTPOHEN and HTPOHRDY respectively in this section when not in PP loopback mode.

HTPOH port signals are referenced to the HPOHCLK on the received side. POH bytes on HTPOH shall align with the receive side HPOHFP signal. The HPOHFP and HTPOHRDY signals are updated on the falling edges of HPOHCLK, and HTPOH and HTPOHEN are sampled on the rising edges of HPOHCLK.

- The HPOHFP signal provides synchronization between the HTPOH port and the transport frame. It asserts high for 1 HPOHCLK clock cycle for every 125 µs. HPOHFP can be used to identify the most significant bit of the first J1 byte for the first path on HTPOH.
- During the path overhead insertion, the 9 path overhead bytes for each path are input on the HTPOH pin, most significant bit first, in the same order that they are transmitted. 3 time slots on HTPOH are assigned per path (total of 12 paths) per frame (125 µs). A maximum of 2 series of 864 bits (12x9 bytes) can be inserted on HTPOH between two HPOHFP assertions. Hence, 0, 1, or 2 sets of path overhead per path per frame can be inserted to the outgoing data streams.
- The HTPOHRDY and HTPOHEN signals are used for handshaking between the external device and the HTPOH port. When HTPOHRDY is asserted, the HTPOH port is ready to receive path overhead bytes. If HTPOHRDY is asserted and HTPOHEN is sampled high on the most significant bit of the byte, the byte will be inserted in the path overhead of the outgoing data stream. If HTPOHRDY is asserted and HTPOHEN is sample low on the most significant bit of the byte, the byte will not be inserted in the path overhead of the outgoing data stream, and it will need to be reinserted at the next available opportunity.

The following section illustrates the path overhead bytes mapping on HTPOH when the STS-12/STM4 frame carries:

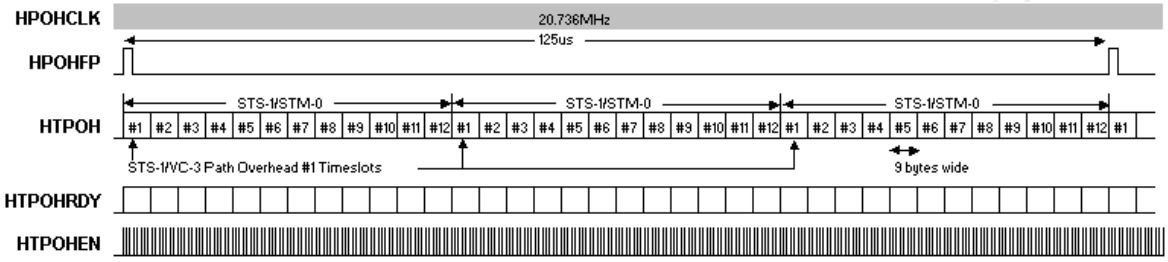
- 12x STS-1s or 12x VC3s,
- 4x STS-3c or 4x VC-4/C-4s,
- 4x STS-3c or 4x VC-4/TUG-3s, and
- 1x STS-12c or 1x VC-4-4c.
- Please note that when the egress traffic is an STS-48c/VC-4-16c data stream, only the first of the 4 ports is used.

In the subsequent figures, each timeslot on the HTPOH signal represents 9 path overhead bytes.

STS-1/VC3

Figure 83 shows an STS-12/STM-4 data stream carrying 12 VC-3 payloads. The HTPOH insertion opportunities are repeatedly assigned from STS-1/STM-0 #1 to #12 for 3 cycles in one 125 µs interval. As described in the previous section, a byte is inserted to the path overhead of an outgoing data stream when HTPOHRDY is asserted and HTPOHEN is sampled high during the most significant bit of the byte.

Figure 83 HTPOH Timeslots for STS-1/VC3 mapped with C3

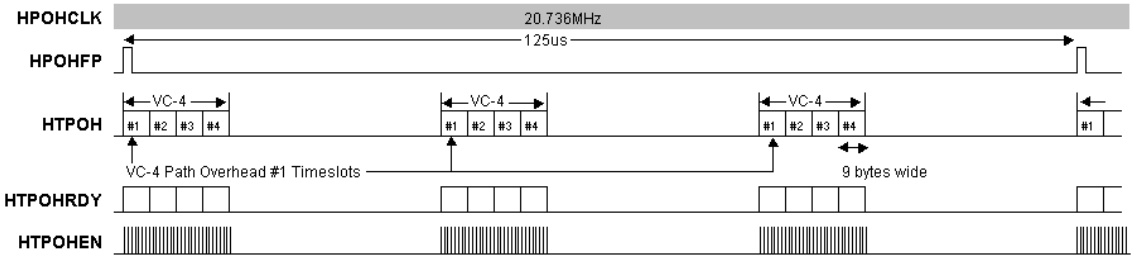


STS-3c/VC4

For description purpose, in this document the timeslots reserved for STS-1#1 to STS-1#4 are denoted as master and the timeslots reserved for STS-1#5 to STS-1#12 are denoted as slave.

Figure 84 shows an STS-12/STM-4 data stream carrying 4 STS-3c/VC-4 payloads. In this figure, only the master timeslots can be inserted with valid path overhead bytes. The 3 master timeslots are reserved for each of the 4 sets of VC-4 path overhead.

Figure 84 HTPOH Timeslots for STS-3c/VC4 mapped with C4

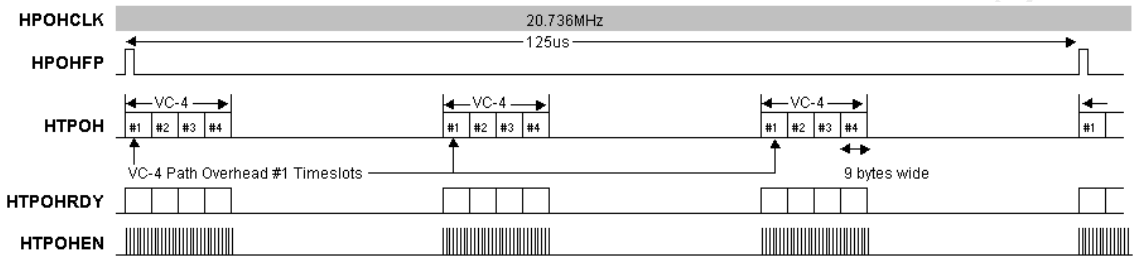


VC-4 with TUG-3

Figure 85 shows an STS-12/STM-4 data stream carrying 4 VC-4 payloads, and each VC-4 carries 3 TUG-3 payloads. Only the master timeslots are valid for insertion, and 3 master timeslots are reserved for each of the 4 sets of VC-4 path overhead.

Please note that the TUPP-2488 does not support low order path overhead bytes insertion. This includes TU3 payload as well.

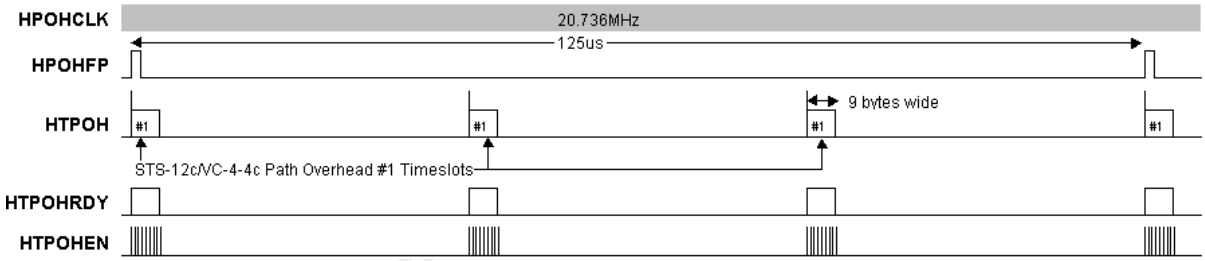
Figure 85 HTPOH Timeslot for VC-4 mapped with TUG3



STS-12c/VC-4-4c

Figure 86 shows the HTPOH timeslots for the case of an STS-12/STM-4 data stream carrying an STS-12c/VC-4-4c payload. The 3 timeslots are reserved for the VC-4-4c path overhead.

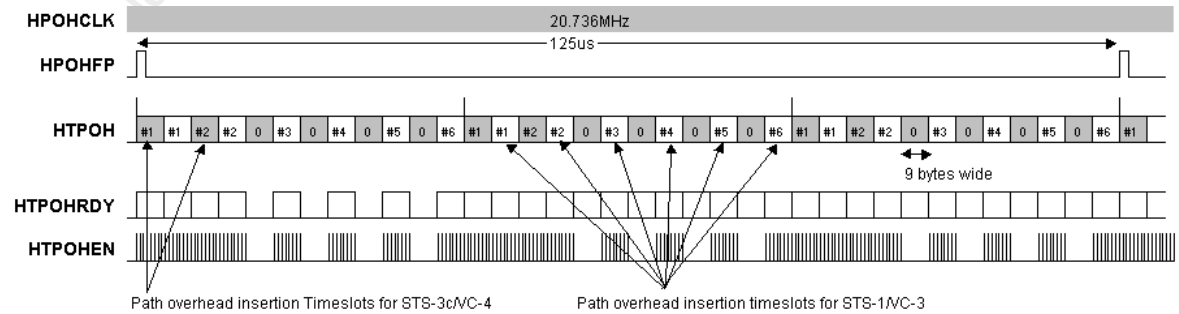
Figure 86 HTPOH Timeslot for STS-12c/VC4-4c



Legal Mix

The HTPOH port can also insert high-order path overheads for any legal mixture of payloads. Figure 87 shows an example of an STS-12/STM-4 data stream carrying 2 STS-3c/VC4 and 6 STS-1/STM-0.

Figure 87 HTPOH Timeslot for Mixture of STS-3c/VC-4 and STS-1/VC-3



14.9 High Order Receive Path Alarm

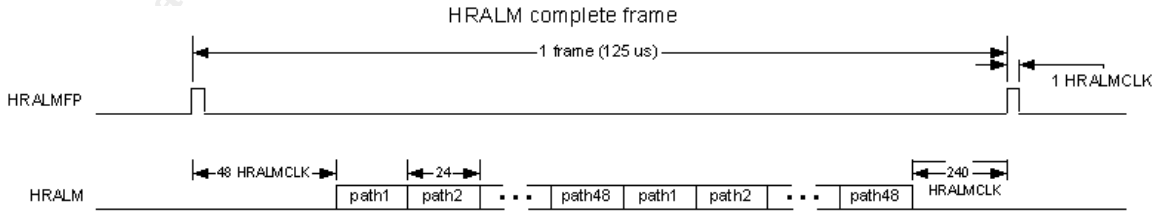
- The TUPP-2488 serially outputs the path alarm for all 48 paths through the High Order Receive Path Alarm port. The HRALM signal is set high for each of the 48 high order SONET/SDH paths when any of the following defects is active: LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PLM, and PDI-P. Each defect can be independently enabled or disabled for each path.
- The High Order Receive Path Alarm port is comprised of the following signals:
- HRALMCLK.
- HRALMFP.
- HRALM.

All signals on the High Order Receive Alarm port are referenced to the HRALMCLK signal. HRALMCLK is a nominal 20.736 MHz 33% high duty cycle clock. It is generated by gapping an internal 25.92 MHz clock. This means every 2 out of 10 clock edges are skipped to trigger exactly 2,592-clock pulses between each 125 µs interval. Note that all signals on this alarm port are updated on the falling edges of HRALMCLK.

The HRALMFP signal provides synchronization between the alarm port and the transport frame. It asserts high for 1 HPOHCLK clock cycle for every 125 µs. HRALMFP is used to identify the first of 2,592-clock pulses of HRALMCLK.

Figure 88 shows the functional timing of HRALM for one complete 125 µs interval. HRALM is time-multiplexed among the 48 STS-1/STM-0 paths. Each HRALM path is asserted or negated for 24 HRALMCLK consecutive cycles and the HRALM value cannot be changed during this duration. In each frame, HRALM reports all 48 paths alarm indications 2 times (two opportunities). The two opportunities are mostly identical, but they could be different when HRALM transitions in a frame depending on the frame timing. During the first 48 HRALMCLK and the last 240 HRALMCLK, the HRALM signal should be ignored.

Figure 88 High Order Receive Path Alarm Timing



15 Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 51 Maximum Ratings

Storage Temperature	-40°C to +125°C
Core Supply Voltage (VDDI)	-0.5V to 1.8V
I/O Supply Voltage (VDDO)	-0.5 V to +3.6 V
I/O Supply Voltage (VDDOPROG_M)	-0.5 to +4.6 V
I/O Supply Voltage (VDDOPROG_E)	-0.5 to +4.6 V
Voltage on Any Digital Pin	-0.3 V to VDDO+0.3 V
Input pad tolerance	-2 V < Vpin < VDDOx +2 V for 10 ns, 100 mA max
Output pad overshoot limits	-2 V < Vpin < VDDOx +2 V for 10 ns, 100 mA max
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+225 °C +0/- 5
Voltage of Overshoot of duration <10ns on any pin (unless otherwise specified)	-2.0V to VDDO+2.0 V
Junction Temperature under bias (correct operation not necessarily guaranteed)	-40°C to +125°C

Note

- VDDOx is the matching VDDO for the input pad in question.

16 Power Information

16.1 Power Requirements

Device power consumption varies with device configuration and operating conditions. The power requirements described in this document are appropriate for thermal and power system design maximums for a fully utilized device over all operating conditions, but may not be appropriate for all applications.

In all cases listed in Table 52:

- The power requirements are based on the ADM application with CCB and MSU-Lite bypassed.
- All the working and protect links are enabled unless otherwise specified.

Table 52 Power Requirements

Conditions	Parameter	Typ[1,2]	Power for Thermal Calculations	Max Current	Units
Line side: 622.08 MHz System side: 622.08 MHz Egress Parallel TelecomBus: disabled.	IDDOP (1.2V)	3.084	—	3.974	A
	IDDOP (2.5 V)	0.099	—	0.116	A
	IDDOP (3.3V)	0.004	—	0.006	A
	Total Power	**3.964**	**4.596**	**—**	**W**
Line side: 2.488 GHz. Unused links are disabled. System side: 622.08 MHz Egress Parallel TelecomBus: disabled	IDDOP (1.2V)	2.795	—	3.650	A
	IDDOP (2.5 V)	0.091	—	0.108	A
	IDDOP (3.3V)	0.004	—	0.006	A
	Total Power	**3.597**	**4.202**	**—**	**W**
Line side: 777.6 MHz System side: 777.6 MHz Egress Parallel TelecomBus: disabled.	IDDOP (1.2V)	3.115	—	4.025	A
	IDDOP (2.5 V)	0.100	—	0.117	A
	IDDOP (3.3V)	0.004	—	0.006	A
	Total Power	**4.003**	**4.647**	**—**	**W**
Line side: 777.6 MHz System side: 777.6 MHz Egress Parallel TelecomBus: enabled.	IDDOP (1.2V)	3.121	—	4.019	A
	IDDOP (2.5 V)	0.102	—	0.119	A
	IDDOP (3.3V)	0.028	—	0.033	A
	Total Power	**4.093**	**4.744**	**—**	**W**

Notes

1. Outputs loaded with 10 pF (if not otherwise specified), and a normal amount of traffic or signal activity.

2. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system.

16.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. There is no requirement on the order that power must be applied to or removed from any of the supply pins.

2. I/Os must only be driven after all the supplies have been powered. Otherwise, the I/Os must be current limited to 20 mA.

3. The RASIO™ CML receiver inputs do not require current limiting ***when the receiver is powered down*** provided the driving voltage is below 1.45V.

16.3 Power Supply Filtering

1. Use a single plane for both digital and analog grounds.

2. Provide separate analog and digital supplies, but otherwise connect the supply voltages together at one point close to the connector where the voltage is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

Refer to the TUPP2488 Hardware Design Guidelines (PMC-2020238) for a detailed description of power supply filtering requirements.

17 D.C. Characteristics

Unless otherwise specified, all DC and AC specifications in this data sheet are valid for the following voltage and temperature ranges.

Table 53 Core Supply Voltage (VDDI) Specification

Process	VDDI min [V]	VDDI typical [V]	VDDI max [V]
Core Supply	1.14	1.2	1.26

Table 54 I/O Supply Voltage (VDDO) Specification

Process	VDDO min [V]	VDDO typical [V]	VDDx max [V]
3.3V Tolerant 2.5V Supply	2.38	2.5	2.62

Table 55 Programmable I/O Supply Voltage (VDDOPROG_E, VDDOPROG_M) Specification

Process	VDDOPROG min [V]	VDDOPROG typical [V]	VDDOPROG max [V]
2.5V Supply	2.38	2.5	2.62
3.3V supply	3.135	3.3	3.465

Table 56 DC Characteristics for 3.3V LVTTL/LVCMOS (Programmable Drive I/O in 3.3V Mode)

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Conditions
VIL	Input Low Voltage	-0.3	—	0.8	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0	—	VDDOPROG+ 0.3	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	—	0.1	0.4	VDDO = 3.135, IOL –12ma for micro interface. -8ma for others
VOH	Output or Bidirectional High Voltage	2.4	2.7	—	VDDO = 3.135, IOH 12ma for micro interface. 8ma for others

Table 57 DC Characteristics for 2.5V LVCMOS (2.5V non-programmable Drive I/O)

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Conditions
VIL	Input Low Voltage	-0.3	—	0.7	Guaranteed Input LOW Voltage
VIH	Input High Voltage	1.7	—	3.6	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	—	0.1	0.4	VDDO = 2.38, IOL = -8ma for pins HRALMCLK, HPOHCLK, TPOH[4:1], TPOHEN[4:1], TPOHFP[4:1] and TRAD[4:1]. IOL = -4ma for others.
VOH spec.	Output or Bidirectional High Voltage	1.8	2.2	—	VDDO = 2.38, IOH = 8ma for pins HRALMCLK, HPOHCLK, TPOH[4:1], TPOHEN[4:1], TPOHFP[4:1] and TRAD[4:1]. IOH = 4ma for others.

Table 58 DC Characteristics for 2.5V LVCMOS (Programmable Drive I/O in 2.5V Mode)

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Conditions
VIL	Input Low Voltage	-0.3	—	0.7	Guaranteed Input LOW Voltage
VIH	Input High Voltage	1.7	—	VDDOPROG +0.3	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	—	0.1	0.4	VDDO = 2.38, IOL –12ma for micro interface. -8ma for others
VOH	Output or Bidirectional High Voltage	1.8	2.2	—	VDDO = 2.38, IOH 12ma for micro interface. 8ma for others

Notes

1. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing)

Table 59 DC Characteristics independent of Voltage levels

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VT+	Reset Input High Voltage	2.0	—	—	Volts	TTL Schmitt
VT-	Reset Input Low Voltage	—	—	0.8	Volts	TTL Schmitt
VTH	Reset Input Hysteresis Voltage	—	0.5	—	Volts	TTL Schmitt
IILPU	Input Low Current	+20	+83	+200	µA	VIL = GND. Notes 1, 3
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 1, 3
IIL	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 2, 3
IIH	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 2, 3
CIN	Input Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF

Notes

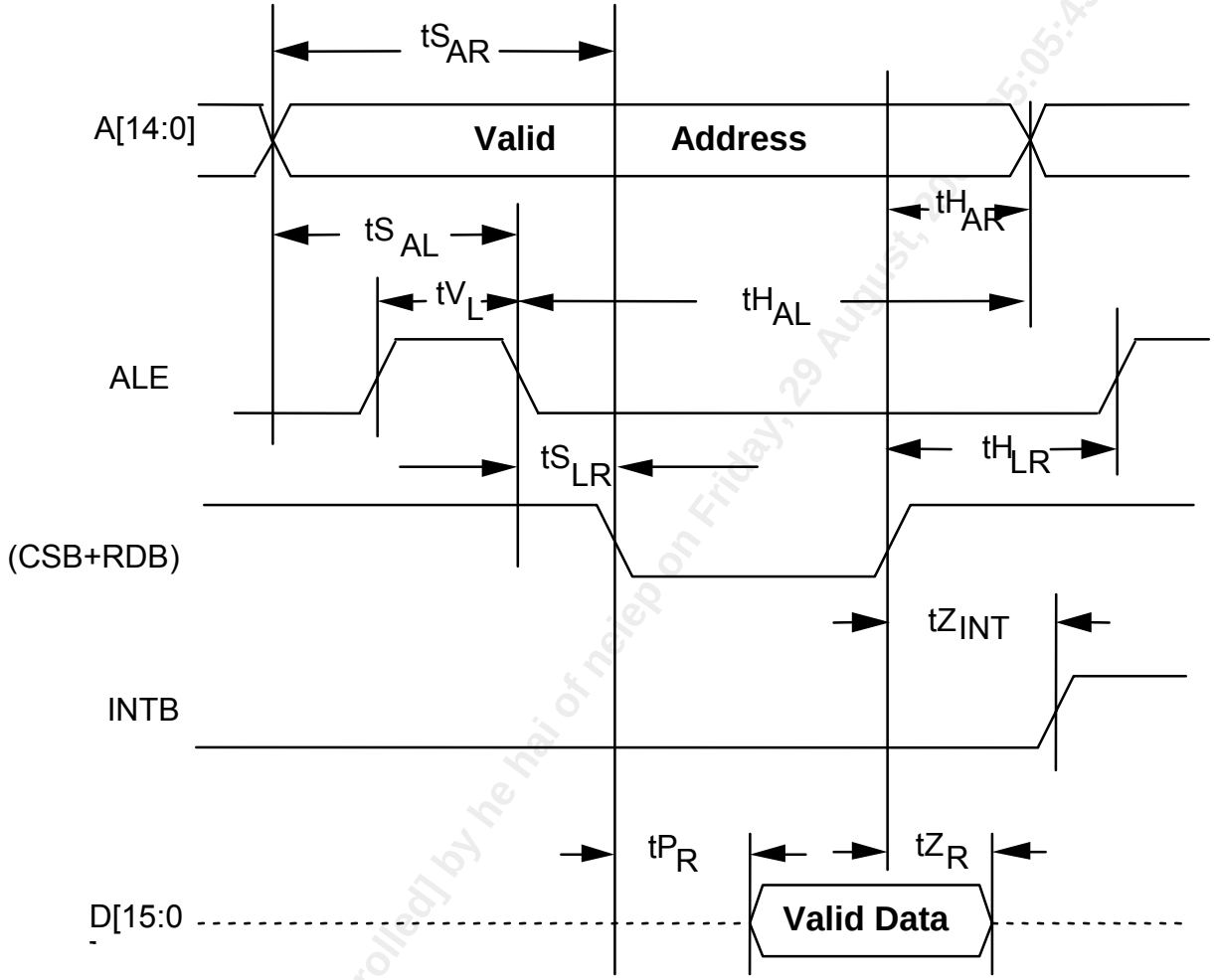
1. Input pin or bi-directional pin with internal pull-up resistor
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing)

18 Microprocessor Interface Timing Characteristics

Table 60 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	10	—	Ns
tHAR	Address to Valid Read Hold Time	20	—	ns
tSALR	Address to Latch Set-up Time	10	—	ns
tHALR	Address to Latch Hold Time	20	—	ns
tVL	Valid Latch Pulse Width	5	—	ns
tSLR	Latch to Read Set-up	0	—	ns
tHLR	Latch to Read Hold	5	—	ns
tPR	Valid Read to Valid Data Propagation Delay	—	70	ns
tZR	Valid Read Negated to Output Tri-state	—	20	ns
tZINTH	Valid Read Negated to Output Tri-state	—	50	ns

Figure 89 Microprocessor Interface Read Timing



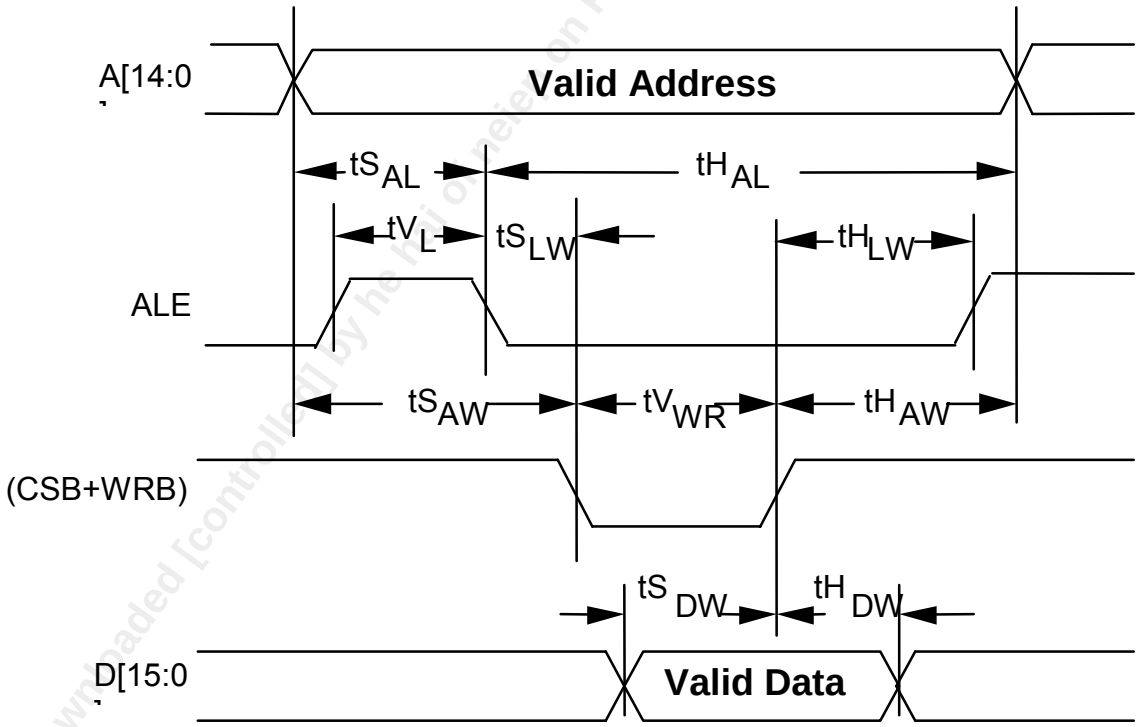
Notes

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0])
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable
5. Parameter tHAR and tSAR is not applicable if address latching is used
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock

Table 61 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10	—	ns
tSDW	Data to Valid Write Set-up Time	20	—	ns
tSALW	Address to Latch Set-up Time	10	—	ns
tHALW	Address to Latch Hold Time	10	—	ns
tVL	Valid Latch Pulse Width	20	—	ns
tSLW	Latch to Write Set-up	0	—	ns
tHLW	Latch to Write Hold	5	—	ns
tHDW	Data to Valid Write Hold Time	5	—	ns
tHAW	Address to Valid Write Hold Time	5	—	ns
tVWR	Valid Write Pulse Width	40	—	ns

Figure 90 Microprocessor Interface Write Timing



Notes

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, and tSLW are not applicable
3. Parameter tHAW is not applicable if address latching is used

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock

19 A.C. Timing Characteristics

T_a=-40°C to T_j=125°C, V_{VDDI}= $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{VDDOtypical}$ ± 5%, V_{AVDH}= $V_{AVDHtypical}$ ± 5%, V_{AVDL}= $V_{AVDLtypical}$ ± 5%,

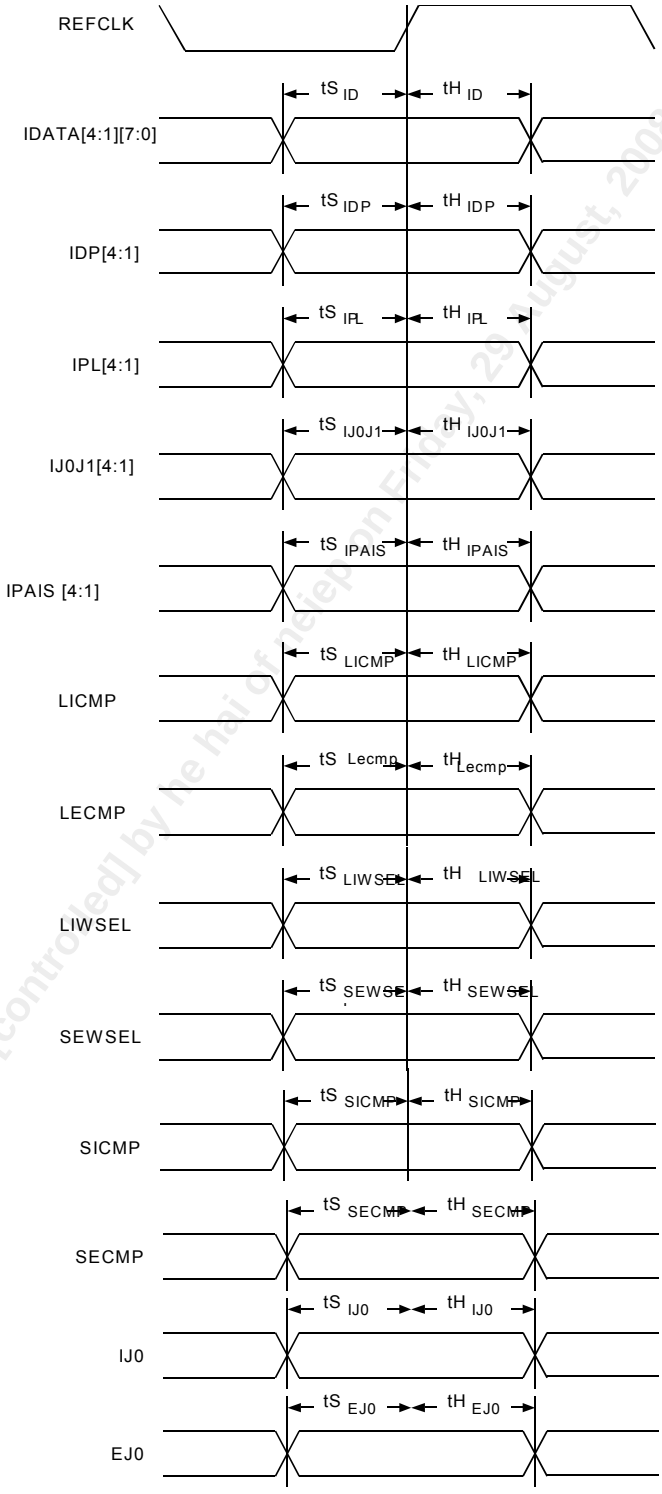
(Typical Conditions: T_J = 75°C, V_{VDDI} = 1.2V, V_{VDDO} = 2.5V, V_{AVDH} = 2.5V, V_{AVDL} = 1.2V)

19.1 TUPP 2488 Line Ingress Parallel Bus Timing

Table 62 TUPP 2488 Line Ingress Parallel Bus Timing

Symbol	Description	Min	Max	Units
	REFCLK Frequency (nominally 77.76MHz)	-50	+50	ppm
	REFCLK Duty Cycle	40	60	%
t_{SIDD}	IDATA[4:1][7:0] Set-up Time	3	—	ns
t_{HIDD}	IDATA[4:1][7:0] Hold Time	1	—	ns
t_{SIDP}	IDP[4:1] Set-up Time	3	—	ns
t_{HIDP}	IDP[4:1] Hold Time	1	—	ns
t_{SIPL}	IPL[4:1] Set-Up Time	3	—	ns
t_{HIPL}	IPL[4:1] Hold Time	1	—	ns
t_{SIJ0J1}	IJ0J1[4:1] Set-Up Time	3	—	ns
t_{HIJ0J1}	IJ0J1 [4:1] Hold Time	1	—	ns
t_{HIPAIS}	IPAIS[4:1] Set-Up Time	3	—	ns
t_{HIPAIS}	IPAIS [4:1] Hold Time	1	—	ns
t_{SLICMP}	LICMP Set-Up Time	3	—	ns
t_{HLICMP}	LICMP Hold Time	1	—	ns
t_{SLECMP}	LECMP Set-Up Time	3.1	—	ns
t_{HLECMP}	LECMP Hold-Up Time	1	—	ns
t_{SSICMP}	SICMP Set-Up Time	3	—	ns
t_{HSICMP}	SICMP Hold Time	1	—	ns
t_{SSECMP}	SECMP Set-Up Time	3	—	ns
t_{HSECMP}	SECMP Hold Time	1	—	ns
$t_{SLEWSEL}$	LEWSEL Set-Up Time	3	—	ns
$t_{HLEWSEL}$	LEWSEL Hold-Time	1	—	ns
$t_{SSEWSEL}$	SEWSEL Set-Up Time	3.3	—	ns
$t_{HSEWSEL}$	SEWSEL Hold Time	1	—	ns
t_{SIJ0}	IJ0 Set-Up Time	3.2	—	ns
t_{HIJ0}	IJ0 Hold Time	1	—	ns
t_{SEJ0}	EJ0 Set-Up Time	3.2	—	ns
t_{HEJ0}	EJ0 Hold Time	1	—	ns

Figure 91 TUPP 2488 Incoming Timing

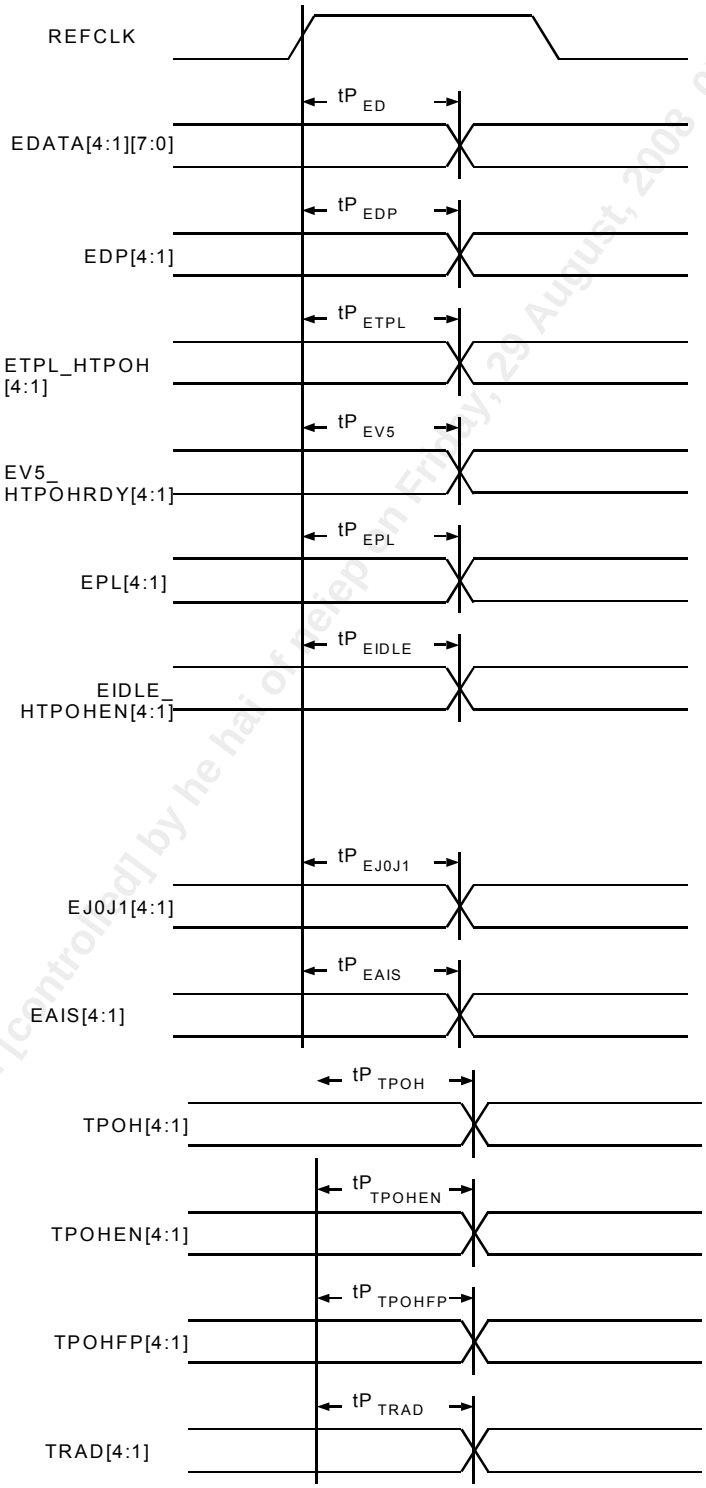


19.2 TUPP 2488 Line Egress Parallel Bus Timing

Table 63 TUPP 2488 Outgoing Timing with 77.76MHz REFCLK

Symbol	Description	Min	Max	Units
t_{PED}	REFCLK High to EDATA[4:1][7:0] Valid	1	7.5	ns
t_{PEDP}	REFCLK High to EDP[4:1] Valid	1	7.5	ns
t_{PETPL}	REFCLK High to ETPL_HTPOH[4:1] Valid	1	7	ns
t_{PEV5}	REFCLK High to EV5_HTPOHRDY[4:1] Valid	1	7	ns
t_{PEPL}	REFCLK High to EPL[4:1] Valid	1	7	ns
t_{PEIDLE}	REFCLK High to EIDLE_HTPOHEN[4:1] Valid	1	7	ns
t_{PEJ0J1}	REFCLK High to EJ0J1[4:1] Valid	1	7.5	ns
t_{PEAIS}	REFCLK High to EAIS[4:1] Valid	1	7.5	ns
t_{PTPOH}	REFCLK High to TPOH[4:1] Valid	1	7	ns
$t_{PTPOHFP}$	REFCLK High to TPOHEN[4:1] Valid	1	7	ns
$t_{PTPOHEN}$	REFCLK High to TPOHFP[4:1] Valid	1	7	ns
t_{PTRAD}	REFCLK High to TRAD[4:1] Valid	1	7	ns

Figure 92 TUPP 2488 Line Egress Parallel Bus Timing

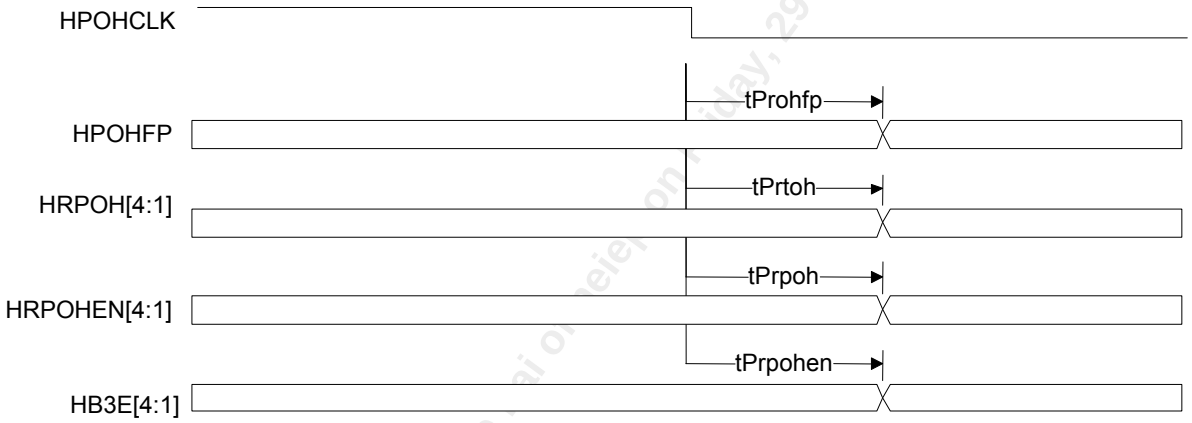


19.3 Receive High Order Path Overhead Port Timing

Table 64 HPOHCLK Output Timing for Serial Receive High Order Port

Symbol	Description	Min	Max	Units
tPHRPOH	HPOHCLK falling edge to HRPOH[4:1] valid	-7	7	ns
tPHRPOHFP	HPOHCLK falling edge to HPOHFP[1:4] valid	-7	7	ns
tPHRPOHEN	HPOHCLK falling edge to HRPOHEN[4:1] valid	-7	7	ns
tPHB3E	HPOHCLK falling edge to HB3E[4:1] valid	-7	7	ns

Figure 93 HPOHCLK Output Timing for Serial Receive High Order Port

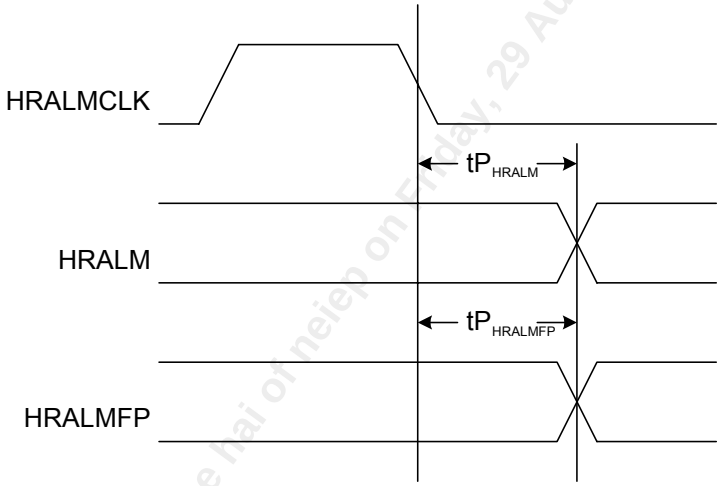


19.4 High Order Alarm Port (output Timing)

Table 65 TUPP 2488 Outgoing Timing with 77.76MHz REFCLK

Symbol	Description	Min	Max	Units
TPHRALM	HRALMCLK High to HRALM valid	-7	7	ns
TPHRALMFP	HRALMCLK High to HRALMFP valid	-7	7	ns

Figure 94 TUPP 2488 High Order Alarm Outgoing Timing



19.5 Transmit High Order Path Overhead Port Timing

Table 66 HPOHCLK Input Timing for Serial Transmit High Order Port

Symbol	Description	Min	Max	Units
tSHTPOH	ETPL_HTPOH[4:1] Set-up time to HPOHCLK rising edge	14	—	ns
tHHTPOH	ETPL_HTPOH[4:1] Hold time to HPOHCLK rising edge	0	—	ns
tSHTPOHEN	EIDLE_HTPOHEN[4:1] Set-up time to HPOHCLK rising edge	14	—	ns
tHHTPOHEN	EIDLE_HTPOHEN[4:1] Hold time to HPOHCLK rising edge	0	—	ns

Figure 95 HPOHCLK Input Timing for Serial Transmit High Order Port

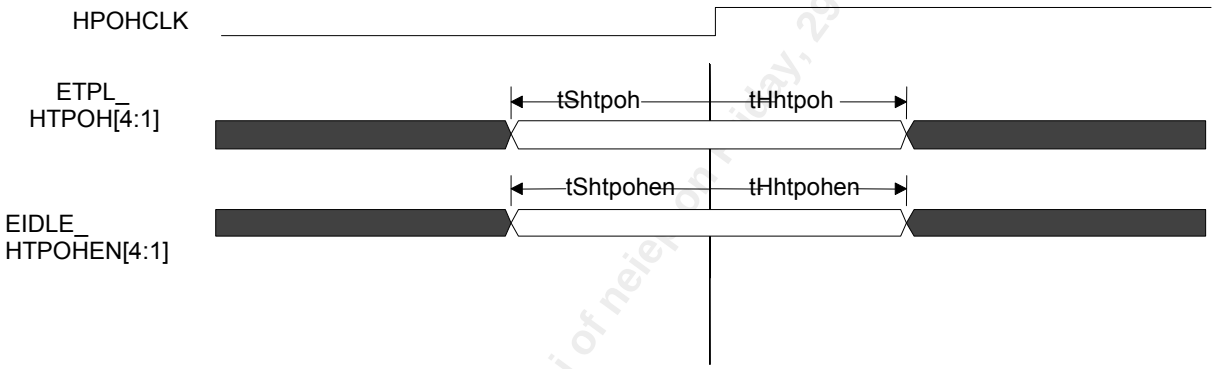
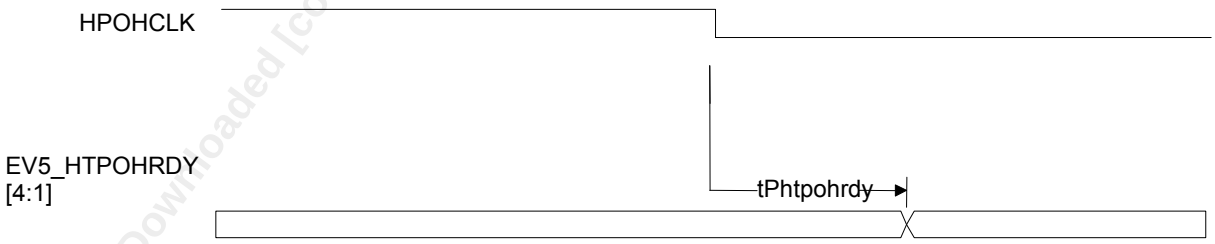


Table 67 HPOHCLK Output Timing for Serial Transmit High Order Port

Symbol	Description	Min	Max	Units
tPHTPOHRDY	HPOHCLK falling edge to EV5_HTPOHRDY[4:1] valid	1	8.3	ns

Figure 96 HPOHCLK Output Timing for Serial Transmit High Order Port

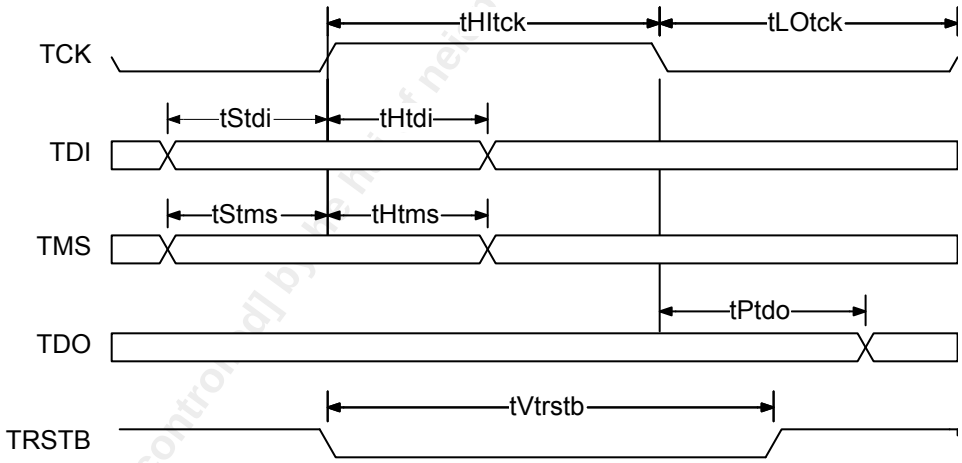


19.6 JTAG Port Interface

Table 68 JTAG Port Interface

Symbol	Description	Min	Max	Units
FTCK	TCK Frequency	—	4	MHz
THITCK	TCK HI Pulse Width	100	—	ns
THITCK	TCK LO Pulse Width	100	—	ns
TSTMS	TMS Set-up time to TCK	25	—	ns
THTMS	TMS Hold time to TCK	25	—	ns
TSTDI	TDI Set-up time to TCK	25	—	ns
THTDI	TDI Hold time to TCK	25	—	ns
TPTDO	TCK Low to TDO Valid	2	35	ns
TVTRSTB	TRSTB Pulse Width	100	—	ns

Figure 97 JTAG Port Interface Timing

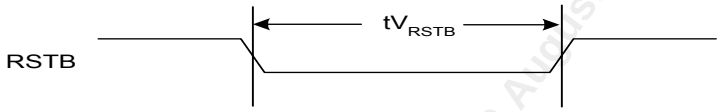


19.7 Reset Timing

Table 69 RSTB Timing (Figure 98)

Symbol	Parameterq	Min	Max	Units
tVRSTB	RSTB Pulse Width	100	—	ns

Figure 98 RSTB Timing



19.8 Transmitter Electrical Characteristics

Table 70 RASIO™ CML Transmitter Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_{DRF}	Differential rise/fall time, 20%-80%.	--	80	--	ps	100 ohm termination
Z_D	Differential Impedance	85	100	115	ohm	
Z_{SE}	Single-ended Impedance	42.5	50	57.5	ohm	
Djod	Output Data Deterministic Jitter (pk-pk between Data_Rate/1667 and Data_Rate/2	--	--	0.17	UI	2.488Gb/s
		--	--	0.08	UI	777.6Mb/s 622.08Mb/s
Tjod	Total Output Data Jitter (pk-pk between Data_Rate/1667 and Data_Rate/2	--	--	0.35	UI	2.488Gb/s
		--	--	0.14	UI	777.6Mb/s 622.08Mb/s

Notes

1. The above values do not include the reference clock jitter
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. 1UI (unit interval) = 1/data_rate. For 2.488Gb/s, 1UI = 402ps.

Table 71 CML Peak-Peak Differential (Vppd) Inner Eye Levels with Pre-Emphasis OFF

(See Figure 99 for signal definition)

No Pre-emphasis	50Ω[1] to 1.2V			100Ω Floating / 100Ω AC-coupled [1]		
TRANSMIT_MODE [4:0]	Min	Typ	Max	Min	Typ	Max
01000	431	560	644	426	561	668
01001	476	616	714	469	614	740
01010	520	673	784	511	670	809
01011	566	729	854	553	713	878
01100	610	784	922	594	755	927
01101	654	836	989	629	796	972
01110	702	888	1038	661	833	1020
01111	742	941	1091	691	868	1060
10000	787	988	1143	716	898	1099
10001	835	1036	1191	741	934	1132
10010	872	1085	1237	764	968	1165
10011	915	1127	1282	794	995	1193
10100	960	1174	1327	806	1015	1219

Notes

1. The swing levels are measured at the pin into an ideal 100ohm ±5% termination
2. Swing levels are based on 3.2Gb/s data. The swing levels are not expected to be more than 7% higher at 2.5Gb/s.

Figure 99 Transmitter AC Swing- Inner Eye Levels

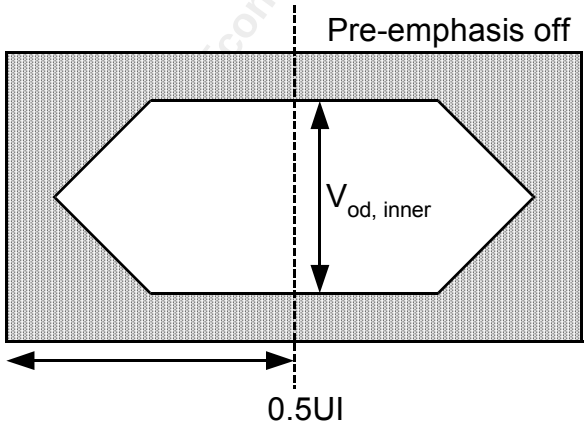


Table 72 CML Peak-Peak Differential (Vppd) Outer Eye Levels with Pre-Emphasis OFF

(See Figure 100 for signal definition)

No Pre-emphasis	50Ω [1] to 1.2V			100Ω Floating / 100Ω AC-coupled [1]		
TRANSMIT_MODE [4:0]	Min	Typ	Max	Min	Typ	Max
01000	495	610	750	490	608	780
01001	543	669	820	540	664	850
01010	592	727	888	586	718	915
01011	641	784	953	631	766	974
01100	690	839	1015	674	822	1029
01101	738	896	1075	717	876	1078
01110	786	955	1131	760	933	1122
01111	834	1013	1186	802	970	1176
10000	881	1070	1239	847	1021	1231
10001	928	1126	1287	890	1070	1282
10010	975	1181	1333	929	1142	1333
10011	1022	1235	1387	968	1184	1378
10100	1068	1289	1445	1004	1226	1415

Note:

1. The swing levels are measured at the pin into an ideal 100ohm ±5% termination
2. Swing levels are based on 3.2Gb/s data. The swing levels are not expected to be more than 7% higher at 2.5Gb/s.

Figure 100 Transmitter AC Swing – Outer Eye Levels

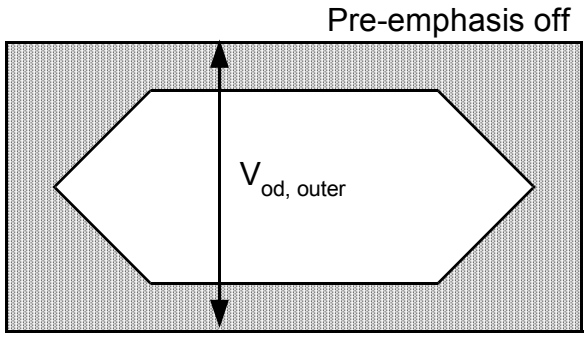


Table 73 Transmitter AC Swing with Pre-Emphasis ON (100 ohm floating Termination)

(See Figure 101 for signal definition)

High Levels				Low Levels				Attenuation (dB)
Transmit_ MODE [4:3]	V_{swHigh}(mVppd)			TRANSMIT_ MODE [2:0]	V_{swLow}(mVppd)			
	Min	Typ	Max		Min	Typ	Max	Typ
				000	447	547	615	-4.65
				001	490	600	688	-3.84
				010	530	656	747	-3.06
				011	572	710	808	-2.38
				100	613	760	867	-1.79
				101	657	814	928	-1.19
				110	700	866	987	-0.65
00	743	934	1100	111	738	910	1036	-0.22
				000	447	547	615	-4.88
				001	490	600	688	-4.08
				010	530	656	747	-3.30
				011	572	710	808	-2.62
				100	613	760	867	-2.02
				101	657	814	928	-1.43
				110	700	866	987	-0.89
01	770	960	1130	111	738	910	1036	-0.46
				000	447	547	615	-5.15
				001	490	600	688	-4.35
				010	530	656	747	-3.57
				011	572	710	808	-2.88
				100	613	760	867	-2.29
				101	657	814	928	-1.70
				110	700	866	987	-1.16
10	790	990	1162	111	738	910	1036	-0.73
				000	447	547	615	-5.33
				001	490	600	688	-4.56
				010	530	656	747	-3.75
				011	572	710	808	-3.06
				100	613	760	867	-2.47
				101	657	814	928	-1.88
				110	700	866	987	-1.34
11	820	1011	1185	111	738	910	1036	-0.91

Note:

1. The swing levels are measured at the pin into an ideal 100ohm ±5% termination

2. Swing levels are based on 3.2Gb/s data. The swing levels are not expected to be more than 7% higher at 2.5Gb/s.

Table 74 Transmitter AC Swing with Pre-Emphasis ON (50 ohm Termination to 1.2V)

(See Figure 101 for signal definition)

High Levels				Low Levels				Attenuation (dB)
Transmit_ MODE [4:3]	V_{swHigh}(mVppd)			TRANSMIT_ MODE [2:0]	V_{swLow}(mVppd)			
	Min	Typ	Max		Min	Typ	Max	Typ
				000	454	565	640	-5.33
				001	502	627	708	-4.42
				010	549	684	774	-3.67
				011	601	740	837	-2.98
				100	644	800	910	-2.31
				101	692	855	970	-1.73
				110	741	914	1038	-1.15
00	837	1044	1204	111	788	970	1093	-0.63
				000	454	565	640	-5.74
				001	502	627	708	-4.83
				010	549	684	774	-4.08
				011	601	740	837	-3.39
				100	644	800	910	-2.71
				101	692	855	970	-2.14
				110	741	914	1038	-1.56
01	889	1094	1252	111	788	970	1093	-1.04
				000	454	565	640	-6.02
				001	502	627	708	-5.12
				010	549	684	774	-4.36
				011	601	740	837	-3.68
				100	644	800	910	-3.00
				101	692	855	970	-2.43
				110	741	914	1038	-1.85
10	932	1131	1287	111	788	970	1093	-1.33
				000	454	565	640	-6.37
				001	502	627	708	-5.47
				010	549	684	774	-4.71
				011	601	740	837	-4.03
				100	644	800	910	-3.35
				101	692	855	970	-2.77
				110	741	914	1038	-2.19
11	970	1177	1330	111	788	970	1093	-1.68

Note:

1. The swing levels are measured at the pin into an ideal 100ohm ±5% termination

2. Swing levels are based on 3.2Gb/s data. The swing levels are not expected to be more than 7% higher at 2.5Gb/s.

Figure 101 Transmitter AC Swing with Pre-Emphasis ON

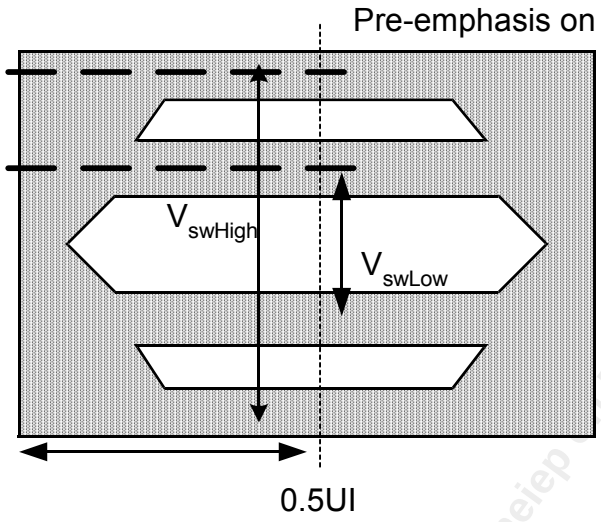


Table 75 CML Common-Mode Output Levels, Vcm (mV)

No Pre-emphasis	Pre-emphasis	50Ω to 1.2V (±5%) [1, 2]			100Ω Floating [1, 2]		
TRANSMIT_MODE [4:0]	TRANSMIT_MODE [4:0]	Typ	Min	Max	Typ	Min	Max
01000	-	1058	950	1128	916	830	967
01001	-	1042	934	1114	885	801	935
01010	-	1027	918	1099	855	773	903
01011	-	1011	902	1084	825	745	871
01100	-	996	886	1070	795	718	840
01101	-	981	871	1056	767	691	810
01110	-	965	855	1042	739	665	780
01111	-	950	840	1028	712	639	752
10000	-	935	825	1014	685	615	724
10001	00XXX	921	810	1000	660	591	699
10010	01XXX	906	796	985	636	569	679
10011	10XXX	892	782	971	614	549	662
10100	11XXX	878	768	958	595	530	650

Notes

1. The receiver termination is assumed to have a tolerance of ± 5%.
2. Common-Mode level is not specified for the AC-coupled case.

19.9 Receiver Electrical Characteristics

Table 76 RASIO™ CML Receiver Input Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DJid	Deterministic Jitter	--	--	0.44	UI	
TJid	Total Jitter[1,2]	--	--	0.74	UI	
Z_{INDIFF}	Differential Impedance	85	100	115	Ω	
V_{tt}	Termination Voltage	1.1	1.2	1.26	V	
L_{DR}	Differential Return Loss	10.5	--	--	dB	From 0.004*baud rate to 0.75*baud rate (Simulated value)
V_{Rsense}	Differential Input Sensitivity	175	--	--	mVpp	Peak-to-Peak Differential (Measured at the middle of the eye)
V_{Rmax}	Max Differential Input Voltage	--	--	2.2	Vpp	Peak-to-Peak Differential
T_{Reye}	Receiver Eye Opening	0.26	--	--	UI	
V_{RCM}	Common Mode Range	0.2	--	1.6	V	If AC-coupled, $V_{RCM} = V_{tt}$
R_{TERM}	Differential Termination resistance (see Figure 57)	85	100	115	Ω	
R_{SERIES}	Series resistance (see Figure 57)	--	--	2	Ω	

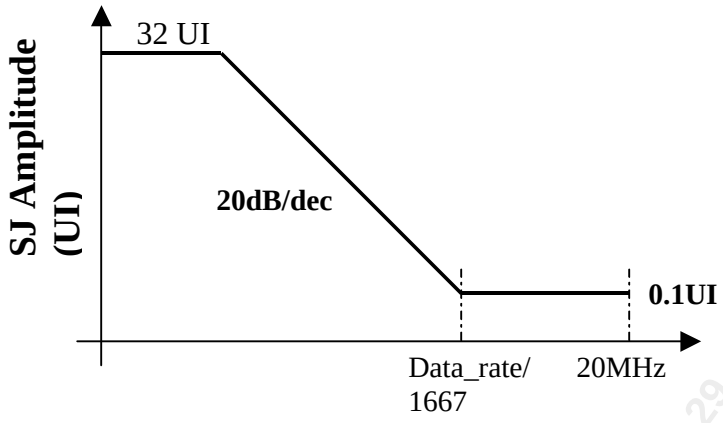
Notes

1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
2. Jitter specs are for bit-error rate (BER) <= 10e-12.

19.9.1 Receiver Wander Requirements

The receiver should be able to tolerate sinusoidal jitter as defined by Figure 102.

Figure 102 Sinusoidal Jitter Tolerance Mask



Note:

1. For TFI-5 compliant devices: The sinusoidal jitter tolerance is measured with at least 0.27UIpp of Deterministic jitter and the sum of Dj and Rj should be at least 0.55UIpp. Therefore the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65UIpp (Dj= 0.27, Rj= 0.28, Sj= 0.1).

19.9.2 Reference Clock Input

Table 77 Reference Clock Input Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DCref	REFCLK Duty Cycle	45	--	55	%	
TJref	REFCLK Total Jitter at Chip pin. (12kHz-20MHz RMS)	--	--	4	pS RMS	See Note 1
tRFref	REFCLK Rise / Fall Times (20% to 80%)			1	ns	
Z_{INDIFF}	Differential Impedance	85	100	115	Ω	
V_{Rsense}	Differential Input Sensitivity	175	--	--	mVpp	Peak-to-Peak Differential
V_{Rmax}	Max Differential Input Voltage	--	--	2.2	Vpp	Peak-to-Peak Differential
R_{TERM}	Differential Termination resistance (see Figure 57)	85	100	115	Ω	

Notes

1. Total jitter includes both deterministic jitter and random jitter but it is assumed the majority of the jitter is random. The REFCLK jitter specification can be relaxed for transmitter rates below or equal to 777.6Mb/s. The amount of allowable REFCLK jitter will depend on the system jitter budget.
2. Reference Clock inputs must be AC-coupled.

20 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for use in central office equipment[1].

Table 78 Central Office Thermal Information

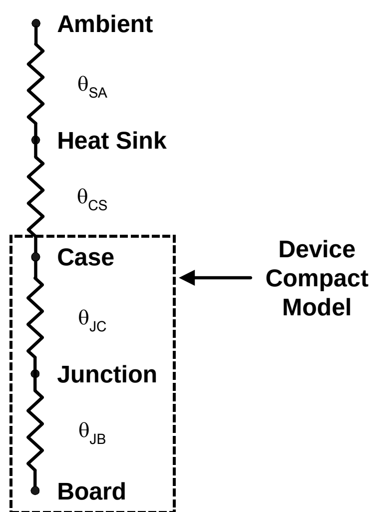
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 70 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 79 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	.29 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	4.24 °C/W

Table 80 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of $\theta_{SA} + \theta_{CS}$ must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation



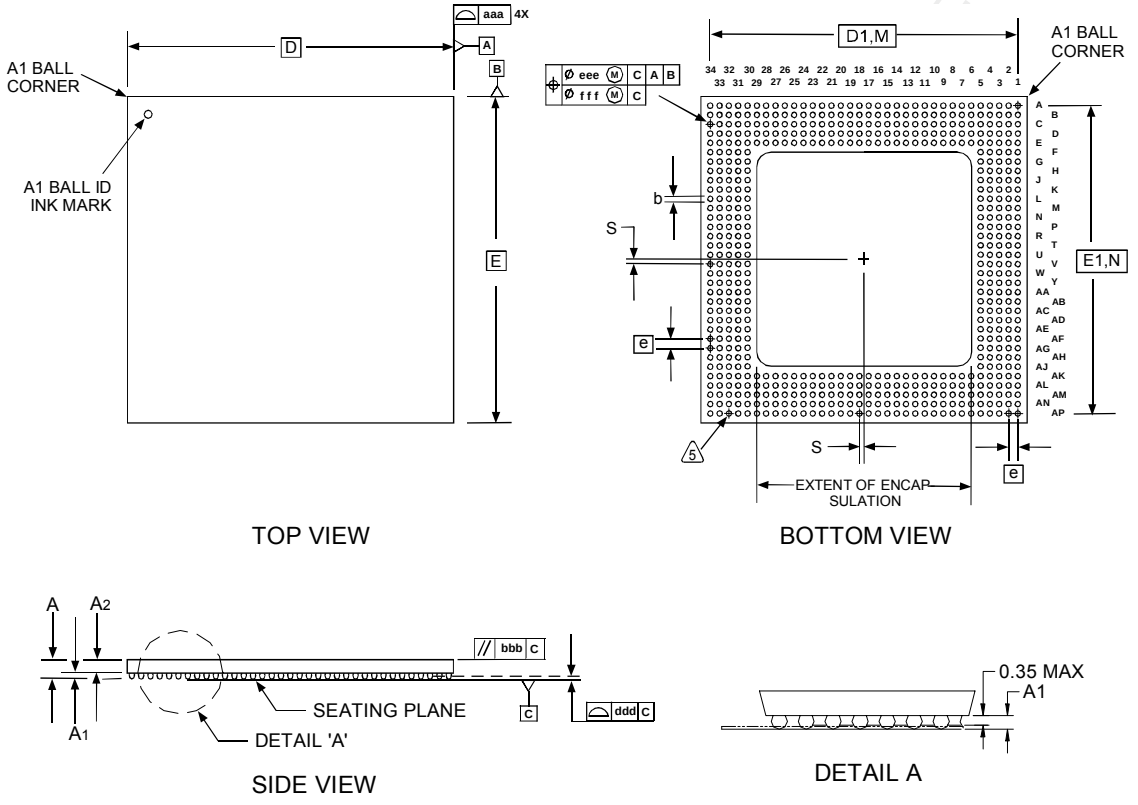
Power depends upon the operating mode. To obtain power information, refer to the 'High' power values in section 16.1 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Central Office Equipment approximates the minimum ambient temperature requirement for Commercial Equipment .
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core; for more information about the GR-63-CORE standard, see [15].
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about the JESD51-8 standard, see [14].
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place.

21 Mechanical Information

The package is a 580 ball CSBGA+ with a body size of 35 mm x 35 mm.



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.435 +/- 0.03 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MS-034, VARIATION AAR-1.

PACKAGE TYPE : 580 THERMALLY ENHANCED BALL GRID ARRAY - CSBGA+																
BODY SIZE : 35 x 35 x 1.47 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	1.32	0.40	0.92	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.47	0.50	0.97	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.60	1.00 BSC	-	-	-	-	-	-
Max.	1.62	0.60	1.02	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.25	0.10	0.50

22 Ordering Information

PART NO.	Description
PM5364-BI	580 CSBGA+

Notes