STB7720L

2.4-2.5 GHz Silicon Linear Power Amplifier IC

PRELIMINARY DATA

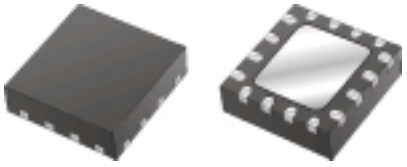
FEATURES SUMMARY

- EXCELLENT LINEARITY EVM 2% @ 19dBm (WITH 802.11g OFDM 54Mb/s MODULATION)
- VERY LOW QUIESCENT CURRENT (60mA)
- INTEGRATED LINEAR ANALOG CONTROL FOR DC CURRENT AND OUTPUT MANAGEMENT
- INTEGRATED AVERAGE CHANNEL POWER DETECTOR
- LEADLESS PACKAGE (3mmx3mm LEAD FREE)

APPLICATIONS

- OPTIMIZED FOR USE IN 802.11 b/g

Figure 1. Package



QFN16L (3x3)

DESCRIPTION

The STB7720L, manufactured in the third generation of ST proprietary pure Si bipolar process, is a three-stage linear power amplifier (PA) optimized for 802.11b/g wireless LAN (WLAN) applications in the 2.4GHz ISM band. It features 32dB of power gain and delivers 19dBm of linear output power with an EVM degradation of only 2% under 802.11g Modulation (54Mbps).
The current consumption is as low as 125mA at 19dBm make the STB7720L a good solution for mobile applications. It achieves less than -40dBc firstside lobe suppression and less than -52dBc secondside lobe suppression under 802.11b modulation (11Mbps).
The device embeds a Linear Analog Control for DC current and output management and a Proprietary Average Channel Power Detector solution. This power detector has 20dB dynamic range with 1 voltage range and ±0.3dB accuracy under 2:1 load mismatch. It provides a buffered DC voltage proportional to the average channel output power. Thanks to this solution we save cost and space by removing a coupler, an op amp (usually required in a power down function) and also an integrator.
The SBT7720 is housed in QFN 3mmx3mm Leadless package.

Table 1. Order Codes

Order Codes	Marking	Package	Packaging
STB7720	7720	QFN16L (3x3)	Tape & Reel

Table 2. Absolute Maximum Ratings (T_{amb} = 25 ^{o}C)

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	5.5	V
T_{stb}	Storage temperature	-55 to + 150	^{o}C
T_a	Operating Ambient Temperature	-30 + 85	^{o}C
P_{in}	Input Power	10	dBm

Table 3. Thermal Data

$R_{th(j\text{-}case)}$	Thermal Resistance Junction-Case	TBD	^{o}C/W

Figure 2. Functional Block Diagram

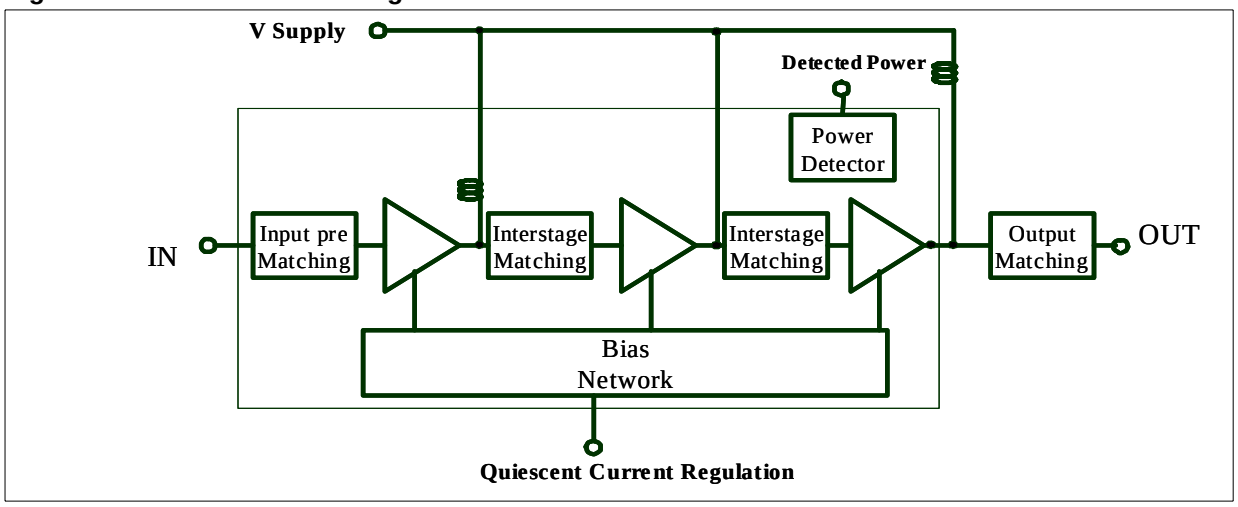


Figure 3. Pin Connection

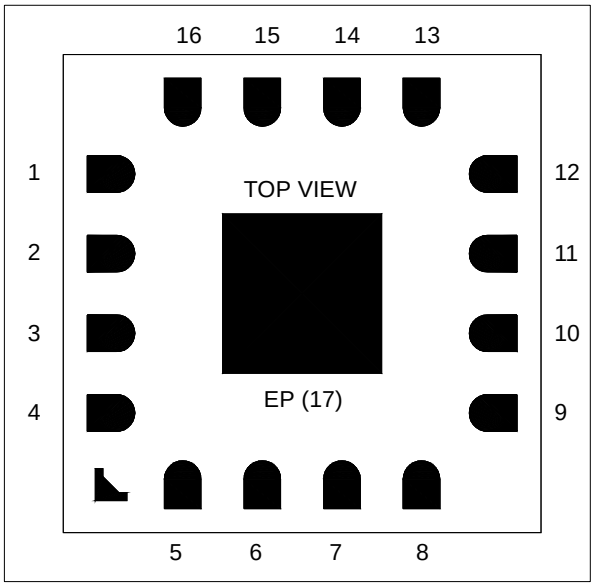


Table 4. Pin Description

PIN	Symbol	Function
1	nc	-
2	RFin	RF input
3	Vcnt	Power Control Voltage
4	Epd	Enable Power Detector
5	Vcc	Supply Voltage
6	VDET	Power Detector Voltage
7	nc	-
8	nc	-
9	nc	-
10	RFout	RF output
11	RFout	RF output
12	nc	-
13	nc	-
14	Vcc	Supply Voltage
15	nc	-
16	Vcc	Supply Voltage
EP	GND	Ground

Table 5. Electrical Characteristics (T_{amd} = 25 °C, V_{cc}=3.3V, f=2.45GHz, Vcnt = 2.9V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f	Frequency		2.4	2.45	2.5	GHz
V_{cc}	Supply Voltage		3.0	3.3	3.6	V
Icc(1)	Current Consumption	P_{out} = 19 dBm		125		mA
Gp	Power Gain			32		dB
P_{1dB}	P1dB Compression			25		dBm
	Gain variation over Frequency			-/+ 0.5		dB
	Gain variation over Temperature			-/+ 0.5		dB
	Quiescent Current			60		mA
EVM(1)	Error Vector Magnitude	P_{out} = 19 dBm		2		%
ACPR(2)	Adiacent Channel Power Ratio	P_{out} = 19dBm, 1st Side Lobe P_{out} = 19dBm, 2nd Side Lobe		-40 -52		dBc dBc
V_{det}	Output Detector Voltage Range			1		V
	Output Detector Voltage Response Time				4	µs
	2nd to 5th Harmonics				-40	dBc
	Spurious (stability)(3)	Load VSWR 10:1		-65		dBc
	Turn On Time(4)			0.5		µs

Notes:
(1) Parameter measured with RF modulation based on IEEE 802.11g standard (OFDM 54Mbps)
(2) Parameter measured with RF modulation based on IEEE 802.11b standard (CCK 11Mbps)
(3) Load VSWR is set to 10:1 and the angle is varied 360 degrees. Pout = -30 dBm to P1dB
(4) Measured from Device On signal turn on to the point where RF Pout stabilizes to 0.5dB

TYPICAL PERFORMANCE

Figure 4. Supply Current Vs Output Power

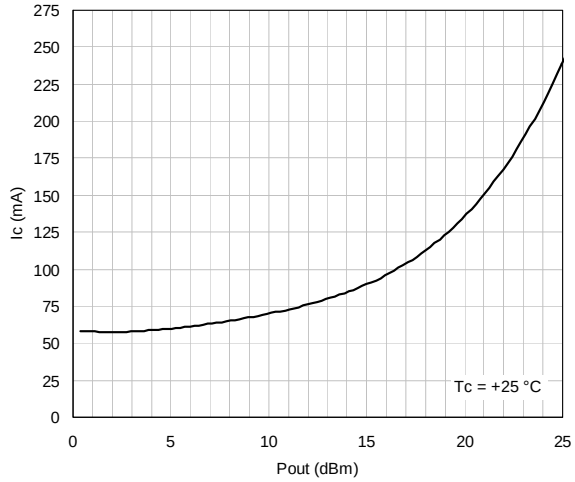


Figure 5. EVM Vs Output Power

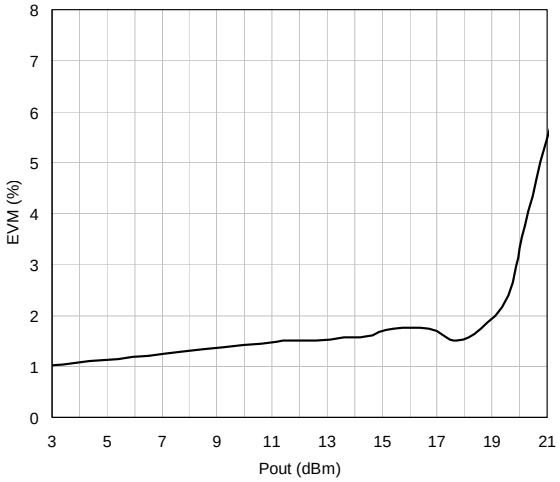


Figure 6. Power Gain Vs Output Power

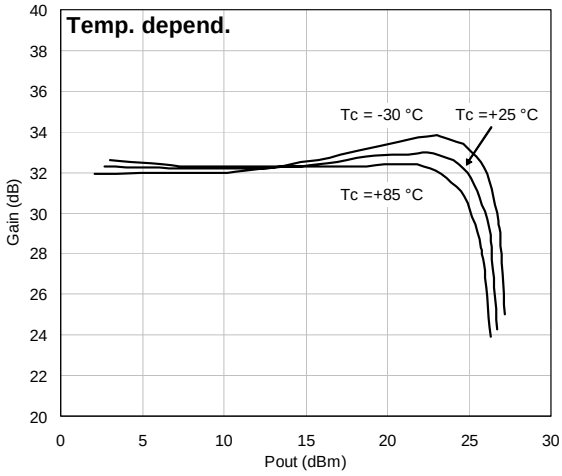


Figure 7. Power Gain Vs Frequency

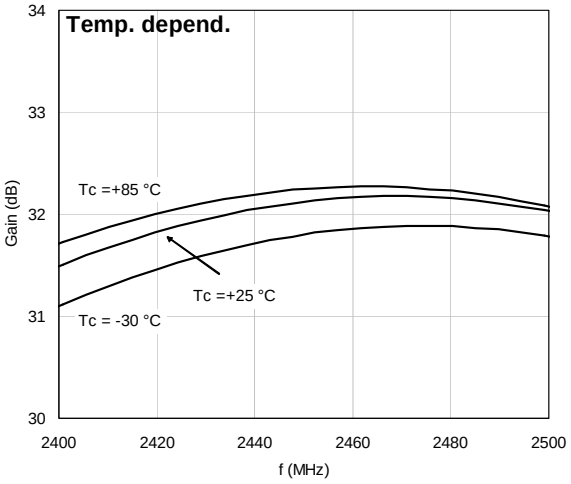


Figure 8. Power Detector Voltage Vs Pout

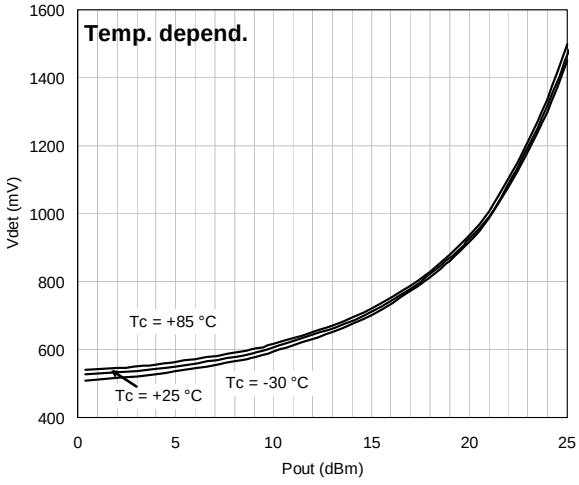


Figure 9. Power Detector Voltage Vs Pout

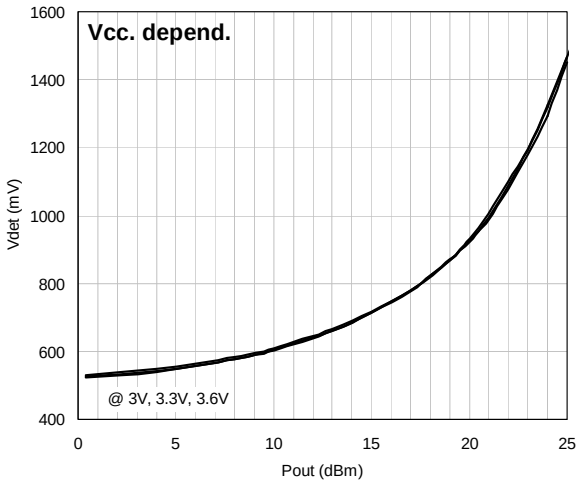
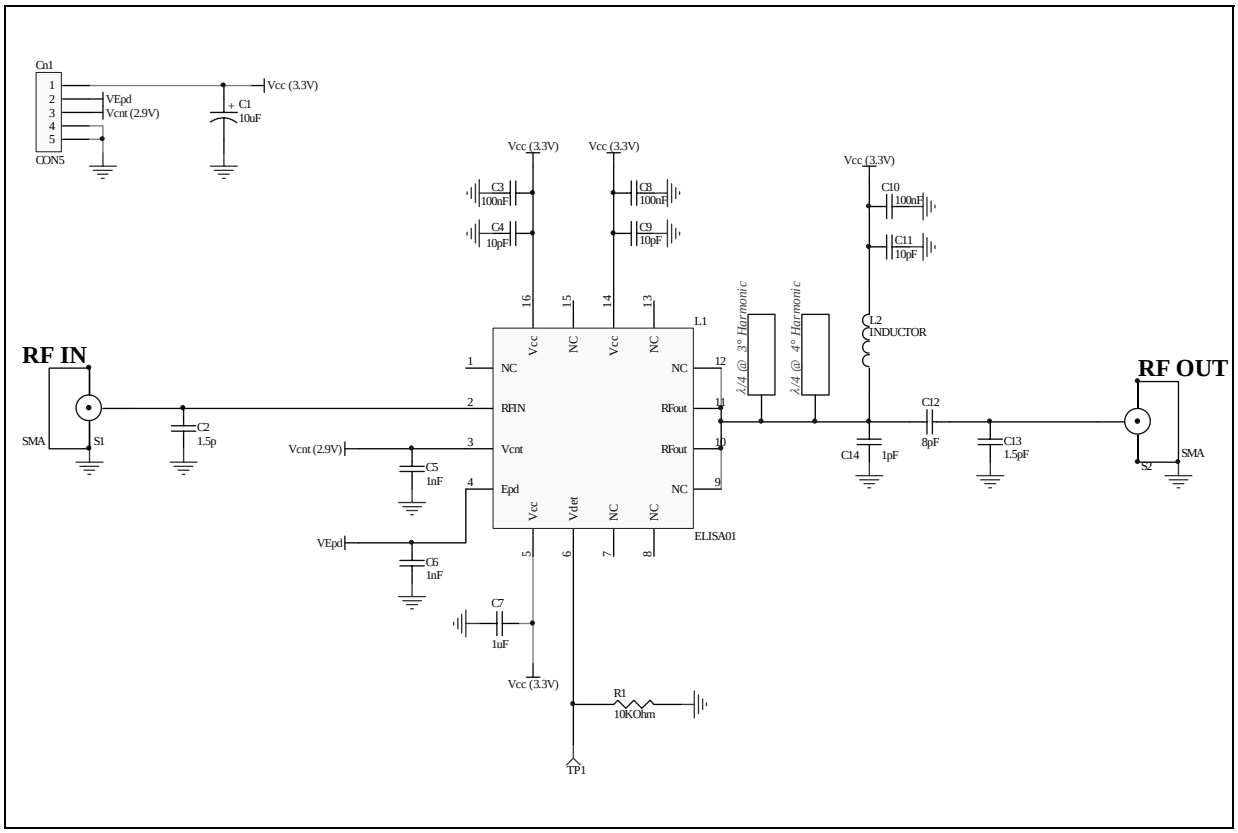


Figure 10. Circuit Schematic

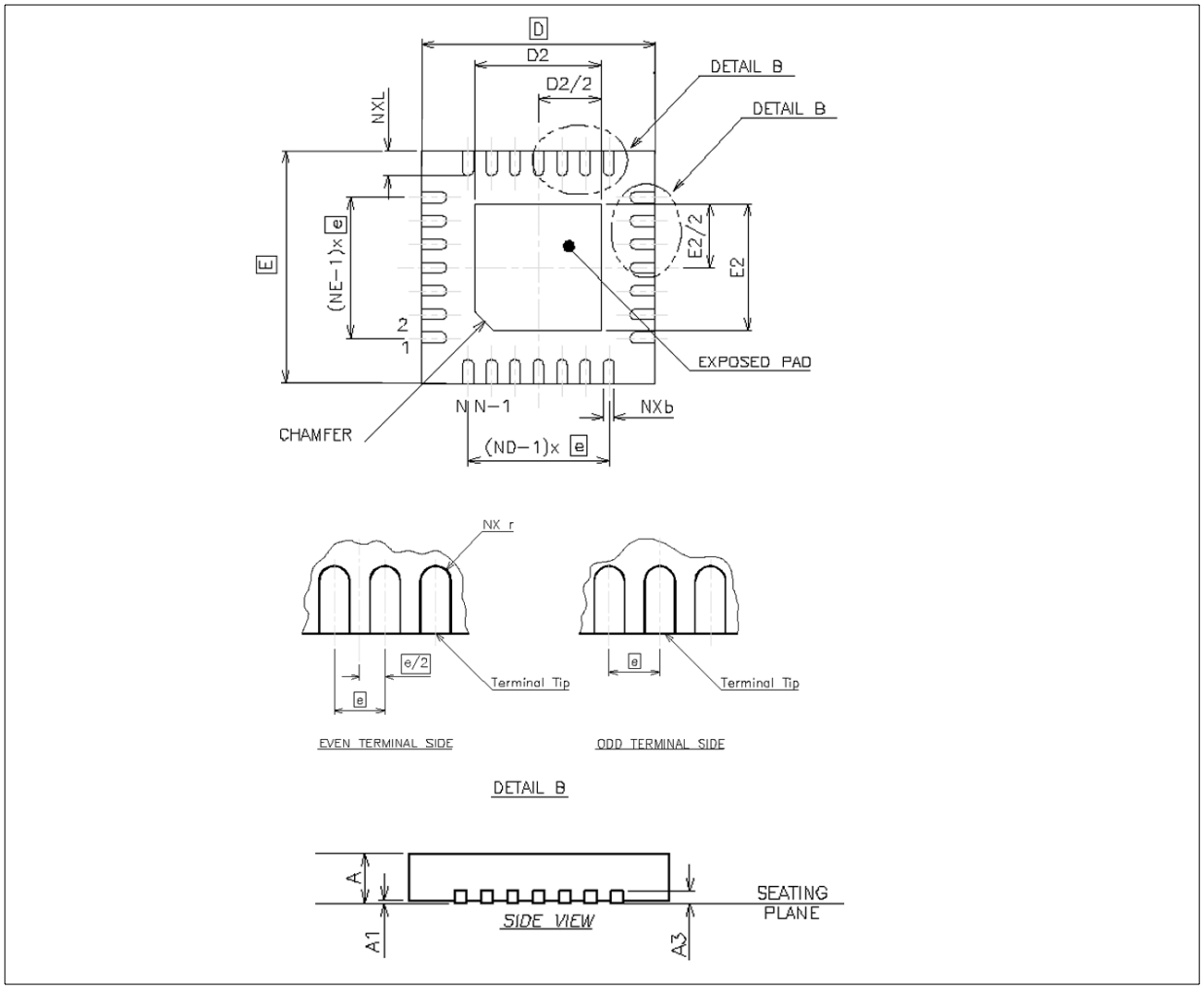


PACKAGE MECHANICAL

Table 6. Mechanical Data - Leadless PACKAGE Exposed Pad (3mm x 3mm)

DIM.	mm		
	MIN.	TYP.	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D		3.00 BSC	
D2	1.30	1.45	1.55
E		3.00 BSC	
E2	1.30	1.45	1.55
e		0.50 BSC	
L	0.30	0.40	0.50
N		16	
ND		4	
NE		4	

Figure 11. Package Dimensions



REVISION HISTORY

Table 7. Revision History

Date	Revision	Description of Changes
2 August 2004	1	First Release