IBM®

STB01000 and STB01010
Digital Set-Top Box Integrated Controller
Product Overview
Version 1.2

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Chapter 1. Introduction

1.1 STB Integrated Controller Overview

The IBM® STB01000 and STB01010 Digital Set-Top Box Integrated Controllers (STB010x0) are single-chip Application Specific Standard Products (ASSPs). The STB01000 offers standard digital (MPEG, PCM, LPCM) audio support, while the STB01010 provides Dolby® Digital (AC-3) audio capability. Both products are PowerPC 401™D2-based. This highly integrated silicon system has been specifically developed for digital STB applications using industry-leading IBM CMOS 5SE (0.35µm) process and IBM Blue Logic™ technology for set-top box applications.

1.2 IBM STB Architecture Design Attributes

The STB010x0 represents the latest IBM solution for digital set-top box components. The PowerPC and peripheral I/O architecture, coupled with the audio and video subsystems, provide high-level performance and functionality.

This architecture provides the following features:

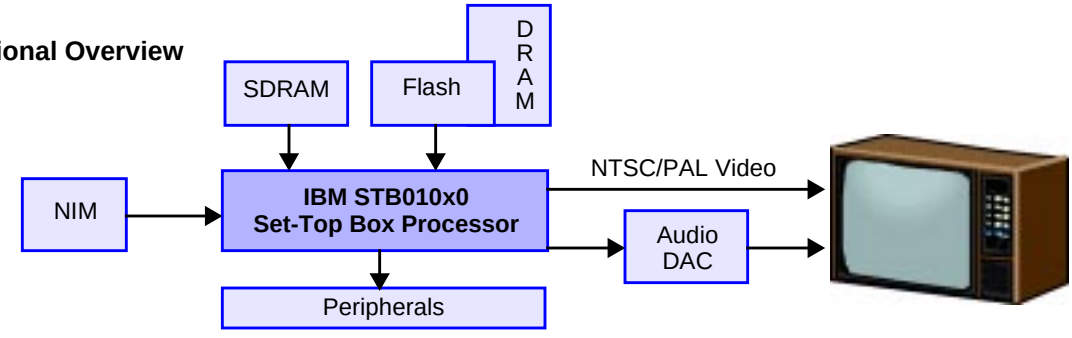
- Minimizes host processor intervention, providing maximum MIPS for operating system and application tasks.
- Simplifies driver and software development.
- Provides maximum on-chip communication efficiency and performance.
- Is designed for scaleability, flexibility, extendibility, and ease of use.

The STB010x0 also provides a full-function STB technology that is easy to use and meets cost and power requirements.

1.3 Features

- PowerPC 401D2 32-Bit RISC CPU core
- High-performance MPEG-2 transport, audio, and video cores
- Optional Dolby Digital audio
- MPEG-2 and digital video broadcasting (DVB) system requirements-compliant
- Multiple peripheral ports for easy interconnect:
  - 1284 parallel port

Functional Overview



  - Two Inter-Integrated Circuit (IIC) interfaces
  - Two Smart Card interfaces (through single controller)
  - Serial Communication Controller (SCC)
  - Serial Interface Communications Controller with IrDA
- Internal DMA and high-speed SDRAM and DRAM controller
- Single 27-MHz system clock input

1.4 Specifications

Table 1-1. IBM STB010x0 Specifications	
CPU core performance	49.5MHz
Technology	0.35-µm CMOS
Power supply	3.3V (supports 3V and 5V I/Os)
Operating temperature	0° C to 70° C (ambient)
Packaging	304-pin, 31-mm PBGA
Power	2.5 watts (nominal)
Part numbers (P/Ns)	IBM39 STB01000 PBB 22C IBM39 STB01010 PBB 22C
Note: Dolby Digital is only available on STB01010.	

1.5 Description

More than 20 essential set-top box elements have been engineered in the STB010x0. Architecturally, this chip consists of discrete units that are functionally partitioned into four major subsystems: PPC401D2 Core processor; digital audio/video subsystem; memory interface subsystem; and peripheral subsystem. All four subsystems are connected and tuned, using additional units that embody the IBM multiple-bus, on-chip interconnect structure.

The PPC401D2 subsystem includes:

- PPC401D2 CPU
- Code Pack Code Decompression
- Universal Interrupt Controller (UIC)
- On-Chip Memory (CCM)

The MPEG-2 Digital Audio/Video subsystem includes:

- MPEG-2 Video Decoder
- MPEG-2 Audio Decoder
- Dolby Digital Audio Support[1]
- MPEG-2 Transport/DVB Descrambler

1. Dolby Digital support available only on STB01010, Dolby Digital license required.

- NTSC/PAL DENC with Macrovision[1]

The memory subsystem includes:

- DMA Controller
- Cross-Bar Switch
- External Bus Interface Unit (EBIU) for EDO DRAM, SRAM, and Flash interface
- SDRAM Controller (SDRAMC) (also known as High Speed Memory Controller [HSMC])

The peripheral subsystem includes the following functions attached to the on-chp peripheral bus (OPB) via the OPB bridge:

- General Purpose Timers (GPTs) and PWM
- 1284 Printer interface
- Two Smart Card interfaces
- Two IIC interfaces
- SICC Serial interface
- SCC interface
- Modem CODEC Serial interface
- Serial Controller Port (SCP)
- General Purpose I/Os

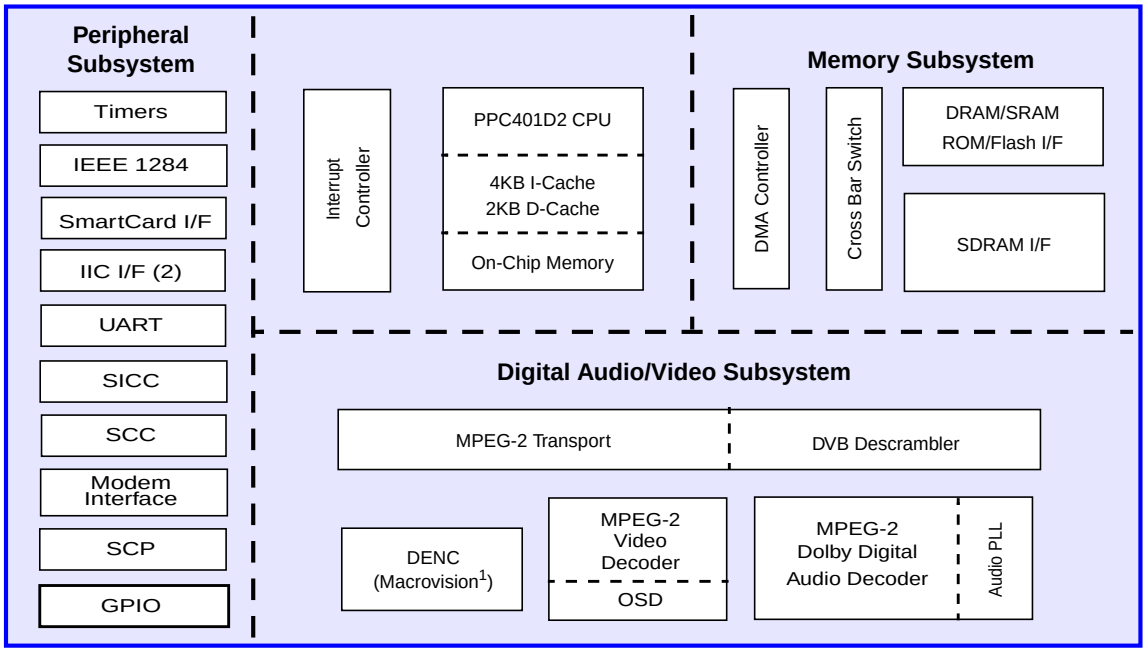


Figure 1-1. STB010x0 Block Diagram

1. Macrovision license required.

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Chapter 2. Processor Subsystem

The PowerPC 401D2 (PPC401D2) subsystem handles all system initialization and control, as well as provides power and flexibility for product differentiation.

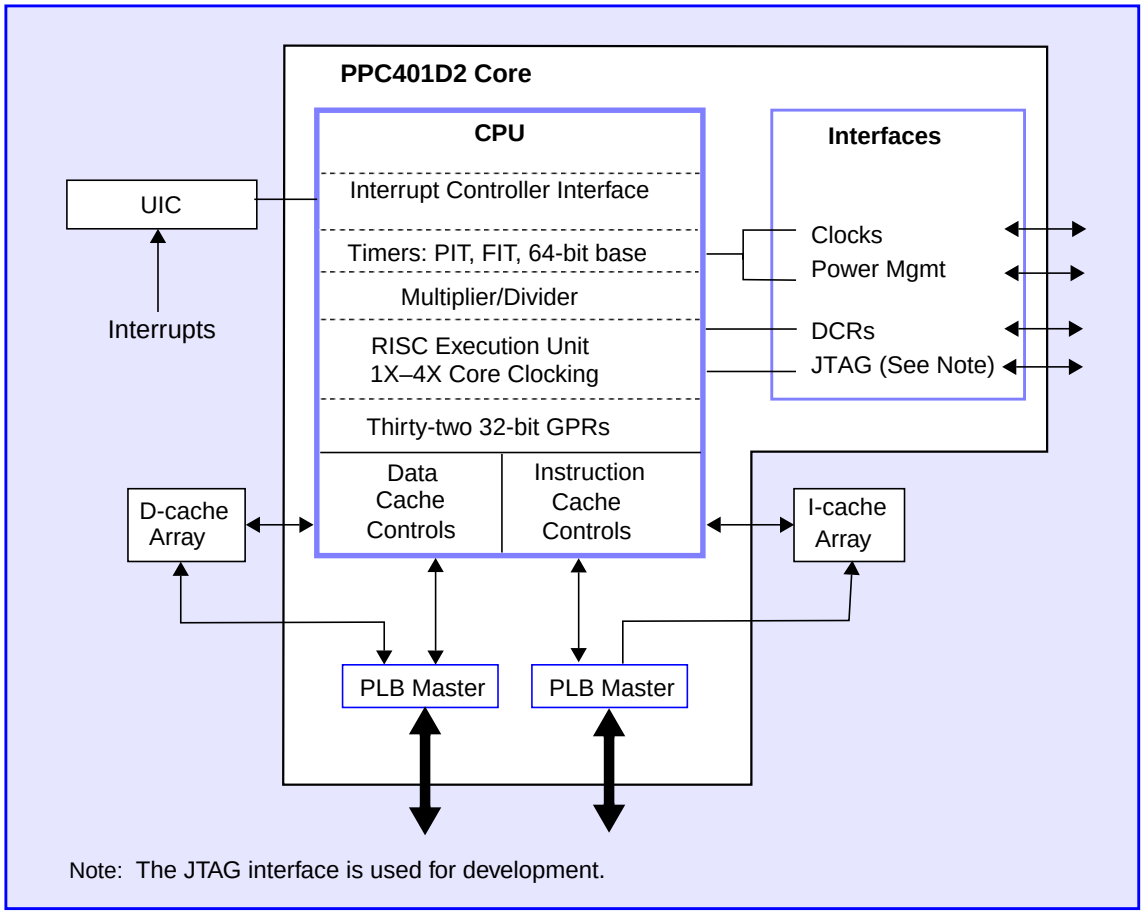


Figure 2-1. PPC401D2 Subsystem

2.1 PowerPC 401D2 CPU

2.1.1 Overview

The PPC401D2 CPU provides high performance and low power consumption. The PPC401D2 RISC CPU executes at sustained speeds of approximately one cycle per instruction. On-chip instruction and data cache arrays reduce chip count and design complexity in systems and improve system throughput.

2.1.2 Features

- Compatible with PowerPC User Instruction Set Architecture
- 50MHz (49.5MHz) performance
- 32-bit x 32 general purpose registers

- Multiply and divide instructions are performed in hardware, and are not emulated in software
- Branch prediction execution for most instructions
- 52 MIPS total bandwidth, with 45 available MIPS for OS and applications
- Addressing for up to 40MB Flash memory, 128MB DRAM and MMIO
- Interrupt latency is three cycles best time for critical interrupts
- Separate two-way set-associative 4KB instruction cache and 2KB write-back/write-through data cache

2.2 PPC401D2 Code Decompression

2.2.1 Overview

The PowerPC Embedded Architecture uses a 32-bit fixed-length instruction set. A separate supplied program compresses PowerPC instructions into variable length instructions, reducing code image size by as much as 40 percent. Program code is compressed after compilation and stored in memory to be decompressed *on the fly* by this decompression hardware.

The decompression circuitry, connected between the Processor Local Bus (PLB) and External Bus Interface Unit (EBIU), intercepts memory accesses to the compressed code area and converts the compressed instructions into 32-bit fixed-length instructions before presenting them to the PPC401D2 core via the PLB. Areas of memory which are not compressed pass through the decompression hardware without incurring any additional latency.

2.2.2 Features

- PowerPC code size reduction up to 40 percent
- Decompression core is transparent to PLB and EBIU
- Accesses to non-compressed memory areas
- Loadable SRAMs provide programmable compression algorithm coefficients for application specific tuning of compression

2.3 Universal Interrupt Controller

2.3.1 Overview

The Universal Interrupt Controller (UIC) provides all the necessary control, status, and communication necessary between all the various sources of interrupts and the PowerPC microprocessor.

The UIC supports 30 interrupts. All interrupts can be programmed to generate either a critical or a non-critical output.

There is an optional read-only vector that can be used to reduce critical interrupt servicing latency. This vector is generated by adding together an offset (based on the bit position of the highest priority, enabled, active, critical interrupt relative to the highest priority interrupt) and a vector base address register.

A configurable priority control bit determines whether the least significant or most significant bit in the status register has the highest priority. Proper ordering of the interrupt bits in the Status register is critical to making the interrupt vector generation beneficial to the programmer.

2.3.2 Features

- Combines 21 internal STB010x0 interrupts along with 9 external interrupts and presents them to the CPU's critical or non-critical inputs
- External Interrupts 0:4 can be edge- or level-sensitive. External interrupts 5:8 are level-sensitive.
- Interrupt Polarity is programmable
- Programmable critical/non-critical interrupt selection for each interrupt bit

2.4 On-Chip Memory

2.4.1 Overview

The 4KB On-Chip Memory (OCM) unit is connected to the Data Control Register (DCR) bus and to the OCM interface of the PPC401D2 Processor. The OCM provides access to a high-speed, low-latency memory without using up valuable cache space. It can hold either instructions, data, or both.

2.4.2 Features

- Direct interface to the PPC401D2 CPU I-side OCM read-only interface
- Direct interface to the PPC401D2 CPU D-side OCM read/write interface
- Single-cycle access to I-side OCM
- Two-cycle access to D-side OCM

2.5 CPU Trace Support

2.5.1 Features

Trace allows the following operations:

- Forward trace allows the user to specify the number of cycles after trigger event has occurred. Number of cycles to trace forward is set in the RISCWatch™ debug tool.
- Backtrace capability allows the user to specify the number of cycles before the trigger event has occurred. Number of cycles to trace backward is set in the debug tool (IBM RISCWatch Debug tool)
- Number of cycles that the trace window specified by sum of forward and backward trace cycles *must not* exceed the maximum size of trace, which is 64 Kcycles in RISCWatch

2.6 Processor Local Bus

2.6.1 Overview

The processor local bus (PLB) is designed to interface directly with the PPC401D2 and other major functions. The primary goal of the PLB is to provide a standard interface between functions requiring direct memory access and the integrated bus controllers. STB010x0 uses two processor local buses (PLBs) to provide high bandwidth between the various cores and the two external memory interfaces. The STB010x0 PLB Architecture includes a cross-bar switch to present both memory interfaces as a flat, shared memory space.

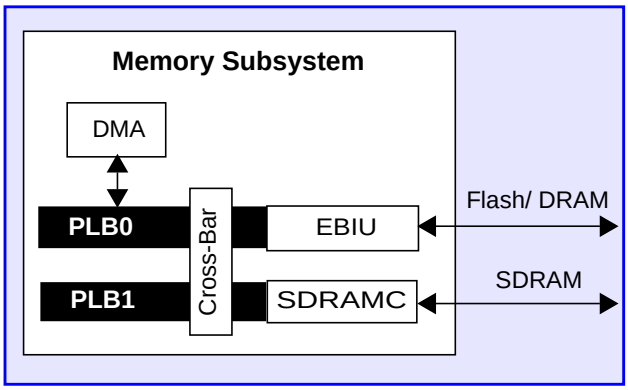
2.7 Clock and Power Management

2.7.1 Overview

For power-saving purposes, there is a Clock and Power Management (CPM) input , which is used to shut down each unit's clocks. One cycle after being activated, the clocks to the internal registers stop oscillating and the state of the registers is frozen until the CPM input is deactivated and the clocks begin to oscillate again.

Chapter 3. Memory I/F Subsystem

The memory interface subsystem provides the system memory controller interface for the DRAM, SRAM, FLASH Memory, ROM, as well as the SDRAMC (also known as the High Speed Memory Controller [HSMC]) interface for synchronous DRAM. It also provides the DMA interfaces for these memories. A key advantage built into the memory interface is its ability to have concurrent access (one function to SDRAM; one function to DRAM) and mutual access (given function can get to either port).



3.1 Direct Memory Access Controller

The Direct Memory Access (DMA) controller is a processor local bus master that allows faster data transfer between memory and peripherals than that which is possible under program control. The use of DMA controller enables the PPC401D2 processor to be free to execute instructions, with no contention for the bus if the PPC401D2 is executing from cache. DMA is useful when the overhead associated with the DMA controller setup is minimal when compared to the time it would take to move the data using load and store instructions executed under program control.

3.1.1 Overview

The four-channel DMA controller handles data transfers between memory and peripherals and memory to memory. Each channel has an independent set of registers needed for data transfer. It contains a control register, a source address register, a destination address register, and a transfer count register. Each channel also supports chained DMA operations; therefore, it contains a chained count register, and its source address register functions as the chained address register. All DMA channels report their status to the DMA execution unit.

The DMA unit supports the following transfers:

- Fly-by transfers to external peripherals
- Fly-by burst transfers to external peripherals
- Memory-to-memory transfers
- Buffered peripheral to memory transfers
- Buffered memory to peripheral transfers

3.1.2 Features

- Four DMA channels can each, independently and concurrently, support any one of the following:

  - 2 external DMA channels
  - 10 internal STB010x0 DMA channels that are used by features such as the 1284, Smart Card, SICC, and 16550 UART
- Chained operation for back-to-back DMA on the same channel
- 16- and 32-bit peripheral support (on-chip peripheral bus and external)
- 32-bit addressing
- Address increment or decrement
- Internal data buffering capability
- Data chaining
- Support for memory mapped peripherals

3.2 External Bus Interface Unit

3.2.1 Overview

The external bus interface unit (EBIU) expands the local bus to transfer data between the PLB and memory or peripheral devices attached to the external bus. It provides direct processor bus attachments for most memory and peripheral devices. The EBIU controls up to 8 banks or regions of memory or devices, one of which must use SRAM/ROM style controls, and two of which can be either SRAM/ROM or DRAM memories. There is also a separate interface for device control registers (DCRs) that enables the PPC401D2 processor CPU to read and write internal registers specific to the EBIU in order to program the attributes of each of the 8 banks.

3.2.2 Features

- Easily connects a wide range of memory and peripheral devices
- Low latency design for high system performance
- Direct connect DRAM interface:
  - Up to four DRAM banks with programmable address select;
  - Extended data output (EDO) and fast page mode (FPM) support;
  - Early RAS mode (ERM) for timing flexibility;
  - Programmable refresh rates for automatic CAS before RAS refresh;
  - Software initiated and self refresh modes supported for power savings;
  - Extended refresh cycle to support slower DRAM parts at high SysClk frequencies.
- Direct connect SRAM / ROM / PIA interface:
  - Up to five SRAM / ROM / PIA banks with programmable address select;
  - Programmable or device paced wait states;
  - Burst mode (BME) and single cycle transfers.
- 16-, 32-bit byte addressable bus width support.
- Programmable target word first or sequential cache line fills.
- Support for fully pipelined single cycle read and write.

- PLB bus interface - supports the processor local bus specifications:
  - Support for 4 masters on PLB_B0 (data bus 0) and 2 masters on PLB_B1 (data bus 1);
  - Supports all applicable PLB transfer types including burst and DMA types;
  - PLB cycles can be bus locked or ordered;
  - Line requests of four, eight and sixteen words. For line reads and writes, the data is transferred in word sizes. EBIU handles packing and unpacking to halfword and byte devices.
  - Does not utilize optional address pipelining features of the processor local bus specifications.
- DVB-CI support.
- Configurability of DCR addresses and base addresses of SRAM / DRAM regions.
- External bus master support
- Common bank-specific programmability
- Supports up to 40MB FLASH (4 banks), and up to 2 banks DRAM (64MB/bank)
- Device Paced Ready input
-

3.3 SDRAM Controller

3.3.1 Overview

The SDRAM Controller (SDRAMC) (also known as High Speed Memory Controller [HSMC]) transfers data between the PowerPC Local Bus (PLB) and SDRAM memory devices attached to the external bus. This version of the SDRAMC implements support for two (2) banks of SDRAM. There is a also a separate interface for device control registers (DCR) to allow the PPC401D2 CPU to read and write internal registers specific to the SDRAMC in order to program the attributes for each bank.

3.3.2 Features

- Direct connect SDRAM interface
  - Up to two (2) SDRAM Banks with programmable address select
  - Programmable refresh rates for automatic SDRAM Refresh
  - Software initiated and Self Refresh modes supported for power savings
- Implements address and data pipelining
- Provides high bandwidth with a narrow, 16-bit interface (200MB/s peak)
- Page interleaving
- Supports 16Mb and 64Mb SDRAMS, concurrently

3.4 Cross-Bar Switch (CBS)

3.4.1 Overview

The Unified Memory Architecture (UMA) is implemented via the PowerPC Local Bus (PLB) Cross-Bar Switch (CBS), which connects multiple PLB master buses (PLB_B0 and PLB_B1) to multiple PLB slave buses (PLB_S0 and PLB_S1), thus, allowing two sets of PLB buses to inter-communicate. The switch decodes the address on the PLB bus and directs the transfer to the slave device on PLB_S0 or PLB_S1.

This feature allows all PLB masters connected to master bus PLB_B0 to request all PLB transfer types from PLB slaves on either PLB_S0 or PLB_S1. Similarly, all PLB bus masters connected to master bus PLB_B1 request all PLB transfer types from PLB slaves on either PLB_S0 or PLB_S1. Simultaneous data transfers can occur on both PLB buses. Each PLB master bus contains a separate PLB arbiter to arbitrate the requests from the PLB masters attached to the bus.

A programmable PLB bus priority control bit is used to prioritize PLB_B0 and PLB_B1 buses when there are simultaneous data transfer requests to the same slave port.

The PLB Transfer Abort Control bit is used to abort data transfer requests in progress by the lower priority PLB bus when the higher priority PLB bus requests a transfer to the same slave port. When set, the lower priority burst transfer request is aborted.

The PLB CBS provides a DCR bus interface for access to its control registers.

3.4.2 Features

The PLB CBS has the following features:

- Zero-cycle latency access at 49.5MHz
- DCR access of programmable registers
- Programmable PLB_Bx bus priority
- Programmable PLB transfer abort
- Creates a flat memory model
- Processor, transport, and the audio and video decoders can access memory through either memory controller
- Provides additional bus bandwidth for high-performance peripherals

3.5 Chip Interconnect Control

3.5.1 Overview

Chip Interconnect Control (CIC) is used to customize several on-chip connections. It provides control for DMA signals between the DMA core and each DMA device, so that any DMA channel can be connected to any DMA device. It also provides miscellaneous chip control and video signal multiplexing.

3.5.2 Features

- Direct Memory Access Control
  - Any internal DMA request/acknowledge signal pair can be connected to any DMA channel

  - Any external DMA request/acknowledge/end of transfer/transfer complete signal set can be connected to any DMA channel
  - Asynchronous – Choice of edge or level sensitive triggering is programmable
- Select SRAM Mode Control

  Controls selection between SRAM and DVB-CI modes
- External Graphics / Video (EGV) Selection
  - Selection for pixel data to internal DENC (from video decoder or GPIO pins)
  - Selection for video decoder HSYNC and VSYNC (from internal DENC or GPIO pins)
  - Selection for video decoder pixel clock (from 27MHz clock or GPIO pin)
- Smart Card Multiplexor Control

  Provides internal multiplexing for two smart card interfaces
- Miscellaneous Chip Control
  - Control for internal DENC OSD inputs
  - Control for video only and video/OSD outputs
  - Control for SCC RTS and CTS signals (for hardware flow control)
  - Control for SCC DMA Enable logic
  - Control for Smart Card clock enable
  - Control for GPT FreqGenGate input
  - Control for Smart Card / SICC received byte signals to timer unit

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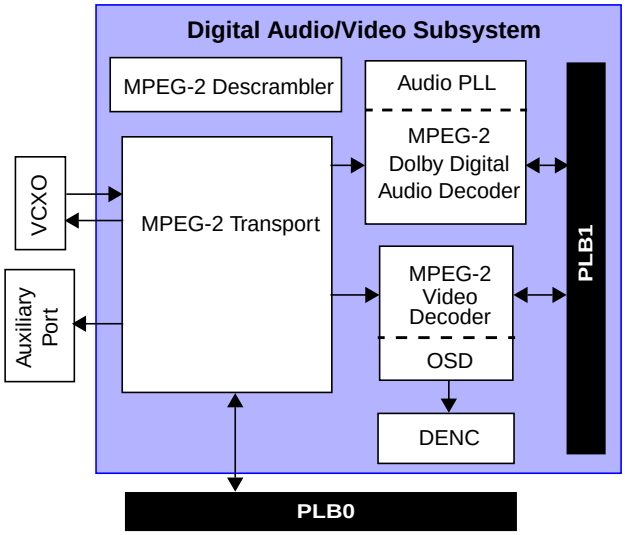
Chapter 4. Digital Audio / Video / Transport Subsystem

The MPEG-2 Digital Audio/Video subsystem provides fully-synchronized playback of digital streams carrying video and audio programs, with a minimum of interaction required from the processor



4.1 MPEG-2 Video Decoder with OSD

4.1.1 Overview

The MPEG-2 video decoder is targeted for digital video decompression applications, providing decoding and synchronized playback of video streams with a minimum of host support. The video decoder is compliant with all features of the ISO/IEC 13818-2 (also called “MPEG-2 Standard”) Main Profile/Main Level. It supports interlaced output video data and is capable of supporting MPEG-2 compressed datastreams up to an average rate of 15 Mbps. The video decoder is also backward compatible to support the ISO/IEC International Standard 11172-2 (11/93) (also called “MPEG-1 Standard”).

4.1.2 Features

The MPEG-2 video decoder has the following features:

- Provides MP@ML video playback.
- MPEG-2 MP@ML compliance with 2MBytes memory. Only 2MB of memory are needed to decode full CCIR601 resolution NTSC and PAL encoded MPEG-2 bitstreams with sustained data rates up to 15 Mbps.
- Real-time decoding of all resolutions in 16-pixel multiples up to and including 720x480x30 or 720x576x25.
- Video rates from 1.5 Mbps to 15 Mbps (up to 45 Mbps in data bursts).
- Supports European DVB standard.
- PES layer decoding of video to extract the PTS.
- Accepts PES or ES MPEG-2 streams.

- Handling of user data and other selected bit fields of the PES layer available through memory access from the PPC401D2.
- Input from transport or directly from system memory.
- Horizontal and vertical filters deliver high quality video. Chrominance filtering and up-sampling to provide CCIR601 4:2:2 video output. Pan and scan supported in 1/16 pel accuracy for 16:9 source material. These are the supported input image sizes for automatic expansion:
  - 352 x 240 (288) 4:3 in NTSC (PAL);
  - 352 x 480 (576) 4:3 in NTSC (PAL);
  - 480 x 480 (576) 4:3 in NTSC (PAL);
  - 544 x 480 (576) 4:3 in NTSC (PAL);
  - 720 x 480 (576) 16:9 pan & scan in NTSC (PAL);
  - 544 x 480 (576) 16:9 pan & scan in NTSC (PAL);
  - 480 x 480 (576) 16:9 pan & scan in NTSC (PAL);
  - 352 x 240 (288) 16:9 pan & scan in NTSC (PAL);
  - 352 x 480 (576) 16:9 pan & scan in NTSC (PAL).
- Letterbox Format Display.
- Outputs provided for video-only and for video-with-OSD.
- Can blend or multiplex graphics through embedded on-screen display (OSD).
- Output interface flexibility (programmable controls):
  - Composite blanking and Field ID signals;
  - V-sync and H-sync signals;
  - V-ref and H-ref signals;
  - CCIR656 slave mode;
  - programmable signal polarity.
- Sophisticated error concealment including transport error support.
- 3:2 pull-down support.
- Supports closed caption data, teletext data.
- Allows insertion of data in vertical blanking interval (VBI).
- Supports decoding of still or fixed images.
- Supports display of scaled video images (1/4x, 1/2x, 2x) and two (2) graphic planes.
- Multi-Plane On-Screen Display (OSD).

The video decoder has the capability of using bitmap data in memory to be merged with or displayed in place of the motion video data. Two OSD planes (the graphics plane and the image plane) are provided for increased display flexibility.

  - Programmable Background Color.

    The background color can be defined by the user via a 16-bit YUV value.

  - Multi-region link list graphic and image plane OSD with a color table for each region.
  - There can be multiple regions defined on a screen via lists that specify the horizontal and vertical start with width and height. The user can specify color and shading per region.
  - Overlay and video blending of graphic plane.

    A 6-bit value can be defined (0 for full OSD and 1–63 for various levels of blending) for each region.

  - Video shading in graphic plane OSD area

    The intensity of the OSD can be set to any of 64 levels for luminance.

  - Animation Support.

    Through the use of two buffers and the link-list capability, the OSD will switch between buffers at a rate which can be set by the user, allowing animation of the graphics image.

  - Programmable bitmap resolution on a region-by-region basis.

    4- to 256-color CLUT or 16 million direct colors.

- Supports automated channel change and time-base change features

  OSD control output for external mux (picture-in-picture support).

- An output is available to externally mux the OSD programmed areas with a video signal from another source.
- Blending of external graphics

  The OSD can accept pixel data from an external graphic source and blend that data with the decoder video.

4.2 MPEG-2 Transport and DVB Descrambler

4.2.1 Overview

The MPEG-2 transport demultiplexor provides ISO / IEC 13818-1 MPEG-2 transport system layer demultiplexing and includes an integrated DVB descrambler which may be turned off for non-DVB applications.

- Compliant with Digital Video Broadcasting (DVB) system layer requirements
- 100-Mbps (parallel) or 60-Mbps (serial) peak input rate.
- 88-Mbps (parallel) or 60-Mbps (serial) peak input rate with optional descrambler.
- Packet Identifier (PID) filtering based on 32 programmable entries.
- Detection and notification of errors and lost packets.
- Hardware based clock recovery on Program Clock References (PCRs) to reduce processor load:
  - Calculation of clock difference between PCR and System Time Clock (STC);
  - Modulated output to drive an external VCXO;
  - Optional internal clock recovery algorithm based on clock difference.

- Internal DVB descrambler including filtering and storage of eight control word pairs (optional).
- Auxiliary output port for real-time data transfers (optional):
  - 2-bit mode at the system clock speed;
  - 8-bit mode at 1X, 1/2X, 1/3X and 1/4X of the system clock speed.
- Table section filtering:
  - 64 separate 4 byte filter blocks with bit level masking;
  - Multiple filters can be linked to extend filtering depth in 4-byte increments;
  - Multiple filters per PID;
  - Filters program-specific information (PSI), service information (SI), private tables;
  - Handles multiple sections per packet and sections that span packets;
  - Optional CRC checking of section data.
- Selective routing of some or all of packet data to system memory:
  - Based on 32 separate queues (one per PID);
  - Ability to route entire packets, payloads, adaptation fields, table sections (after filtering) and private data.
- Direct transfer of audio / video (PES) data to decoders.
- Simplified channel changes, time-base changes and error flagging / concealment through direct communication with decoders.
- Interface for a Transport Assist Processor to provide additional processing:
  - Extended filtering / parsing of tables, private data, adaptation fields and PES headers;
  - Ability to selectively route alternative data fields to system memory.

4.3 MPEG-2/Dolby Digital Audio Decoder

4.3.1 Overview

The Audio Decoder receives and decodes either PES (Packetized Elementary Stream) or ES (Elementary Stream) audio data. The audio compute engine consists of a generic DSP processor. It can decode either MPEG, Dolby Digital™ (AC-3), 16-, 18- or 20-bit unformatted PCM or Linear PCM (LPCM) audio data via individual software programs. Each program is downloaded to the Digital Audio Decoder by the host processor following initialization. All audio programs are provided by IBM to authorized IBM customers in object code form only. The Audio Decoder generates up to two channels of decoded PCM for MPEG, LPCM and PCM audio playback output. It can generate up to six channels of audio output for Dolby Digital.

The Dolby Digital audio capability is optionally available[1] via a separate IBM STB Processor / Decoder part number, STB01010. A Dolby Digital license must be in effect between the STB01010 purchaser and Dolby Laboratories, Inc. Additional per-chip royalities may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license may be obtained by writing to:

1. Pending certification by Dolby Laboratories.

Dolby Laboratories Inc.
Dolby Laboratories Licensing Corporation
Attn: Intellectual Property Manager
100 Potrero Avenue
San Francisco, CA 94103-4813

4.3.2 Features

- Provides two channel MPEG audio output; six channel Dolby Digital down mixed to two channels or six channels Dolby Digital output.
- Decodes Dolby Digital 5.1 channels and supports Dolby Digital which is described in the ATSC Specification for Digital Audio Compression (AC-3).
- Decodes MPEG-1 and MPEG-2 audio, Layers I and II and two channel output, two channel input including:
  - Single channel, stereo, joint stereo, and dual channel modes.
- Performs MPEG-1 audio parsing, MPEG-2 PES audio parsing and also accepts audio elementary streams.
- Supports 16-kHz, 22.05-kHz, 24-kHz, 32-kHz, 44.1-kHz and 48-kHz audio sampling frequencies:
  - 16-kHz, 22.05-kHz, and 24-kHz frequencies are derived within the Audio Decoder, from 32-kHz, 44.1-kHz and 48-kHz sampling frequencies, respectively.
- Supports audio / video synchronization through PTS / STC comparison with each audio frame.
- Linear PCM (LPCM) playback at a sampling frequency of 48-kHz and quantization sample width selections of 16, 18 or 20 bit input and 20 bit output.
- Unpacketized PCM (UPCM) playback at sampling frequencies of 16-kHz, 22.05-kHz, 24-kHz, 32-kHz, 44.1-kHz and 48-kHz along with quantization sample width selections of 16-, 18- or 20-bit input and 20-bit output.
- Supports Karaoke Mode for Dolby Digital and PCM playback.
- Supports an encoded audio bit rate up to 640 Kbps. This bit rate only pertains to encoded bitstream data.
- Audio Clip Mode for PES, ES and PCM formats with byte address granularity and 2 MBytes maximum per clip.
- Expandable rate buffer size selectable from 4K to 64K (4K increments).
- Relocatable rate buffer region using a programmable base register with 128-byte location granularity.
- Relocatable PTS Value and Ancillary data region using a programmable base register with 128-byte location granularity.
- Relocatable Audio Temporary Data and Decoded Audio Data Bank region using a programmable base register with 128-byte location granularity with additional offset register.
- Reduced memory requirement for 2 channel MPEG verses 5.1 channel Dolby Digital decoding
- 256x and 512x DAC sampling clock frequency configurations.
- Programmable stream ID register with corresponding 8-bit enable field.
- Provides two 20 bit PCM output formats:
  - I^2S;

  - Left-justified.
- Performs audio bitstream error concealment, either by frame repeats or muting, due to loss of synchronization or detection of CRC errors.
- MPEG error checking using framesize calculation for each frame.
- Provides de-emphasis pins that interface to external de-emphasis circuitry.
- Provides Dolby Surround Mode (dsurmod) pins that interface to external surround mode circuitry.
- Provides a programmable interface that supports the following:
  - Play, stop and mute;
  - Rate buffer purge to support channel and mode changes;
  - Provides a compressed buffer full indicator;
  - Synchronization enable/disable for PTS-STC comparison.
- Parses and stores ancillary data into external memory for later use by the host processor:
  - Interrupts are provided when audio ancillary data is available and when the audio ancillary data buffer is full.
- SPDIF meeting IEC958 (or Dolby Digital) specs.
- Enhanced IEC 958 S/P DIF Channel Status Bit Support by including 16 SPDIF Channel Status Bits, with host control over most of the bits. Added Copyright bit control.
- Host-controlled Validity Bit into SPDIF sub-frame via DCR register.
- Audio attenuation in 64 steps with smooth transitions between steps.
- Tone generation with up to 128 generated tones at 31 different durations with 7 levels of attenuation via processor command.
- Supports automated channel change.
- Supports automated time base change.

4.4 Audio PLL

4.4.1 Overview

The Phase Lock Loop (PLL) circuitry supplies the appropriate clock frequencies to the Audio Decoder to allow it to properly decode and play back decoded PCM audio data at the appropriate sample rate.

The supported audio output sample frequencies are 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz.

4.4.2 Features

- Generates all required audio clocks from 27MHz input
- Automatically synchronizes playback of audio data locked to the incoming stream clock reference

4.5 NTSC/PAL Digital Encoder Core with Macrovision

4.5.1 Overview

The Multi-standard Digital Video Encoder (DENC) converts digital video data into an analog NTSC or PAL signal. Macrovision™ copy protection is supported in the STB01000 / STB01010 products. A valid Macrovision license must be in effect between the STB010x0 purchaser and Macrovision Corporation. Additional per-chip royalties may be required and are to be paid by the purchaser to Macrovision Corporation.

Macrovision Corporation
1341 Orleans Avenue
Sunnyvale, CA 94089

4.5.2 Features

- Converts digital video to NTSC/PAL-compliant analog output
- Provides up to five concurrent analog video outputs, including S-Video, composite video, YPbPr, and RGB; compatible with SCART connectors
- Supports Macrovision Copy Protection[1] Revision 7[2]
- Analog outputs of the NTSC/PAL encoder are driven by 10-bit D/A converters, operating at 27 MHz. The outputs drive standard video levels into 75-Ω loads.
- Supports closed caption, teletext insertion
- 8-color, on-screen display
- Line 23 WSS (Wide-screen Signaling) support per ITU-R BT.1119
- Switchable pedestal with gain compensation
- Allows synchronized playback of video data locked to the incoming stream clock reference

4.6 Additional Interfaces

4.6.1 External Graphics and Video (EGV) Port

The EGV port provides flexibility for interfacing external graphics and video components. Many of the signals are bi-directional.

When the EGV is used as an output, the signals may be routed to an external graphics chip or DENC. When used as an input, either the internal OSD graphics can be replaced with data from an external graphics chip or external digital video (from an analog signal converted to digital via DSMD for example) could replace the internally decoded MPEG video. In the later case, the external digital video can be merged/blended with the internal OSD graphics.

The EGV port is activated using the GPIO.

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1. This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited.
2. This feature is available only to Macrovision licensees.

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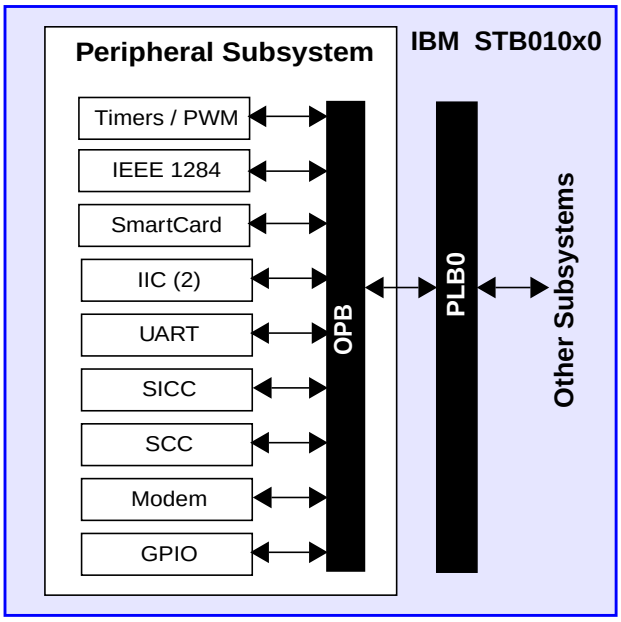
Chapter 5. Peripheral Subsystem

There are 10 peripheral subsystem interfaces on the chip.



5.1 General Purpose Timer

5.1.1 Overview

The General Purpose Timer (GPT) is an On-chip Peripheral Bus (OPB) function that provides a separate time base counter and additional system timers beyond those defined in the PPC401D2. Up to 3 capture timers and 3 compare timers can be implemented per GPT unit.

5.1.2 Inter-Character (IC) Timers

Three Inter-Character (IC) time-out timers are also implemented in this functional unit. These timers receive the count signal inputs from other units they are timing. Each timer is an 10-bit down counter that is loaded with a programmable value (TOUT) upon the active edge of the count signal input. Once loaded the IC timer counts down TOUT number of TCLK cycles until it reaches 0 (that is, the IC timer has expired). When a timer expires, it sets its corresponding bit in the IC interrupt status register.

5.1.3 Features

- A separate time base inside this unit, distinct from the one within the PPC401D2
- Up to three capture event timers with unique inputs
- Separately configurable and programmable synchronization and edge detection
- Up to three compare timers with unique outputs
- Separately configurable and programmable synchronization and output levels
- Two reset inputs; one for the entire GPT unit; one just for the time base

5.2 Pulse Width Modulation

5.2.1 Overview

The Pulse Width Modulation (PWM) function produces two square wave outputs with a variable duty cycle under program control. The duty cycle varies from 100 percent to 0 percent in steps of 1/256. There is a control register with two bits for each PWM. This register will control if the PWM is active or not, and what its inactive output level should be. When the PWM control register is set to disable a PWM, the 8-bit period counter will be inactive to minimize power.

5.2.2 Operation

The pulse width modulation portion of this unit contains two identical blocks, each containing an 8-Bit programmable and reloadable down counter and control logic. A timebase generator that is a free-running counter (TCLK based) generates the frequency of the pulse-width modulated output.

5.3 IEEE 1284 Host/Peripheral Interface

5.3.1 Overview

The Host/Peripheral Parallel Port Unit (PPU)is implemented as either the host side or peripheral side of the parallel port data bus to be used as an on-chip peripheral bus (OPB) slave device. The PPU will be connected to the OPB to allow independent data transfers from other OPB masters. The PPU's bidirectional parallel port interface supports IEEE Std. 1284 extended capability port (ECP)[1], byte[2], nibble[3], and compatibility[4] modes of operation. The PPU also helps monitor the IEEE Std. 1284 negotiation mode events, which allows the host to determine what the capabilities of the attached peripheral are and to set the interface into one of the other modes. The PPU does not support EPP mode.

5.3.2 Features

- Two channels of DMA for transmit and receive
- Inter-Character Timeout Facility support with the GPT/PWM
- Allows independent data transfers from other peripherals
- Supports IEEE Standard 1284 ECP, byte, nibble, and compatibility modes of operation
- Compatible with existing parallel port hosts
- Helps monitor the IEEE 1284 Negotiation mode events

5.4 Inter-Integrated Circuit (IIC) Interface

5.4.1 Overview

Two IIC interfaces are provided in this chip. The IIC provides a simple to use, highly programmable interface between the On-chip Peripheral Bus, or OPB, and the industry standard IIC serial bus. Two

1. ECP refers to the extended capability port. An asynchronous, byte-wide, bidirectional channel.
2. Byte refers to an asynchronous, reverse (peripheral-to-host) channel, under the control of the host.
3. Nibble refers to an asynchronous, reverse (peripheral-to-host) channel, under the control of the host.
4. Compatibility refers to an asynchronous, byte-wide forward (host-to-peripheral) channel.

unique IIC units are used to provide two independent IIC interfaces. The IIC can be programmed to operate as a master, as a slave, or as both a master and a slave on the IIC interface. The unit's logic manages the IIC bus, freeing the OPB interface for other time-critical operations. In addition to sophisticated IIC bus protocol management, the IIC provides full data buffering between the OPB and the IIC bus.

5.4.2 Features

- Compliant with Phillips Semiconductors I^2C Specification, dated 1995
- 100 and 400kHz operation
- 8-bit data transfers
- 7-bit and 10-bit address decode/generation
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{dd} IIC interface
- Two independent 4 x 1-byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Class 3 clock power management

5.5 Smart Card Interface

5.5.1 Overview

The purpose of the Smart Card Interface (SCI) is to handle the communications between an Integrated Circuit Card (ICC) and an appropriate processing unit (host CPU). This interface device (SCI) is a hardware construction with its control structure developed in software dut to the many types of protocols and communication possibilities. This interface is designed for use with asynchronous transmissions.With some minimal external multiplexing glue logic, communication with multiple ICCs can be accomplished via timesharing the SCI.

5.5.2 Features

- Compatibility with ISO/IEC 7816-3
- Support for T0 and T1 protocols
- Hardware error checking
- 8-bit memory mapped registers
- Supports two-channel Direct Memory Access (DMA).
- Inter-Character Timeout Facility support with the GPT/PWM

5.6 Serial Communication Controller

5.6.1 Overview

The Serial Communication Controller (SCC) is a universal asynchronous receiver/transmitter (UART) with FIFOs, and is compatible with the 16550 part numbers manufactured by National Semiconductor (NS) Corporation.

5.6.2 Features

- Compatible with National Semiconductor 16550 UART family
- Compatible with National Semiconductor 16450 (non-FIFO version)
- Complete status reporting capability
- Support for two DMA channels ˚
- 16-byte FIFO for receive path
- 16-byte FIFO for transmit path
- Programmable baud rate generator
- Internal loopback for diagnostics
- Fully programmable serial interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1-, 1.5-, or 2-stop-bit generation
  - Variable Baud rate
- Modem control functions
- Inter-Character Timeout Facility support with the GPT/PWM

5.7 Serial and Infrared Communication Controller

5.7.1 Overview

The Serial and Infrared Communication Controller (SICC) is functionally identical to the 403 Serial Port Unit (SPU). The SICC can be put into an alternate mode (IrDA mode) to allow transfer and reception of infrared characters. IrDA transmissions are bounded by the Infrared Data Association (IrDA) Specification 1.1.

The SICC is capable of both asynchronous reception or transmission of data characters at various programmable baud rates and can run at IrDA speeds of up to 1.152 Mbps. The SICC provides a programmable baud rate generator that is capable of dividing the processor clock speed by 0 to (2^{12} -1), thus producing the 16 X clock for normal SPU and low-speed IrDA operations, and the 4 X clock for high-speed IrDA operations. It provides features typically found on advanced serial communications controllers, including DMA peripheral support, internal loopback mode, automatic echo mode, automatic handshaking capability on both receive and transmit operations, low and high speed IrDA operation, and bit stuffing/unstuffing on transmission/reception of characters. The CPU can read the complete status of the SICC at any time during functional operation. Status information includes the type and condition of the transfer operation being performed by the SICC as well as any error conditions that occurred (parity, overrun, framing, break interrupt, handshaking line loss, or an aborted frame in IrDA mode). The SICC

offers a 4 bytes FIFO which can be programmed via byte, halfword or word instructions. This FIFO is available for normal UART operation and Ir operation.

5.7.2 Features

- Supports RS-232 and infrared communications
- Automatic insertion/removal of standard ASYNC communication bits
- Programmable baud rate generator
- Individual enable for receiver and transmitter interrupts
- Internal loopback and auto-echo modes
- Full-duplex operation
- Programmable serial interface
- Status reporting capability
- Individual receiver and transmitter DMA support
- Auto-handshaking mode for receiver and transmitter
- Transmitter pattern generation capability
- Serial clock frequency up to one half system clock frequency
- Inter-Character Timeout Facility support with the GPT/PWM

5.8 Modem Codec Interface

5.8.1 Overview

The Modem Codec Interface provides a glueless communication from the chip to/from many standard and economical telephony codecs. Utilization of the PPC401D2 CPU and licensed software for a software modem can be used to implement an inexpensive solution for a modem. To insure the required data throughput, two DMA channels are supported (one receive and one transmit). The external interface supports the industry standard 4-wire interface consisting of the following:

- Transmit data
- Receive data
- Clock
- Frame sync

5.8.2 Features

- Glueless interface to industry standard telephony codecs such as the following:
- Two channels of DMA support off-loading CPU for data movement
- Status reporting and interrupt generation

5.9 Serial Control Port

5.9.1 Overview

The SCP is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other SCP bus-compatible serial devices. The SCP is a slave device to the OPB bus, and supports a three-wire interface to the serial port (receive, transmit, and clock)

5.9.2 Features

- Provides glueless serial interface to many microcontrollers
- Three-wire interface
- Full-duplex serial data communication
- OPB bus slave and SCP bus master
- Programmable clock rate divider (Sysclk/4 to Sysclk/1024)
- Clock inversion
- Reverse data.
- Local data loopback for test
- Bit rate supported up to 1/4 the frequency of the System Clock

5.10 General Purpose I/O Controller

5.10.1 Overview

The GPIO Controller is an On-Chip Peripheral Bus (OPB) unit that enables multiplexing of module I/Os with many different functions. It can significantly reduce the quantity of module I/Os required.

5.10.2 Features

- Enables multiplexing of module I/Os with many different functions
- Programmable open-drain output conversion
- Registered input and output functions