

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

The **DK** Series of non-isolated dc-dc converters provide high efficiency, cost effective, and complete Point-of-Load power solutions in very small and low profile SMD packages. Occupying a footprint of less than 2 cm² (0.3 in²), these are the converters of choice for a wide range of telecommunications, data communications, computing, industrial and consumer applications where board space, cost, height, efficiency, and reliable operation in elevated temperature environments are critical.

非絶縁型DC/DCコンバータの**DK**シリーズは、高効率、低価格、小型・低背のSMDパッケージで完全なPOL電源ソリューションを提供します。実装面積が2cm² (0.3 in²)以下のこのコンバータは、基板スペース、費用、高さ、効率、及び高温環境での信頼性のある動作が重要な広範囲の電気通信、データ通信、コンピュータ、産業及びコンシューマ向けのアプリケーションに最適です。

The **FPDK12SR8003PSS** converter of the **DK** Series operates from a 5.6Vdc to 14.0Vdc input, and delivers 3A of output current at a tightly regulated programmable output voltage of 0.8Vdc to 6.6Vdc. The thermal performance of the **FPDK12SR8003PSS** is best-in-class: No derating is needed up to 85°C, under natural convection.

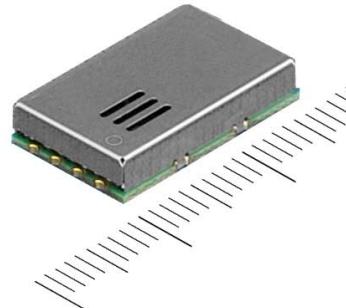
DKシリーズのFPDK12SR8003PSSは5.6V～14.0V入力で動作し、高い電圧精度でプログラム可能な出力電圧0.8V～6.6Vdcで、3Aの出力電流を供給します。FPDK12SR8003PSSの温度特性はクラス最高レベルです。自然対流で85°Cまで出力電流デリーティングを必要としません。

The leading edge performance of the **DK** Series products, and their extremely high quality and reliability are achieved through advanced circuit and thermal design techniques and FDK's state of the art in-house manufacturing processes and systems.

DKシリーズ製品の最先端の特性と非常に高い品質及び信頼性は、高度な回路設計及び温度設計技術とFDKの最先端の自社製造プロセス及びシステムによりもたらされます。

Applications

- Telecommunications
 - Routers, Base Stations, Wireless
テレコムシステム（ルータ、基地局、無線）
- Data Communications
 - Internet Routers, Processors
データ通信（インターネットルータ、プロセッサ）
- Computing
 - Servers, Workstations
コンピュータ関係（サーバー、ワークステーション）
- Industrial and Consumer
 - Navigation, POS systems, Office Equipment
- Entertainment
産業及びコンシューマ向け
(ナビゲーション、POSシステム、オフィス機器、エンターテインメント)



FPDK12SR8003PSS

Features

- RoHS compliant
RoHS準拠
- Delivers up to 3A (19.8W)
3A (19.8W)まで供給可能
- High efficiency, no heatsink required
高効率-放熱器が不要
- No derating up to 85°C
85°Cまでデリーティング不要
- Small size and low profile: 0.657" x 0.402" x 0.134"
小型、低背 (16.7 x 10.2 x 3.4mm)
- Programmable output voltage via external resistor
外部接続の抵抗によりプログラム可能な出力電圧
- No minimum load required
最小負荷は不要
- Start up into pre-biased output
出力にプリバイアスがあつても起動可能
- Remote ON/OFF
リモートON/OFF機能
- Output voltage tracking function
出力電圧トラッキング機能
- Auto-reset output over-current protection
過電流保護機能: 自動復帰
- Auto-reset output over-temperature protection
内部過熱保護機能
- Power Good Signal
パワーグッド信号出力
- High reliability, MTBF = 1 Million Hours
高信頼性: MTBF = 1 Million Hours
- UL60950 recognition in U.S. & Canada, and CB Scheme certification per IEC/EN60950 (pending)
UL60950、CB Scheme（準拠）
- All materials meet UL94, V-0 flammability rating
全ての部品は UL94 V-0に適合

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet**Electrical Specifications 電気的仕様**

All specifications apply over specified input voltage, output load, and temperature range, unless otherwise noted.

注記が無い場合、全ての仕様は指定された入力電圧、負荷、温度範囲で適用されます。

Conditions: $T_a=25\text{degC}$, Airflow=50LFM (0.25m/s), $V_{in}=12\text{Vdc}$, unless otherwise specified.

| PARAMETER | NOTES | MIN | TYP | MAX | UNITS |
|---|---|------|------------|--------------|-------------|
| ABSOLUTE MAXIMUM RATINGS¹ | | | | | |
| Input Voltage | Continuous | -0.3 | | 16 | Vdc |
| Operating Temperature | See page 9 | -40 | | 85 | °C |
| Storage Temperature | | -55 | | 125 | °C |
| Output Voltage | | 0.8 | | 6.6 | Vdc |
| Power Good Voltage | | -0.3 | | 5.0 | Vdc |
| Power Good Sink Current | | | | 5.0 | mA |
| Track Pin Voltage | For non-sequenced operation | 0.85 | | 5.0 | Vdc |
| FEATURE CHARACTERISTICS | | | | | |
| Switching Frequency | | | 600 | | kHz |
| Output Voltage Programming Range | See page6. Output Voltage Adjust | 0.8 | | 6.6 | Vdc |
| Turn-On Delay Time | Full resistive load | | | | |
| with V_{in} (module enabled, then V_{in} applied) | From $V_{in}=V_{in}(\text{min})$ to $0.1*V_{out}(\text{nom})$ | | 3.0 | | ms |
| with Enable (V_{in} applied, then enabled) | From enable to $0.1*V_{out}(\text{nom})$ | | 3.0 | | ms |
| Rise Time (Full resistive load) | From $0.1*V_{out}(\text{nom})$ to $0.9*V_{out}(\text{nom})$ | | 3.0 | | ms |
| Remote Control (Positive Logic) | | | | | |
| Module Off | | -5 | | $V_{in}-2.7$ | Vdc |
| Module On | | | $V_{in}-1$ | V_{in} | Vdc |
| Power Good | Set point for power good output high | 82 | 88 | 93 | % V_{out} |
| Power Good Output Low | $I_{PGOOD}=5\text{mA}$ | | | 0.5 | V |
| Power Good Leakage Current | | | | 10 | uA |
| Tracking Delay Time | Delay from $V_{in,\text{MIN}}$ to application of tracking voltage | 10 | | | ms |

¹Absolute Maximum Ratings 絶対最大定格

Stresses in excess of the absolute maximum ratings may lead to degradation in performance and reliability of the converter and may result in permanent damage.

絶対最大定格を超えたストレスは、性能の低下、信頼性の低下、及びモジュールの破損を引き起こすことがあります。

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data SheetConditions: $T_a=25\text{degC}$, Airflow=50LFM (0.25m/s), $V_{in}=12\text{Vdc}$, unless otherwise specified.

| PARAMETER | NOTES | MIN | TYP | MAX | UNITS |
|--|---|-----|-----|-----|-------|
| INPUT CHARACTERISTICS | | | | | |
| Operating Input Voltage Range | $V_{out} \leq 3.63\text{Vdc}$ | 5.6 | 12 | 14 | Vdc |
| | $3.63\text{Vdc} < V_{out} \leq 5.5\text{Vdc}$ | 8 | 12 | 14 | Vdc |
| | $5.5\text{Vdc} < V_{out}$ | 10 | 12 | 14 | Vdc |
| Input Under Voltage Lockout | | | | | |
| Turn-On Threshold | | 4.0 | 4.5 | 5.2 | Vdc |
| Turn-Off Threshold | | 3.7 | 4.2 | 4.4 | Vdc |
| Maximum Input Current | 3Aout at V_{in} -min | | | | |
| | $V_{out}=6.6\text{V}$ | | | 2.2 | Adc |
| | $V_{out}=6.0\text{V}$ | | | 2.0 | Adc |
| | $V_{out}=5.0\text{V}$ | | | 2.1 | Adc |
| | $V_{out}=3.3\text{V}$ | | | 2.0 | Adc |
| | $V_{out}=2.5\text{V}$ | | | 1.6 | Adc |
| | $V_{out}=1.8\text{V}$ | | | 1.2 | Adc |
| | $V_{out}=1.5\text{V}$ | | | 1.0 | Adc |
| | $V_{out}=1.2\text{V}$ | | | 0.9 | Adc |
| | $V_{out}=1.0\text{V}$ | | | 0.8 | Adc |
| | $V_{out}=0.8\text{V}$ | | | 0.7 | Adc |
| Input Stand-by Current (module disabled) | | | 3.5 | | mA |
| Input No Load Current | $V_{out}=6.6\text{V}$ | | 57 | | mA |
| | $V_{out}=6.0\text{V}$ | | 57 | | mA |
| | $V_{out}=5.0\text{V}$ | | 54 | | mA |
| | $V_{out}=3.3\text{V}$ | | 41 | | mA |
| | $V_{out}=2.5\text{V}$ | | 32 | | mA |
| | $V_{out}=1.8\text{V}$ | | 25 | | mA |
| | $V_{out}=1.5\text{V}$ | | 22 | | mA |
| | $V_{out}=1.2\text{V}$ | | 19 | | mA |
| | $V_{out}=1.0\text{V}$ | | 18 | | mA |
| | $V_{out}=0.8\text{V}$ | | 16 | | mA |
| Input Reflected-Ripple Current | See Fig.H for setup (BW=20MHz) | | | | |
| | $V_{out}=6.6\text{V}$ | | 20 | | mAp-p |
| | $V_{out}=6.0\text{V}$ | | 20 | | mAp-p |
| | $V_{out}=5.0\text{V}$ | | 20 | | mAp-p |
| | $V_{out}=3.3\text{V}$ | | 15 | | mAp-p |
| | $V_{out}=2.5\text{V}$ | | 15 | | mAp-p |
| | $V_{out}=1.8\text{V}$ | | 10 | | mAp-p |
| | $V_{out}=1.5\text{V}$ | | 10 | | mAp-p |
| | $V_{out}=1.2\text{V}$ | | 10 | | mAp-p |
| | $V_{out}=1.0\text{V}$ | | 10 | | mAp-p |
| | $V_{out}=0.8\text{V}$ | | 10 | | mAp-p |

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

Conditions: $T_a=25\text{degC}$, Airflow=50LFM (0.25m/s), $V_{in}=12\text{Vdc}$, unless otherwise specified.

| PARAMETER | NOTES | MIN | TYP | MAX | UNITS |
|---|---|------|---------|------|-------|
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Set Point (no load) | | -2.5 | | +2.5 | %Vout |
| Output Regulation | | | | | |
| Over Line | Full resistive load | | +/- 0.1 | | %Vout |
| Over Load | From no load to full load | | +/- 0.3 | | %Vout |
| Output Voltage Range (Over all operating input voltage, resistive load and temperature conditions until end of life) | Output Ripple is not included. | -3.0 | | +3.0 | %Vout |
| Output Ripple and Noise BW=20MHz | See Fig.G for setup (BW=20MHz) | | | | |
| | $V_{out}=6.6\text{V}$ | | 60 | 90 | mVp-p |
| | $V_{out}=6.0\text{V}$ | | 60 | 90 | mVp-p |
| | $V_{out}=5.0\text{V}$ | | 50 | 75 | mVp-p |
| | $V_{out}=3.3\text{V}$ | | 35 | 55 | mVp-p |
| | $V_{out}=2.5\text{V}$ | | 30 | 45 | mVp-p |
| | $V_{out}=1.8\text{V}$ | | 20 | 30 | mVp-p |
| | $V_{out}=1.5\text{V}$ | | 20 | 30 | mVp-p |
| | $V_{out}=1.2\text{V}$ | | 15 | 25 | mVp-p |
| | $V_{out}=1.0\text{V}$ | | 15 | 25 | mVp-p |
| | $V_{out}=0.8\text{V}$ | | 10 | 15 | mVp-p |
| External Load Capacitance | Ceramic Capacitor, $V_{out} < 5\text{Vdc}$ | 10 | | 100 | uF |
| | Ceramic Capacitor, $V_{out} \geq 5\text{Vdc}$ | 10 | | 500 | uF |
| | Min ESR > 10mΩ, $V_{out} < 5\text{Vdc}$ | | | 1000 | uF |
| | Min ESR > 10mΩ, $V_{out} \geq 5\text{Vdc}$ | | | 500 | uF |
| Output Current Range | | 0 | | 3.0 | A |
| Output Current Limit Inception (Iout) | | | 200 | | % |
| Output Short-Circuit Current | Short=10mΩ, $V_{out}=3.3\text{Vdc}$ set | | 0.5 | | Arms |
| Pre-Bias Voltage | Turn-On | | | 3.3 | Vdc |
| DYNAMIC RESPONSE | See Fig.G for setup (BW=20MHz) | | | | |
| Iout step from 1.5A to 3A with di/dt=5A/us | $V_{out}=6.6\text{Vdc}$ | | 180 | | mV |
| | $V_{out}=0.8\text{Vdc}$ | | 120 | | mV |
| Settling time (to within 10% of Vout) | $V_{out}=6.6\text{Vdc}$ | | 60 | | us |
| | $V_{out}=0.8\text{Vdc}$ | | 40 | | us |
| Iout step from 3A to 1.5A with di/dt=-5A/us | $V_{out}=6.6\text{Vdc}$ | | 180 | | mV |
| | $V_{out}=0.8\text{Vdc}$ | | 120 | | mV |
| Settling time (to within 10% of Vout) | $V_{out}=6.6\text{Vdc}$ | | 60 | | us |
| | $V_{out}=0.8\text{Vdc}$ | | 40 | | us |
| EFFICIENCY | Full load (3A) | | | | |
| | $V_{out}=6.6\text{V}$ | | 94.0 | | % |
| | $V_{out}=6.0\text{V}$ | | 93.5 | | % |
| | $V_{out}=5.0\text{V}$ | | 92.5 | | % |
| | $V_{out}=3.3\text{V}$ | | 90.5 | | % |
| | $V_{out}=2.5\text{V}$ | | 88.5 | | % |
| | $V_{out}=1.8\text{V}$ | | 86.0 | | % |
| | $V_{out}=1.5\text{V}$ | | 84.5 | | % |
| | $V_{out}=1.2\text{V}$ | | 81.5 | | % |
| | $V_{out}=1.0\text{V}$ | | 79.5 | | % |
| | $V_{out}=0.8\text{V}$ | | 76.0 | | % |

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

Operation

Input and Output Impedance

The **FPDK12SR8003PSS** converter should be connected to a DC power source using a low impedance input line. In order to counteract the possible effect of input line inductance on the stability of the converter, the use of decoupling capacitors placed in close proximity to the converter input pins is recommended. This will ensure stability of the converter and reduce input ripple voltage. Although low ESR Tantalum or other capacitors should typically be adequate, very low ESR capacitors (ceramic, over 47 μ F) are recommended to minimize input ripple voltage. The converter itself has on-board internal input capacitance of 3uF with very low ESR (ceramic).

FPDK12SR8003PSSと入力電源間に低インピーダンスで接続してください。コンバータの安定性に影響のある入力インダクタンスを抑えるため、コンバータの入力ピンの近傍にデカップリングコンデンサを付加することをお勧めします。これによりコンバータの安定動作を確実にし、入力リップル電圧を抑制します。低ESRタントラム、又はその他のコンデンサも一般的には問題ありませんが、入力リップルを最小にするためには、非常に低ESRコンデンサ(セラミックで47 μ F以上)を推奨します。コンバータ自身は入力回路に極低ESRの3uFセラミック入力コンデンサを搭載しています。

The **FPDK12SR8003PSS** is capable of stable operation with no external capacitance on the output. To minimize output ripple voltage, the use of very low ESR ceramic capacitors is recommended. These capacitors should be placed in close proximity to the load to improve transient performance and to decrease output voltage ripple.

FPDK12SR8003PSSは出力に外付けコンデンサが無い状態でも安定して動作します。出力リップルを最小にするため、極低ESRのセラミックコンデンサの接続を推奨します。過渡時の特性向上と出力リップル低減のために負荷の近傍に極低ESRセラミックコンデンサを実装することをお勧めします。

Note that the converter does not have a SENSE pin to counteract voltage drops between the output pins and the load. The impedance of the line from the converter output to the load should thus be kept as low as possible to maintain good load regulation.

このコンバータは出力端子と負荷間の電圧ドロップを補正するセンス端子を設けていません。精度の高い負荷特性を保持するために、コンバータの出力から負荷までのラインインピーダンスは可能な限り低くしてください。

REMOTE (Pin 3)

The REMOTE pin (Pin 3) can be used to turn the converter on or off remotely using a signal that is referenced to GND (Pin 2 or 7). A typical configuration for remote ON/OFF is shown in Fig. A.

リモート端子(3番ピン)はGND(2又は7番ピン)を基準としたリモート信号によりコンバータをON/OFFするのに使用できます。一般的なリモートON/OFF回路を図-Aに示します。

The **FPDK12SR8003PSS** turns on when the REMOTE pin is at logic high (open) and turns off when it is at logic low. When the REMOTE pin is left open, the converter is on. Voltage ranges for logic high/low are provided in the Electrical Specifications section.

FPDK12SR8003PSSはリモート端子が論理的にHigh (open)で動作し、論理的にLowで停止します。リモート端子が未接続 (オープン)の場合、コンバータはONします。論理的High/Lowの電圧範囲は電気的特性を参照してください。

The REMOTE pin (pin3) is internally pulled-up to Vin. An open collector (open -drain) transistor can be used to drive the REMOTE pin (pin3).

The device driving the REMOTE pin (pin3) must be capable of sinking up to 0.3mA at low logic level.

リモート端子(3番ピン)はモジュール内部でVinにピルアップされています。リモート端子(3番ピン)の操作にはオーブンコレクタ(オープンドレイン)のトランジスタが使用可能です。

リモート端子(3番ピン)を操作するデバイスにはLowレベルで0.3mAのシンク能力が必要です。

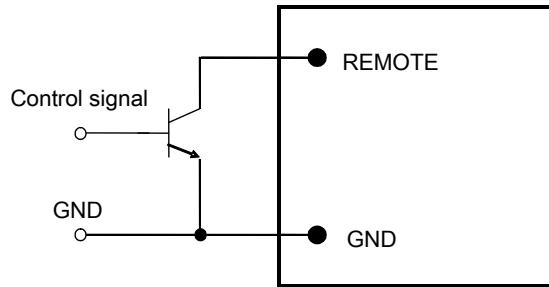


Fig. A: A typical configuration for remote ON/OFF

Power Good (Pin 6)

The Power Good Signal is an open-drain output that asserts low when Vout is out of regulation.

パワーグッド信号はオープンドレイン出力で、出力電圧が確定していない状態ではLowとなります。

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

Output Voltage Adjust/TRIM (Pin 5)

The output voltage of the **FPDK12SR8003PSS** converter can be programmed from 0.8V to 6.6V by using an external resistor

FPDK12SR8003PSSの出力電圧は外部抵抗を接続することで、0.8V～6.6Vまで可変可能です。

External Resistor

An external trim resistor, R_{TRIM} , should be connected between TRIM (pin 5) and GND (pin 2 or 7); see Fig. B. The value of R_{TRIM} , in kΩ, for a desired output voltage, V_{O-REQ} , in V, is given by:

外部抵抗 R_{TRIM} は TRIM 端子(5番ピン)と GND 端子(2又は7番ピン)の間に接続してください。図Bを参照。 R_{TRIM} の定数、及び必要な出力電圧は次の式により求めます。

$$R_{TRIM} = \frac{7}{(V_{O-REQ} - 0.8)} - 1 \quad [\text{k}\Omega]$$

Note that the tolerance of a trim resistor will affect the tolerance of the output voltage. Standard 1% or 0.5% resistors may suffice for most applications; however, a tighter tolerance can be obtained by using two resistors in series instead of one standard value resistor.

Table 1 lists calculated values of R_{TRIM} for common output voltages. For each value of R_{TRIM} , Table 1 also shows the closest available standard resistor value.

R_{TRIM} の公差は出力電圧の公差に影響します。ほとんどの使用状況においては、標準的な1%又は0.5%品の抵抗で十分です。しかしながら、より厳しい出力精度のためには、抵抗1本よりも2本を直列に使用します。Table 1に一般的な出力電圧を設定する際の抵抗値を表示します。またTable 1に標準的な抵抗を使用した場合の近似値も表示しています。

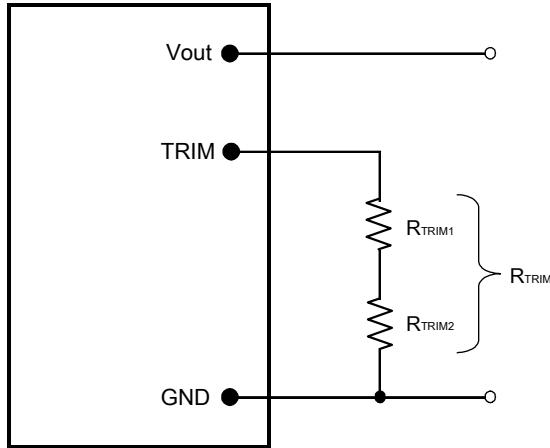


Fig.B: Configuration for programming output voltage

Table 1: Trim Resistor Value

| V_{O-REQ} [V] | R_{TRIM} [kΩ] | The Closest Standard Value [kΩ] $R_{TRIM1} + R_{TRIM2}$ |
|-----------------|-----------------|--|
| 0.8 | Open | Open |
| 1.0 | 34.000 | 34.000 + 0.000 |
| 1.2 | 16.500 | 16.500 + 0.000 |
| 1.5 | 9.000 | 7.500 + 1.500 |
| 1.8 | 6.000 | 3.000 + 3.000 |
| 2.5 | 3.118 | 3.000 + 0.120 |
| 3.3 | 1.800 | 1.800 + 0.000 |
| 5.0 | 0.667 | 0.620 + 0.047 |
| 6.0 | 0.346 | 0.330 + 0.016 |
| 6.6 | 0.207 | 0.180 + 0.027 |

Output Voltage Tracking (Pin 4)

The **FPDK12SR8003PSS** converter incorporates an output voltage tracking function that enables 2 kinds of sequenced start-up and shut-down scenarios when using multiple converters:

- Sequential
- Simultaneous

These scenarios are enabled using the external circuitry shown in Fig.D and Fig.E. If voltage tracking is not needed, the TRACK pin (pin 4) should be connected to Vin, as shown in Fig.C.

FPDK12SR8003PSSコンバータは複数のコンピュータを使用する際に、想定する2種類のシーケンス起動及び停止を可能にする出力電圧トラッキング機能を持っています。

- シーケンス
- 同時

想定されるこれらのシーケンス起動及び停止は、図D-図Eに示される外付け回路を使用することで可能となります。トラッキング機能を使用されない場合、下図のようにTRACK端子(4番ピン)をVinに接続として下さい(図C)。

A recommended value for $R1=13\text{k}\Omega$ / $R2=4.7\text{k}\Omega$.

各抵抗の推奨値は $R1=13\text{k}\Omega$ / $R2=4.7\text{k}\Omega$

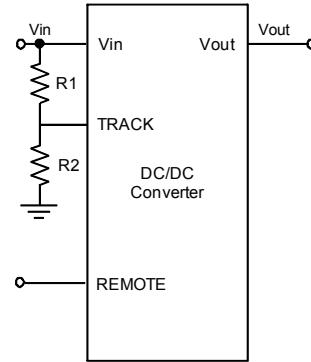


Fig. C: TRACK pin connection to Vin

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

Sequential

Sequential start-up and shut-down of converters PS1 and PS2 (Fig.D) is enabled by placing an On/Off circuit between the Vout of PS1 and the REMOTE pin (pin 3) of PS2.

コンバータPS1とPS2のシーケンス起動及び停止(図D)はオン/オフ制御回路をPS1のVoutとPS2のリモート端子(3番ピン)の間に配置することで実行されます。

A recommended value for R1=13kΩ / R2=4.7kΩ.

各抵抗の推奨値はR1=13kΩ / R2=4.7kΩ

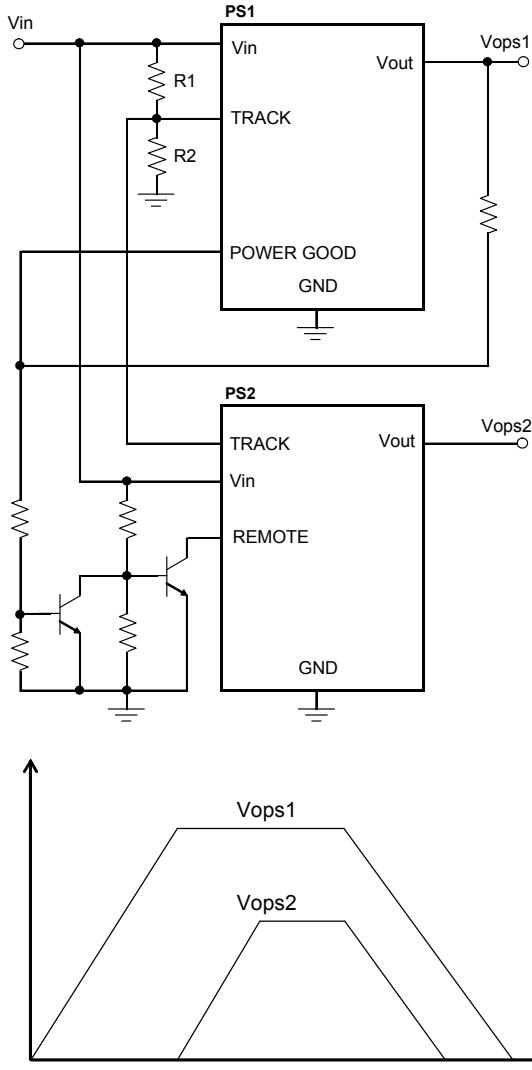


Fig. D: Sequential

For sequential start-up and shut-down, the PSV type converters of the FPDK12S Series can be used for both PS1 and PS2. In that case, R1 and R2 are not necessary.

シーケンス起動及び停止については、PS1及びPS2ともにFPDK12シリーズのPSVタイプも使用可能です。その際は、R1及びR2は不要です。

Simultaneous

Simultaneous start-up and shut-down of converters PS1 and PS2 (Fig.E), whereby the difference in output voltage between the converters during turn-on and turn-off is minimized, is enabled by connecting the Vout of PS1 to the TRACK pin (pin 4) of PS2. Note the output voltage setting of PS1 should always be higher than the output voltage setting of PS2.

電源オン及びオフ時のPS1とPS2間の出力電圧の差異を最小化する、これら2つのコンバータの同時起動及び停止は、図Eに示される様に、PS1のVoutをPS2のTRACK端子(4番ピン)に接続することで可能となります。PS1の設定電圧は常にPS2の設定電圧より高い必要があることに注意してください。

A recommended value for R1=13kΩ/ R2=4.7kΩ/ R3=10kΩ.

各抵抗の推奨値はR1=13kΩ / R2=4.7kΩ / R3=10kΩです。

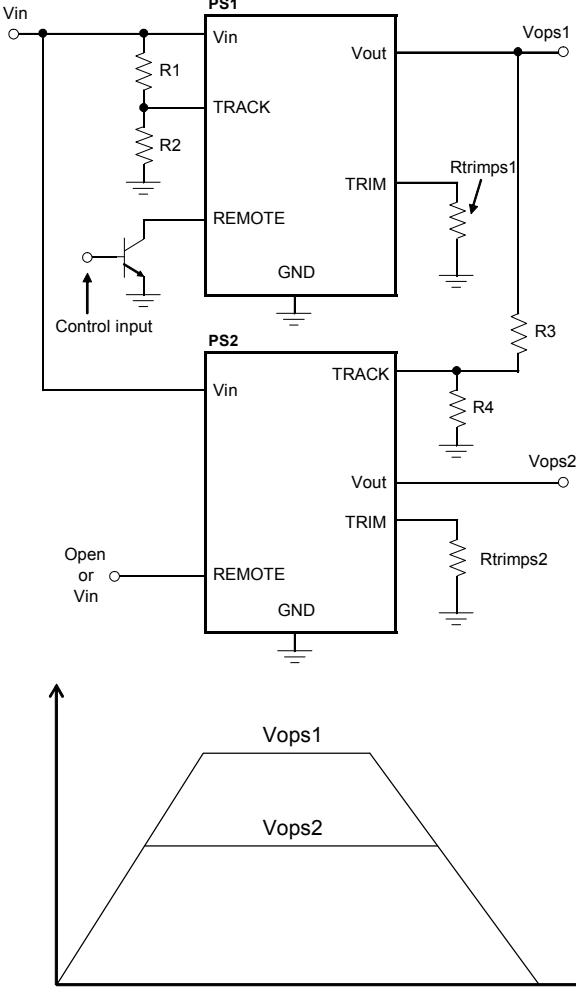


Fig. E: Simultaneous

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

The values of R4 can be determined from:

R4の値は次の方程式から求められます。

$$R4 = \frac{70 \times (1 + R_{trimps}^2)}{71 + R_{trimps}^2} \text{ [k}\Omega\text{]}$$

However, a recommended value of R4 is 70kΩ for Vo=0.8V of PS2.

但し、PS2がVo=0.8Vの場合は、R4の値は70kΩを推奨します。

The PSV Type of the FPDK12 series can be used for PS1. In that case, R1 and R2 are unnecessary.

PS1にはFPDK12シリーズのPSVタイプも使用可能です。その際は、R1及びR2は不要です。

Notes :

- (a) For simultaneous start-up and shut-down, the REMOTE pin (pin 3) of PS2 should be in the ON state before applying input voltage to PS1 and PS2. (The REMOTE pin of PS2 should be tied to Vin or left open.)

同時に起動及び停止の場合、PS1とPS2に入力電圧を印加する前にPS2のリモート端子(3番ピン)はON状態にして下さい。(リモート端子をVinに接続、または未接続。)

- (b) For proper voltage tracking, the TRACK pin (pin 4) voltage should stay at 0V for 10ms or more after the input voltage reaches Vin-MIN. This time period allows for the initialization of soft-start.

適切な電圧トラッキングにおいては、TRACK端子(4番ピン)の電位は入力電圧がVin-MINに達してから10ms以上の間、0Vのままの状態を保持しておく必要があります。この時間は、ソフトスタートの初期化のためです。

- (c) Please do not impress the voltage to TRACK pin (4 pin) with the input voltage not impressed.

入力電圧を印加していない状態で、TRACK端子(4番ピン)に電圧を印加しないでください。

Protection Features

Input Under-Voltage Lockout

From a turned-on state, the converter will turn off automatically when the input voltage drops below typically 4.2V. It will then turn on automatically when the input voltage reaches typically 4.5V.

動作している状態で入力電圧がTYPで4.2V未満になると、このコンバータは自動的に停止します。また、入力電圧がTYPで4.5V以上になると、このコンバータは自動的に動作を開始します。

Output Over-Current Protection (OCP)

The converter is self-protected against over-current and short circuit conditions. On the occurrence of an over-current condition, the converter will enter a pulse-by-pulse hiccup mode. On the removal of the over-current or short circuit condition, Vout will return to the original value (auto-reset).

このコンバータは過電流と短絡に対し自己保護します。過電流状態になると、このコンバータはパルスバイパルス HICCUPモードになり、過電流状態が解除されるとVoutは通常の値に戻ります。(自動リセット)

Over-Temperature Protection (OTP)

The converter is self-protected against over-temperature conditions. In case of overheating due to abnormal operation conditions, the converter will turn off automatically. It will turn back on automatically once it has cooled down to a safe temperature (auto-reset).

このコンバータは過熱保護機能を有しています。異常な動作条件によって過熱状態になると、このコンバータは自動的に停止します。安全な温度にまで下がると自動的に復帰します。(自動リセット)

Characterization

Overview

The converter has been characterized for several operational features, including thermal derating (maximum available load current as a function of ambient temperature and airflow), efficiency, power dissipation, start-up and shutdown characteristics, ripple and noise, and transient response to load step-changes.

このコンバータは温度デリーティング、効率、電力損失、スタートアップ時、及びシャットダウン時の動作、リップル・ノイズ、動的負荷変動などを含む、さまざまな動作状態で特徴付けられます。

Figures showing data plots and waveforms for different output voltages are presented in the following pages.

各出力電圧時のデータ、及び波形は以後のページに掲載されています。

Test Conditions

To ensure measurement accuracy and reproducibility, all thermal and efficiency data were taken with the converter soldered to a standardized thermal test board. The thermal test board was mounted inside FDK's custom wind tunnel to enable precise control of ambient temperature and airflow conditions.

測定精度、及び再現性を確実にするために、全ての温度、及び効率データは標準化された温度評価ボードにコンバータを半田付けして取得しています。温度評価ボードをFDK特製の風洞実験設備内に設置することで、環境温度、及び風量を精密に管理しています。

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

The thermal test board comprised a four layer printed circuit board (PCB) with a total thickness of 0.060". Copper metallization on the two outer layers was limited to pads and traces needed for soldering the converter and peripheral components to the board. The two inner layers comprised power and ground planes of 2 oz. copper. This thermal test board, with the paucity of copper on the outer surfaces, limits heat transfer from the converter to the PCB, thereby providing a worst-case but consistent set of conditions for thermal measurements.

温度評価ボードは厚さ0.060"(1.6mm)厚の4層PCBで作成しています。表面2層の銅箔はコンバータを実装するためのパッドと周辺部品へのパターンのみに限定しています。内側2層は70 μ mの銅箔で電力、及びグランドラインを形成しています。このように表層の銅箔を限りなく少なくした温度評価ボードは、コンバータからPCBへの熱の逃げを制限し、ワーストケースでありながら矛盾の無い温度評価条件を実現しています。

FDK's custom wind tunnel was used to provide precise horizontal laminar airflow in the range of 50 LFM to 600LFM, at ambient temperatures between 30°C and 85°C. Infrared (IR) thermography and thermocouples were used for temperature measurements. (See Fig. F & Fig. G)

FDK特製の風洞実験装置は水平方向の層流を50LFM(自然対流と同等, NC)から600LFMまで精密に制御でき、環境温度は30°Cから85°Cを制御できます。温度測定には赤外線(IR)サーモグラフィと熱電対を使用しています。(図F及びG参照)



Fig. F: FDK Original Wind Tunnel

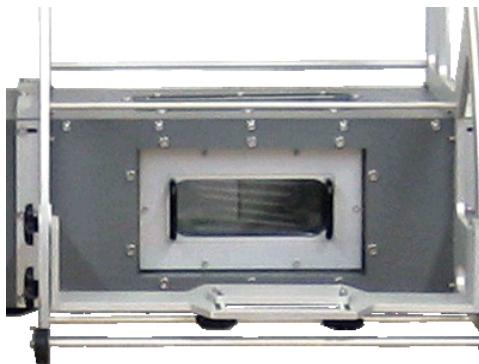


Fig. G: Test Chamber

Thermal Derating

Fig.1 shows the maximum available load current vs. ambient temperature and airflow rates. Ambient temperature was varied between 30°C and 85°C, with airflow rates from NC(50LFM) to 400LFM (0.25m/s to 2.0m/s). The converter was mounted horizontally, and the airflow was parallel to the long axis of the converter, going from pin 1 to pin 8.

図1はある環境温度と風量の条件下における最大出力電流を表します。環境温度は風量NC(50LFM)～400LFMの条件で30°C～85°Cの間を変動させています。コンバータは水平に設置し、風向きはコンバータの長手方向に平行で1番ピンから8番ピンに向けて吹いています。

The maximum available load current, for any given set of conditions, is defined as the lower of:

- (i) The output current at which the temperature of any component reaches 120°C, or
- (ii) The current rating of the converter (4A)

各々の測定条件で最大出力電流の値は下記のとおり定義します。

- (i) いずれかの部品の温度が120°Cに到達した時点の出力電流値、又は
- (ii) コンバータの公称定格電流 (4A)

Note that continuous operation beyond the derated current as specified by the derating curves (Fig.1) may lead to degradation in performance and reliability of the converter and may result in permanent damage.

出力電流「デーラーティングカーブ」(図1)で指定された定格電流を超えた連続した操作は、性能の低下、信頼性の低下、及びモジュールの破損を引き起こすことがあります。

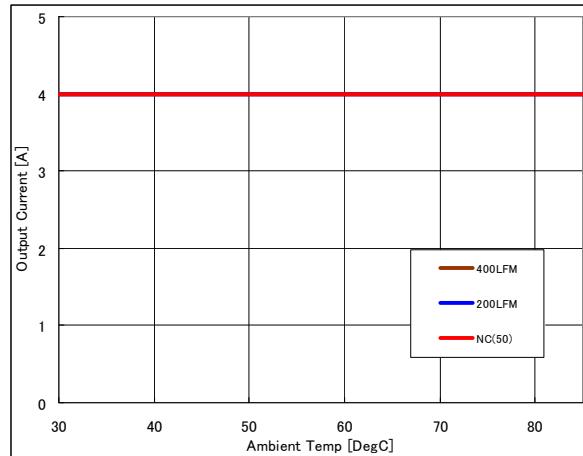


Fig.1: Output current vs. ambient temperature and air velocity at 12Vin, 0.8V to 6.6V out

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet**Test Circuit**

The test circuit setup shown in Fig. H was used to obtain the output voltage ripple and output voltage response to step load change. Fig. J was used to obtain the input reflected ripple current waveforms.

図Hに示す試験回路は出力リップル及び負荷急変の測定に使用しております。入力リップルの測定には図Jの試験回路を使用しています。

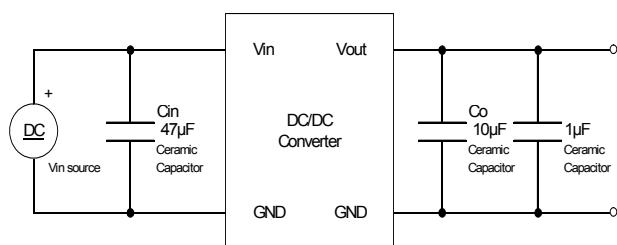


Fig. H: Test setup for measuring output voltage ripple and output voltage response to step load change

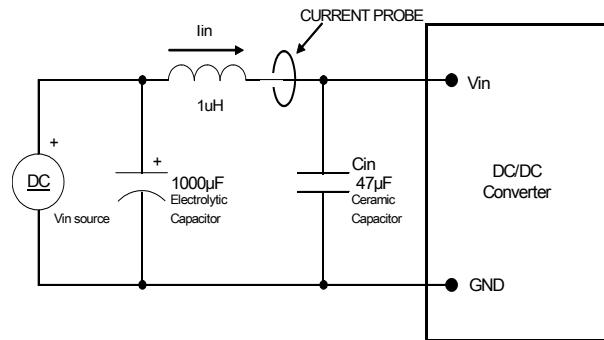


Fig. J: Test setup for measuring input reflected ripple current

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

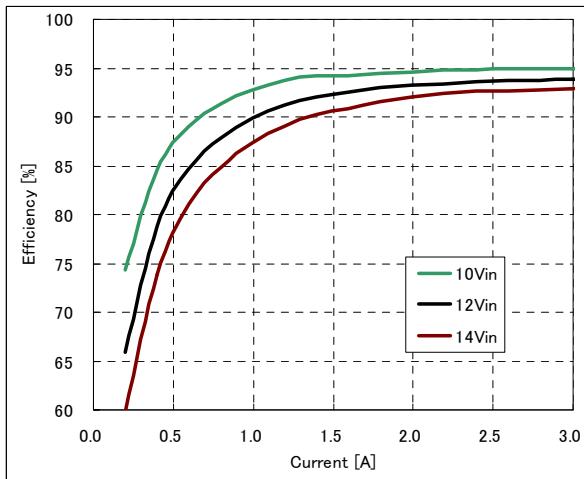


Fig.2: Efficiency vs. load current and input voltage for 6.6Vout

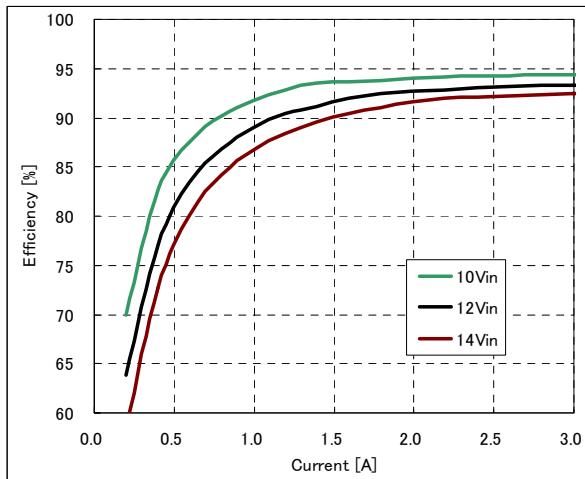


Fig.3: Efficiency vs. load current and input voltage for 6.0Vout

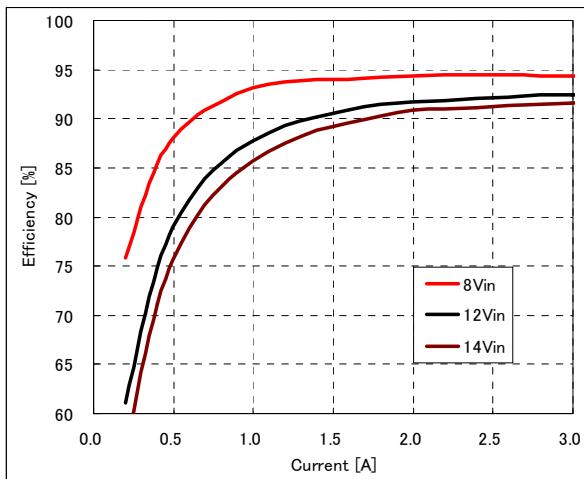


Fig.4: Efficiency vs. load current and input voltage for 5.0Vout

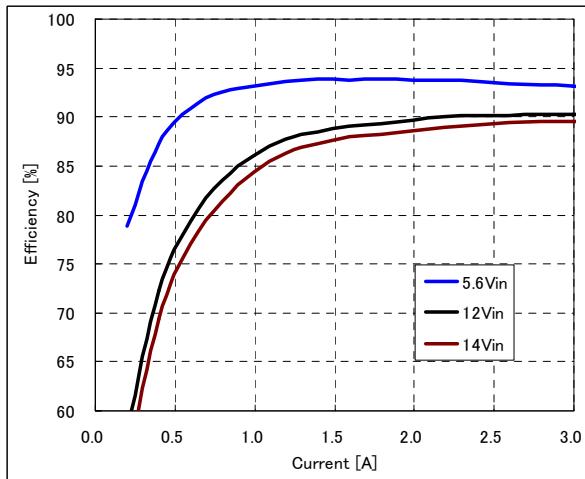


Fig.5: Efficiency vs. load current and input voltage for 3.3Vout

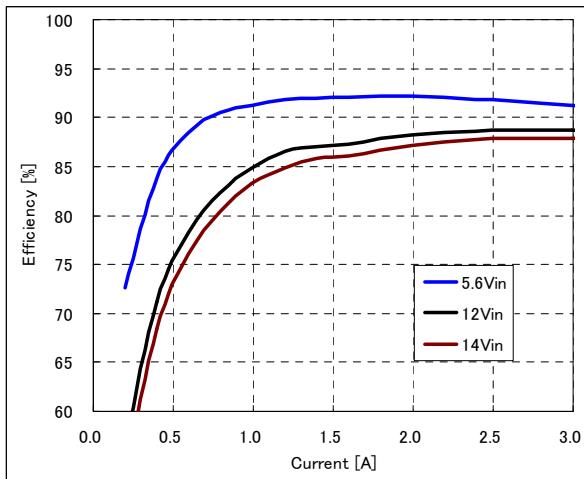


Fig.6: Efficiency vs. load current and input voltage for 2.5Vout

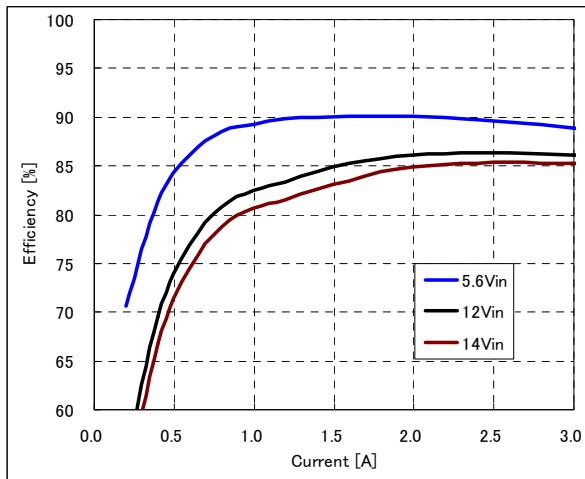


Fig.7: Efficiency vs. load current and input voltage for 1.8Vout

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

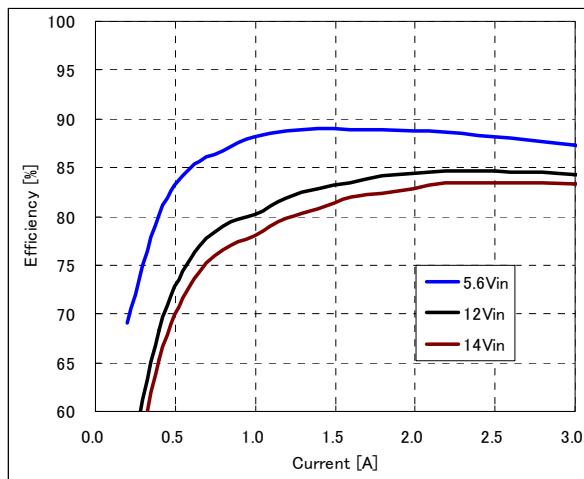
Data Sheet

Fig.8: Efficiency vs. load current and input voltage for 1.5Vout

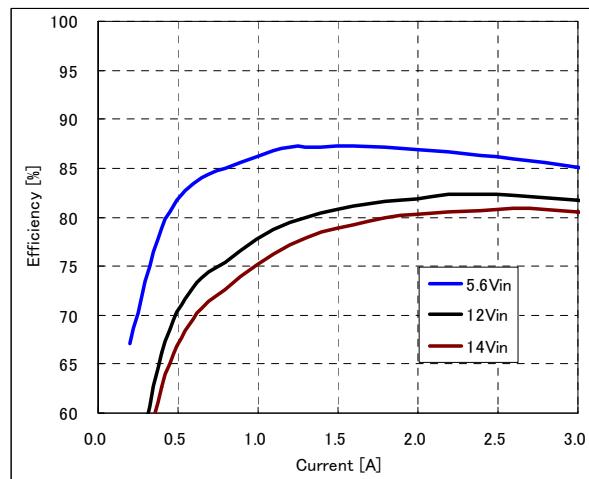


Fig.9: Efficiency vs. load current and input voltage for 1.2Vout

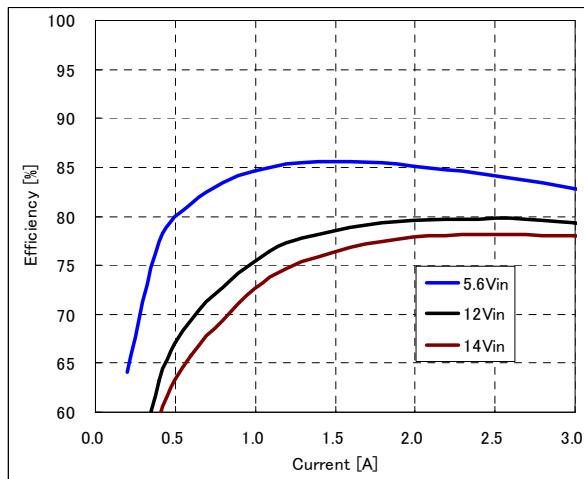


Fig.10: Efficiency vs. load current and input voltage for 1.0Vout

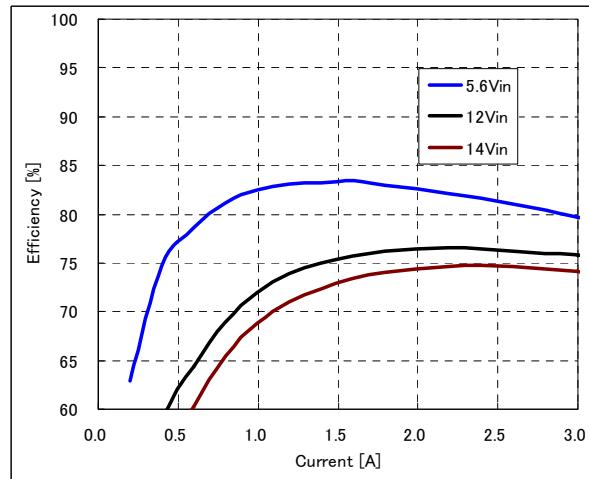


Fig.11: Efficiency vs. load current and input voltage for 0.8Vout

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

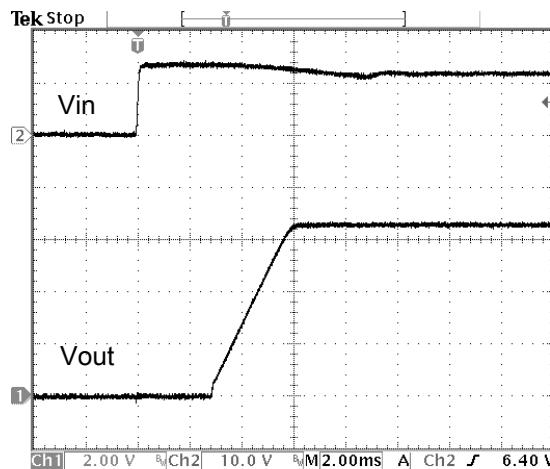


Fig.12: Turn on delay time at 12Vin, 6.6V/3A out

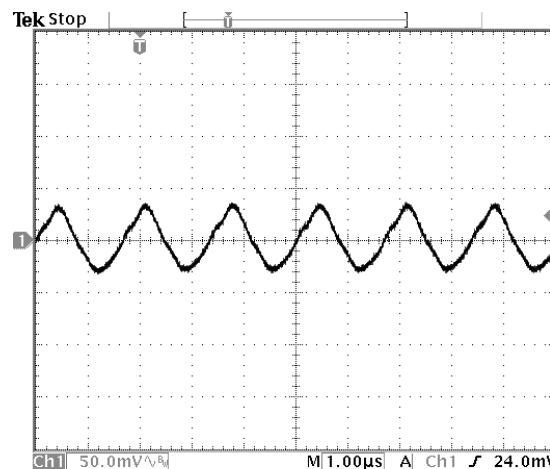


Fig.13: Output ripple and noise at 12Vin, 6.6V/3Aout

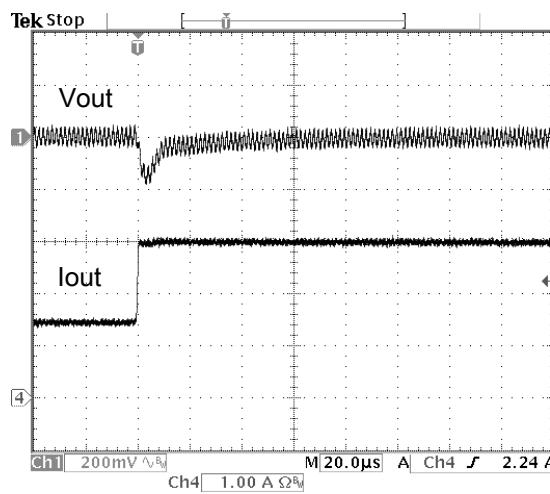


Fig.14: Output voltage response to step load change at 5A/us from 50% to 100% (12Vin, 6.6Vout)

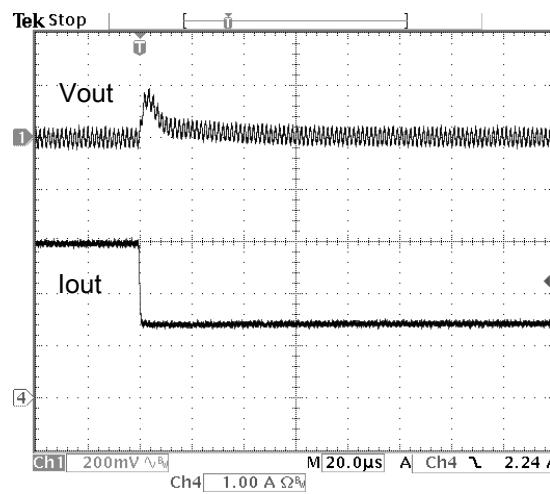


Fig.15: Output voltage response to step load change at 5A/us from 100% to 50% (12Vin, 6.6Vout)

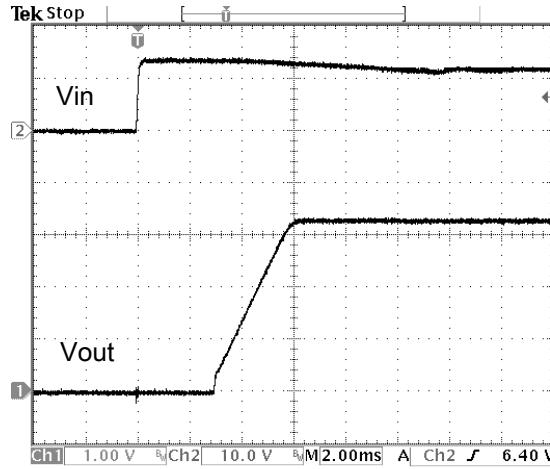


Fig.16: Turn on delay time at 12Vin, 3.3V/3A out

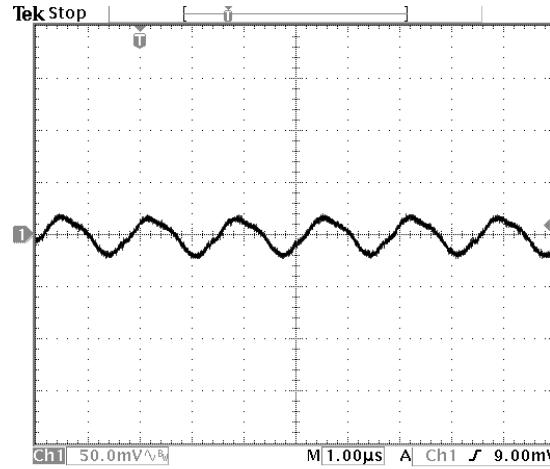


Fig.17: Output ripple and noise at 12Vin, 3.3V/3Aout

FPDK12SR8003PSS

5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

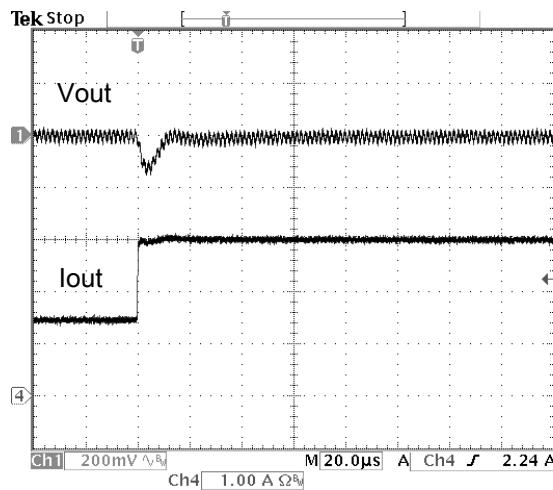


Fig.18: Output voltage response to step load change at 5A/us from 50% to 100% (12Vin, 3.3Vout)

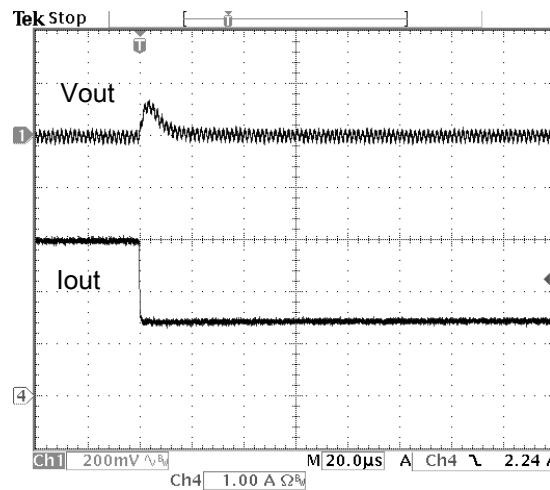


Fig.19: Output voltage response to step load change at 5A/us from 100% to 50% (12Vin, 3.3Vout)

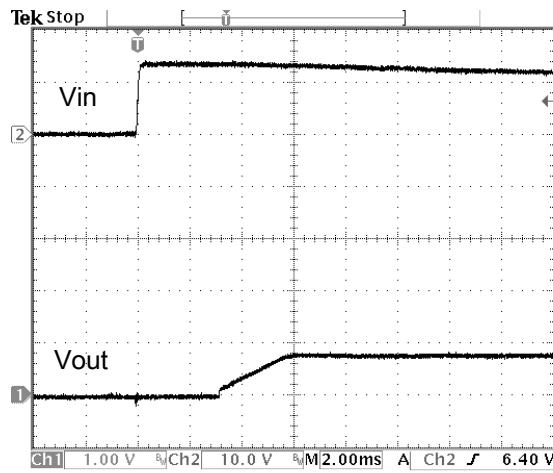


Fig.20: Turn on delay time at 12Vin, 0.8V/3A out

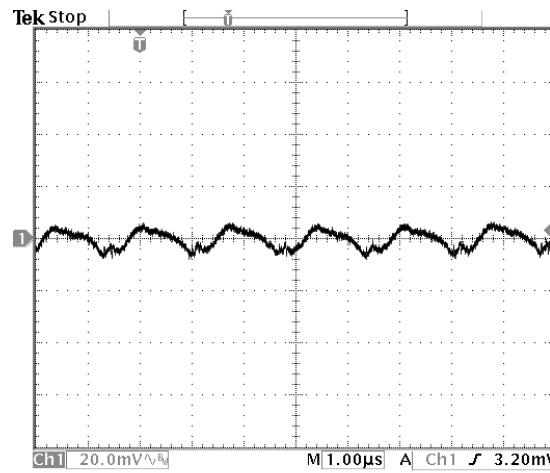


Fig.21: Output ripple and noise at 12Vin, 0.8V/3Aout

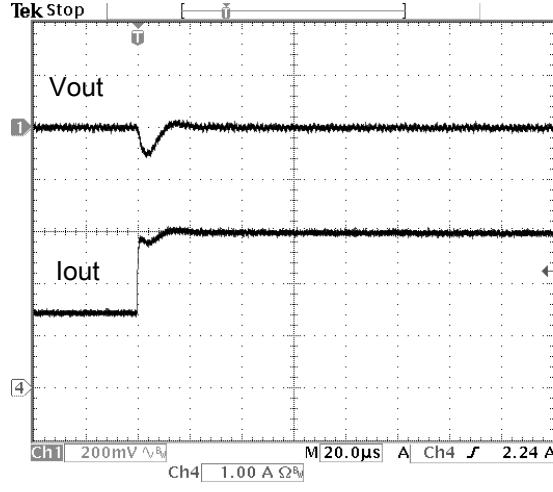


Fig.22: Output voltage response to step load change at 5A/us from 50% to 100% (12Vin, 0.8Vout)

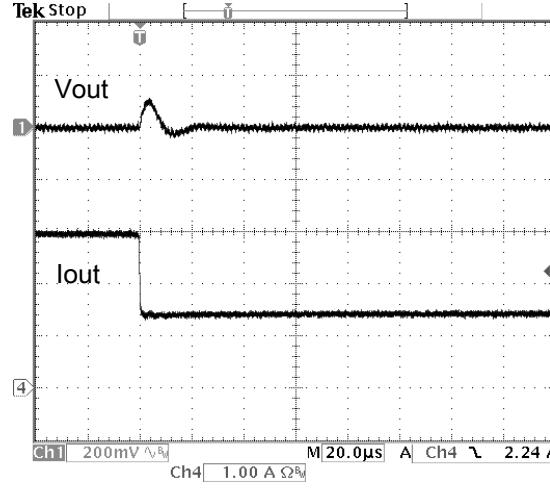


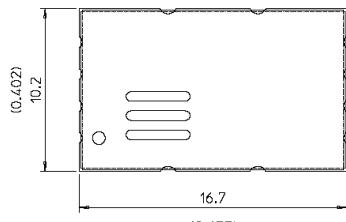
Fig.23: Output voltage response to step load change at 5A/us from 100% to 50% (12Vin, 0.8Vout)

FPDK12SR8003PSS

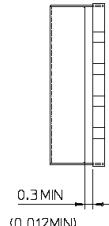
5.6-14.0Vdc Input, 3A, 0.8-6.6Vdc Output

Data Sheet

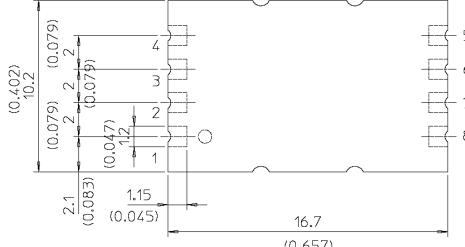
Mechanical Drawing



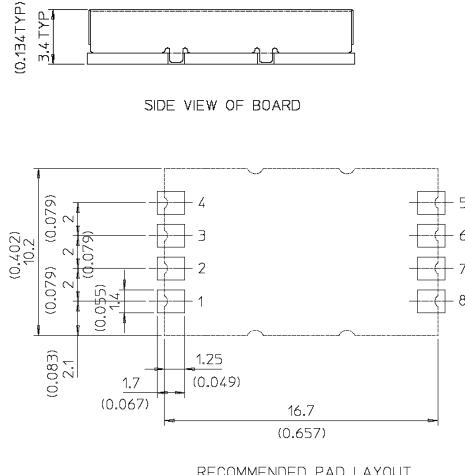
TOP VIEW OF BOARD



SIDE VIEW OF BOARD



TOP VIEW OF BOARD



RECOMMENDED PAD LAYOUT

Notes

- All dimensions are in millimeters (inches)
- Unless otherwise specified, tolerances are +/- 0.25mm
- Connector Finish: Gold over Nickel
- Converter Weight: 0.039oz (1.1g)
- The only PCB traces under the convertor should be the recommended pads, and GND traces.

Terminal Connections

| Pin# | Function | Pin# | Function |
|------|----------|------|------------|
| 1 | Vin | 5 | TRIM |
| 2 | GND | 6 | POWER GOOD |
| 3 | REMOTE | 7 | GND |
| 4 | TRACK | 8 | Vout |

DK Series Part Numbering Scheme

| Product Series | Sub Series | Nominal Input Voltage | Mounting Scheme | Output Voltage | Rated Current | ON/OFF Logic | Option1 | Option2 |
|----------------|------------|-----------------------|-----------------|---------------------------------------|---------------|--------------|----------|----------|
| FP | DK | 12 | S | R80 | 03 | P | S | S |
| Series Name | | Typ=12V | Surface Mount | 0.8V (Programmable: See page 6) | 3A | Positive | Standard | Tracking |

Notes

NUCLEAR AND MEDICAL APPLICATIONS: FDK Corporation products are not authorized for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems without the written consent of FDK Corporation.

CLEANSING : Cleansing of this converter is not recommended. When cleansing, determine a cleansing condition on your own responsibility after confirming there is no impact on the characteristics/performance of the converter.

SPECIFICATION CHANGES AND REVISIONS: Specifications are version-controlled, but are subject to change without notice.